What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042t6y6tr

List of tables

threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F042x4/x6 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1 USART1, USB or the CEC.

  The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

3.10.3 V$_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the V$_{BAT}$ battery voltage using the internal ADC channel ADC_IN18. As the V$_{BAT}$ voltage may be higher than V$_{DDA}$, and thus outside the ADC input range, the V$_{BAT}$ pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V$_{BAT}$ voltage.

3.11 Touch sensing controller (TSC)

The STM32F042x4/x6 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 14 capacitive sensing channels distributed over 5 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F042x4/x6 devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA11
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA12
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO2	PB0			
	TSC_G3_IO3	PB1			
	TSC_G3_IO4	PB2			

Table 10. STM32F042x4/x6 USART implementation (continued)

USART modes/features[1]	USART1	USART2
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F042x4/x6 SPI/I^2S implementation

SPI features[1]	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.18 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
26	-	-	-	-	-	PB13	I/O	FTf	-	SPI2_SCK, TIM1_CH1N, I2C1_SCL	-
27	-	-	-	-	-	PB14	I/O	FTf	-	SPI2_MISO, TIM1_CH2N, I2C1_SDA	-
28	-	-	-	-	-	PB15	I/O	FT	-	SPI2_MOSI, TIM1_CH3N	WKUP7, RTC_REFIN
29	E2	18	18	-	-	PA8	I/O	FT	(4)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-
30	D1	19	19	19	17	PA9	I/O	FTf	(4)	USART1_TX, TIM1_CH2, TSC_G4_IO1, I2C1_SCL	-
31	C1	20	20	20	18	PA10	I/O	FTf	(4)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2, I2C1_SDA	-
32	C2	21	21	19(5)	17(5)	PA11	I/O	FTf	(4)	CAN_RX, USART1_CTS, TIM1_CH4, TSC_G4_IO3, EVENTOUT, I2C1_SCL	USB_DM
33	A1	22	22	20(5)	18(5)	PA12	I/O	FTf	(4)	CAN_TX, USART1_RTS, TIM1_ETR, TSC_G4_IO4, EVENTOUT, I2C1_SDA	USB_DP
34	B1	23	23	21	19	PA13	I/O	FT	(4) (6)	IR_OUT, SWDIO USB_NOE	-
35	-	-	-	-	-	VSS	S	-	-	Ground	
36	E1	17	17	18	16	VDDIO2	S	-	-	Digital power supply	
37	B2	24	24	22	20	PA14	I/O	FT	(4) (6)	USART2_TX, SWCLK	-

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
38	A2	25	25	23	-	PA15	I/O	FT	(4)	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT, USB_NOE	-
39	B3	26	26	24	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
40	A3	27	27	25	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
41	E6	28	28	26	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
42	C4	29	29	27	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
43	A4	30	30	28	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
44	-	-	31	-	-	PF11-BOOT0	I/O	FT	-	-	Boot memory selection
-	B4	31	-	1	1	PB8-BOOT0	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	Boot memory selection
45	-	-	32	-	-	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions	Figure 12. Pin input voltage

Figure 11. Pin loading conditions

C = 50 pF — MCU pin

MS19210V1

Figure 12. Pin input voltage

V_{IN} — MCU pin

MS19211V1
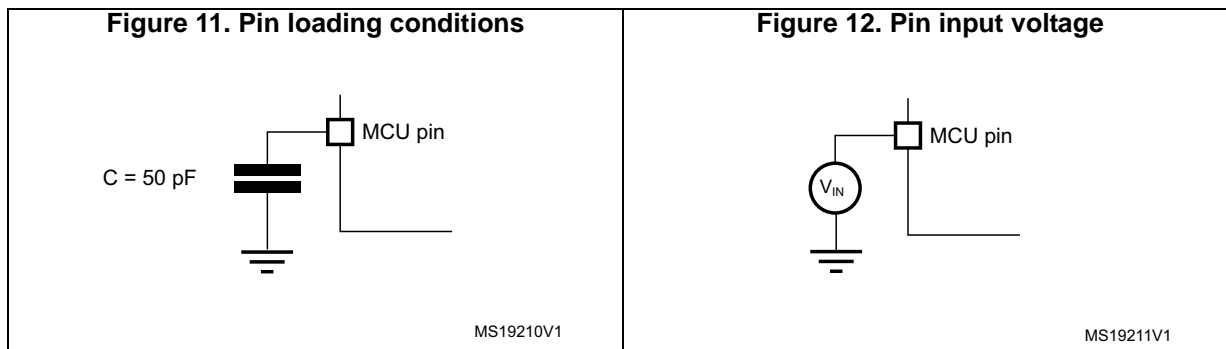
6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics[1]

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	- 0.3	4.0	V
V_{DDIO2}–V_{SS}	External I/O supply voltage	- 0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for V_{DD} > V_{DDA}	-	0.4	V
V_{BAT}–V_{SS}	External backup supply voltage	- 0.3	4.0	V
V_{IN}[2]	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DDIOx} + 4.0 [3]	V
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	V
	Input voltage on any other pin	V_{SS} - 0.3	4.0	V
$|\Delta V_{DDx}|$	Variations between different V_{DD} power pins	-	50	mV
$|V_{SSx} - V_{SS}|$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.

3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 24. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$[1]	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26[1]	µA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10[1]	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4[1]	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10[1]	mV
T_{Coeff}	Temperature coefficient	-	- 100[1]	-	100[1]	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 32*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*

Table 32. Peripheral current consumption

	Peripheral	Typical consumption at 25 °C	Unit
AHB	BusMatrix[1]	2.2	µA/MHz
	CRC	1.9	
	DMA	5.1	
	Flash memory interface	15.0	
	GPIOA	8.2	
	GPIOB	7.7	
	GPIOC	2.1	
	GPIOF	1.8	
	SRAM	1.1	
	TSC	4.9	
	All AHB peripherals	**49.8**	

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram

MS19214V2
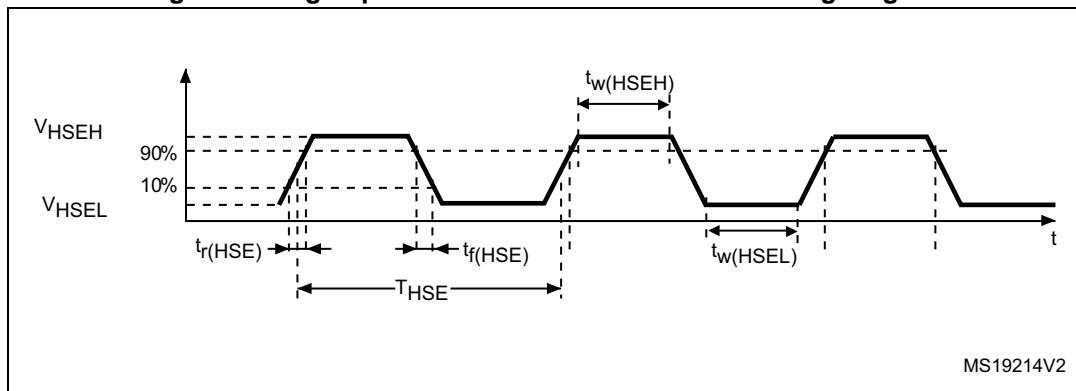
Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 35. Low-speed external user clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram

MS19215V2
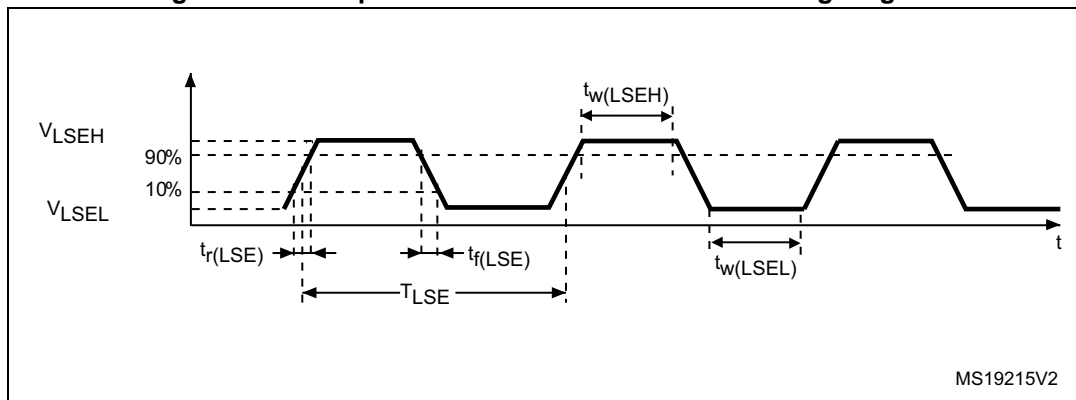
High-speed internal (HSI) RC oscillator

Table 38. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1[2]	%
$DuCy_{(HSI)}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8[3]	-	3.8[3]	%
		T_A = -10 to 85°C	-1.9[3]	-	2.3[3]	
		T_A = 0 to 85°C	-1.9[3]	-	2[3]	
		T_A = 0 to 70°C	-1.3[3]	-	2[3]	
		T_A = 0 to 55°C	-1[3]	-	2[3]	
		T_A = 25°C[4]	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100[2]	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

4. Factory calibrated, parts not soldered.

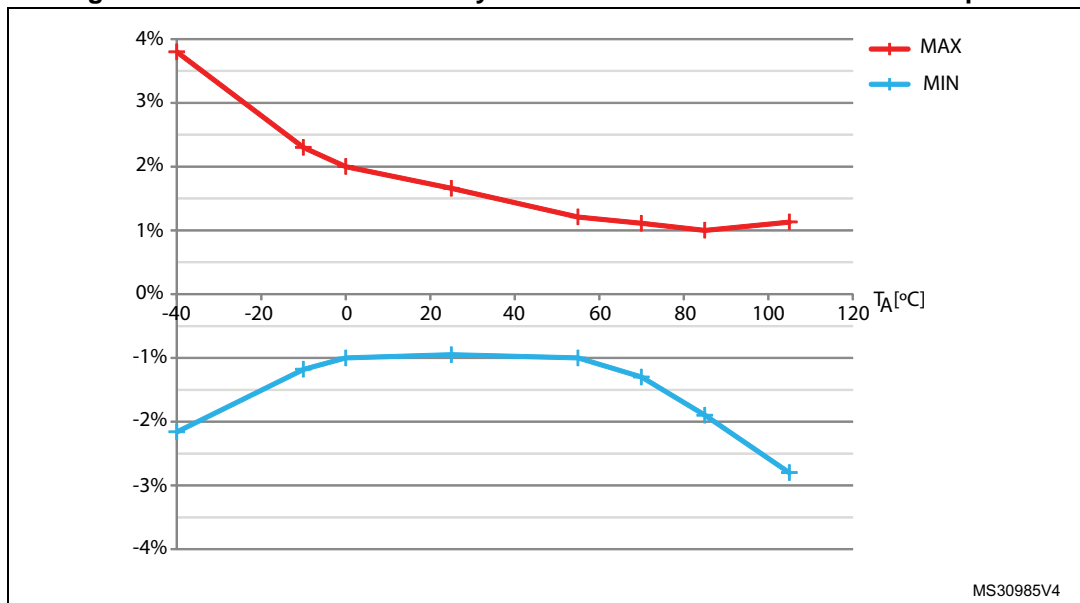**Figure 19. HSI oscillator accuracy characterization results for soldered parts**

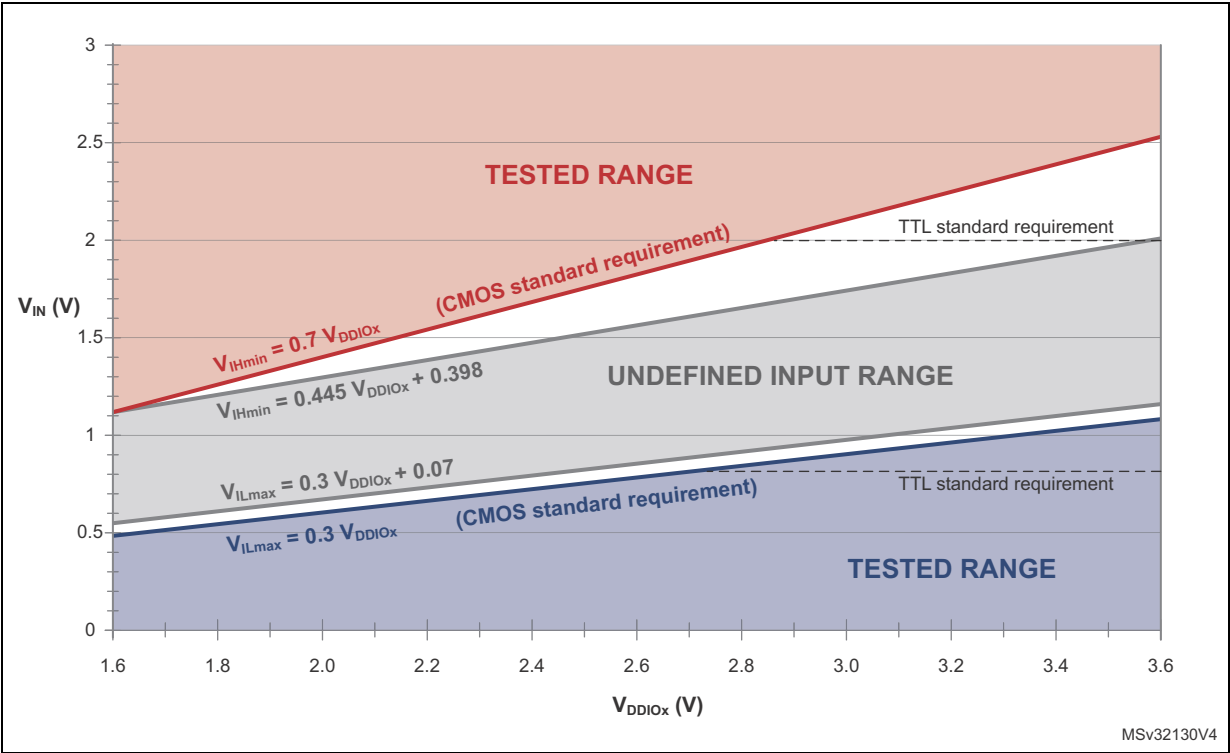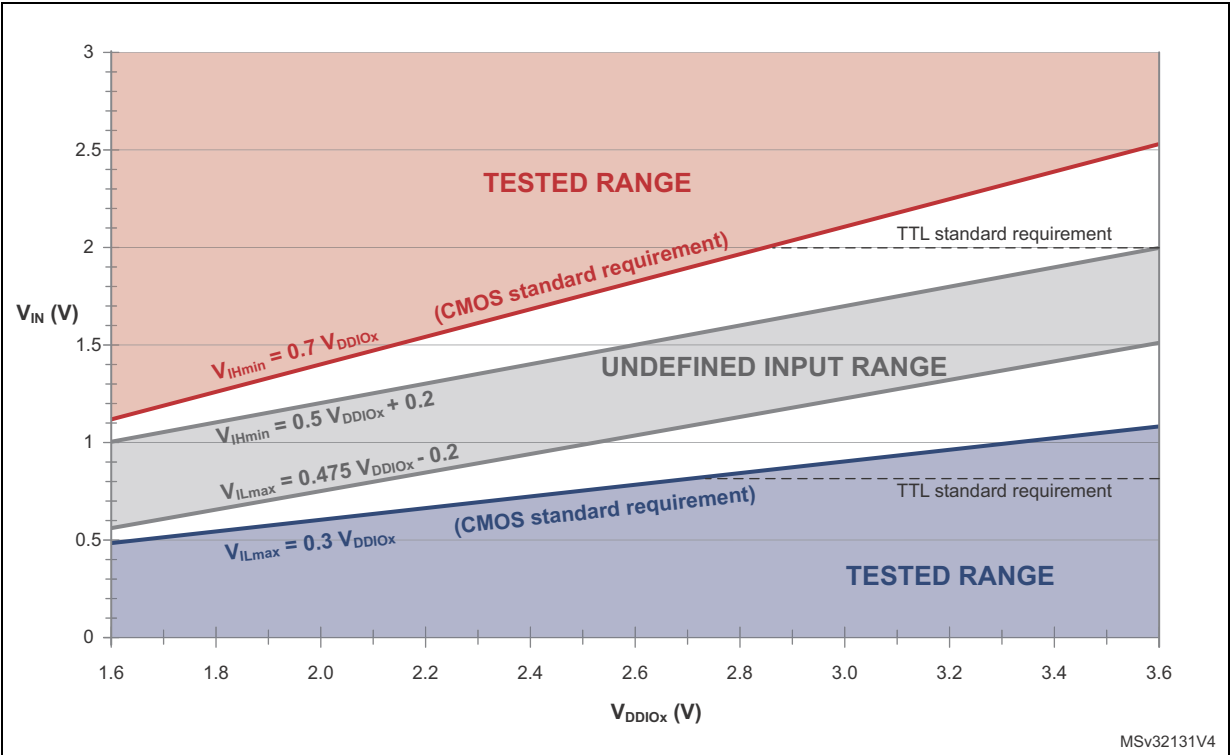**Figure 22. TC and TTa I/O input characteristics**

Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).

- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 51. Output voltage characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port[2] $\|I_{IO}\| = 8$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port[2] $\|I_{IO}\| = 8$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}[3]	Output low level voltage for an I/O pin	$\|I_{IO}\| = 20$ mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}[3]	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}[3]	Output low level voltage for an I/O pin	$\|I_{IO}\| = 6$ mA $V_{DDIOx} \geq 2$ V	-	0.4	V
V_{OH}[3]	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}[4]	Output low level voltage for an I/O pin	$\|I_{IO}\| = 4$ mA	-	0.4	V
V_{OH}[4]	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	V
V_{OLFm+}[3]	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\| = 20$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\| = 10$ mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. Data based on characterization results. Not tested in production.

4. Data based on characterization results. Not tested in production.
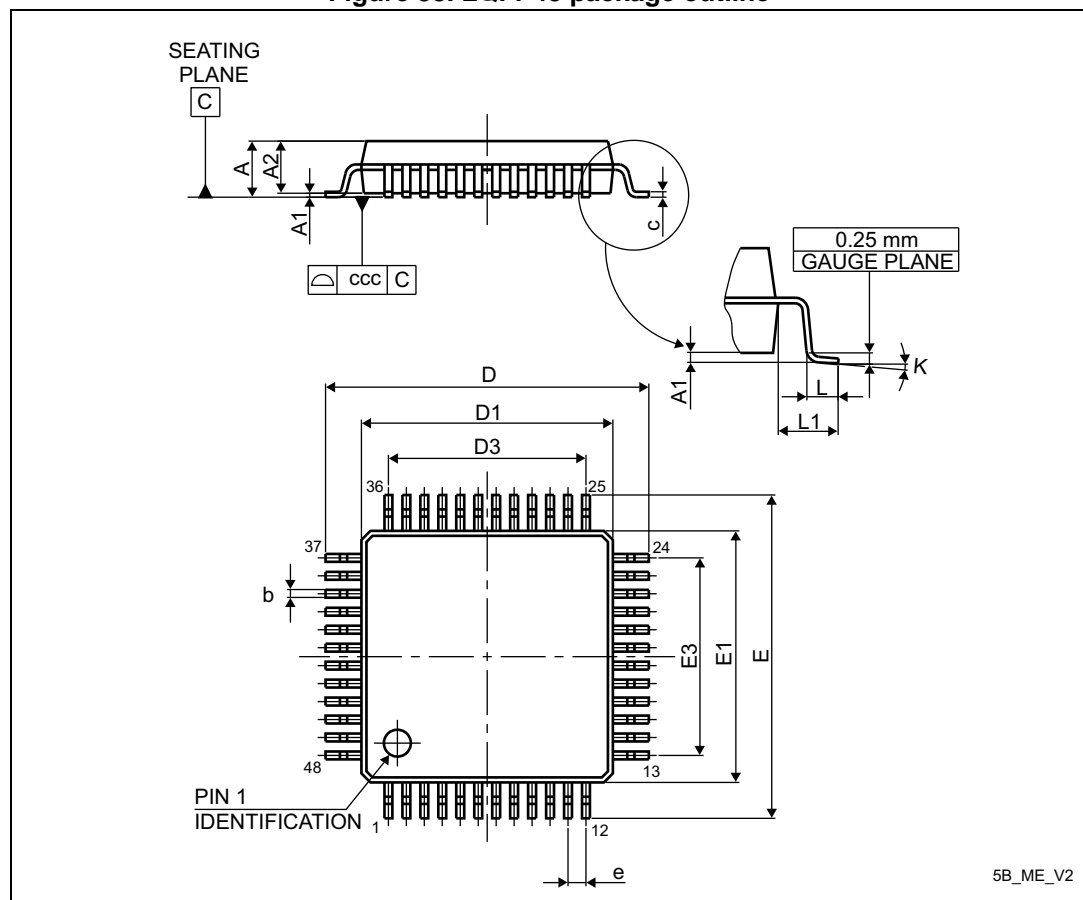
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.
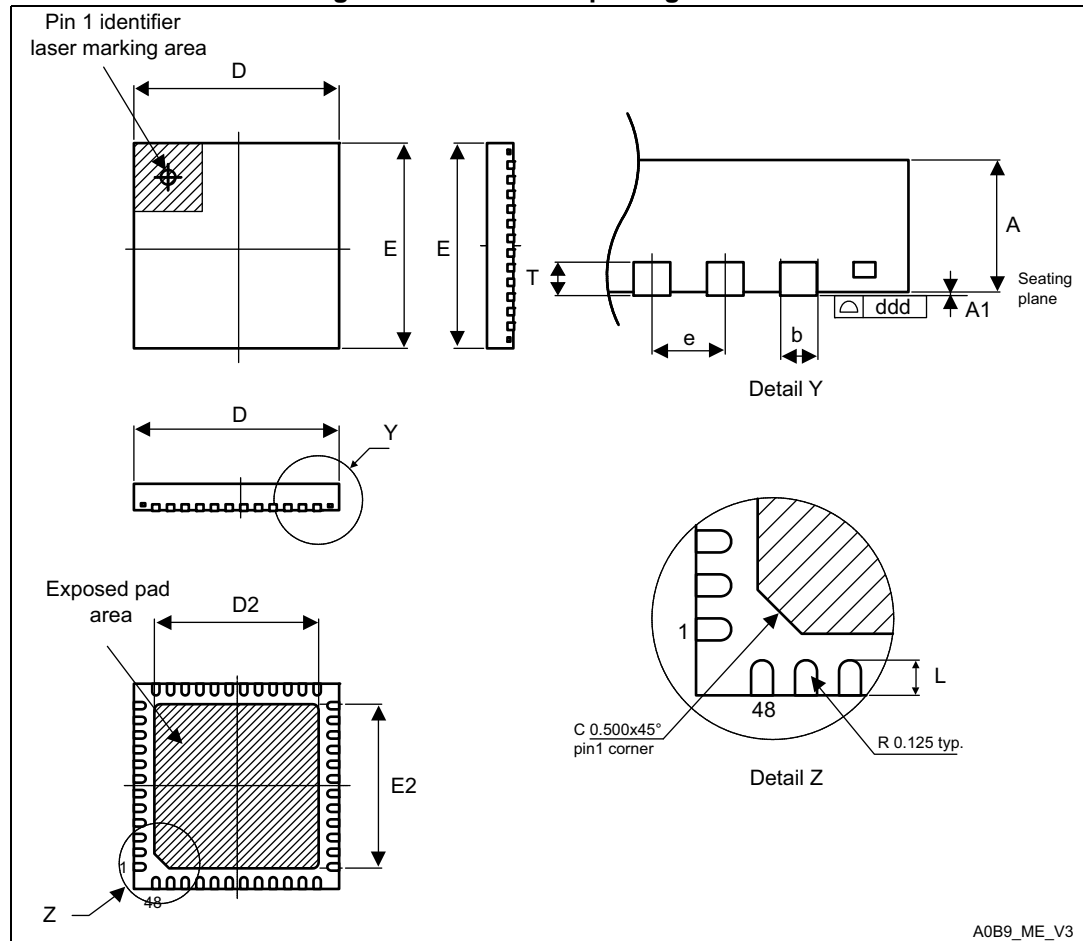
Figure 33. LQFP48 package outline

1. Drawing is not to scale.

7.2 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

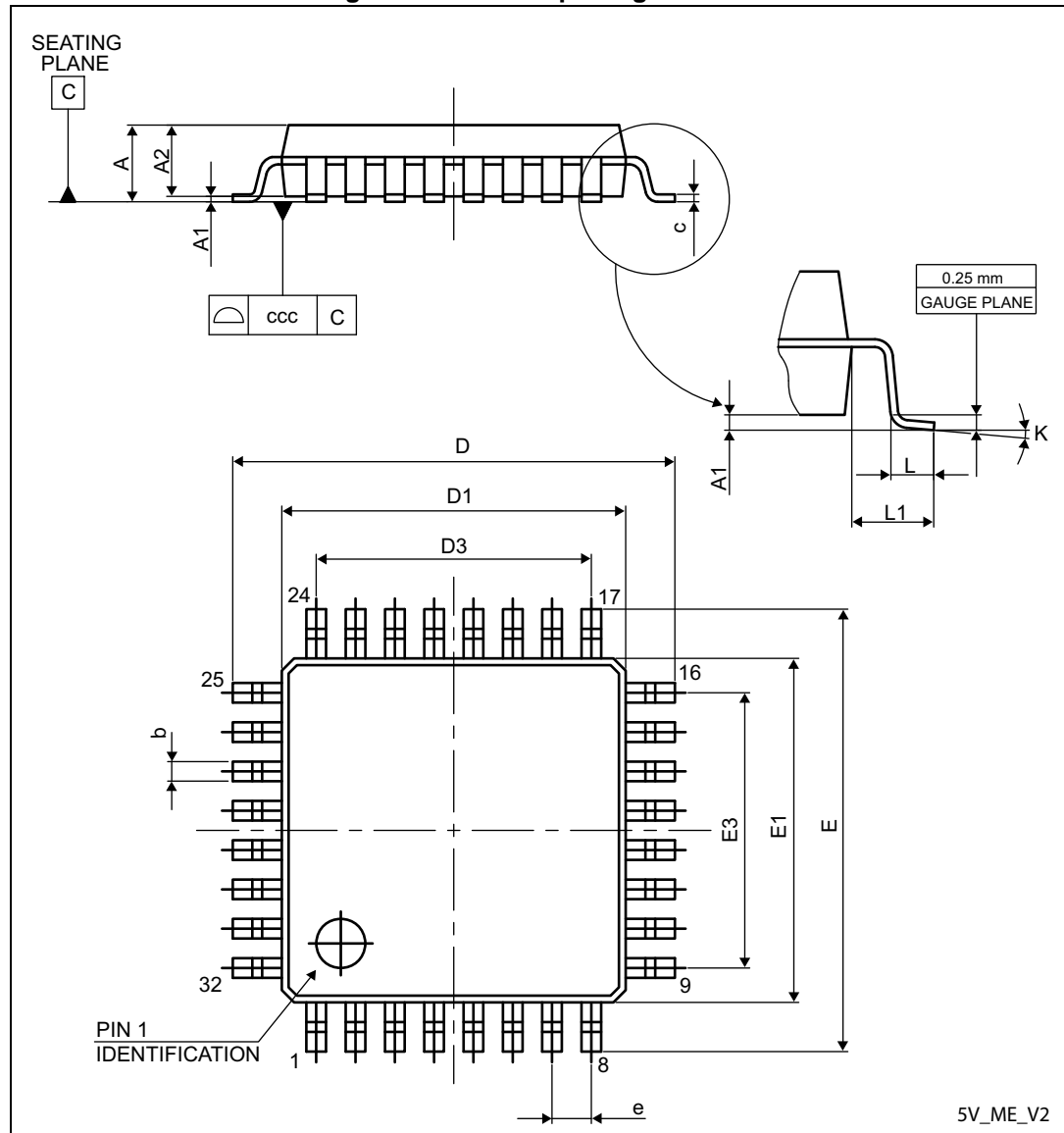**Figure 36. UFQFPN48 package outline**

1. Drawing is not to scale.

2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.

3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.
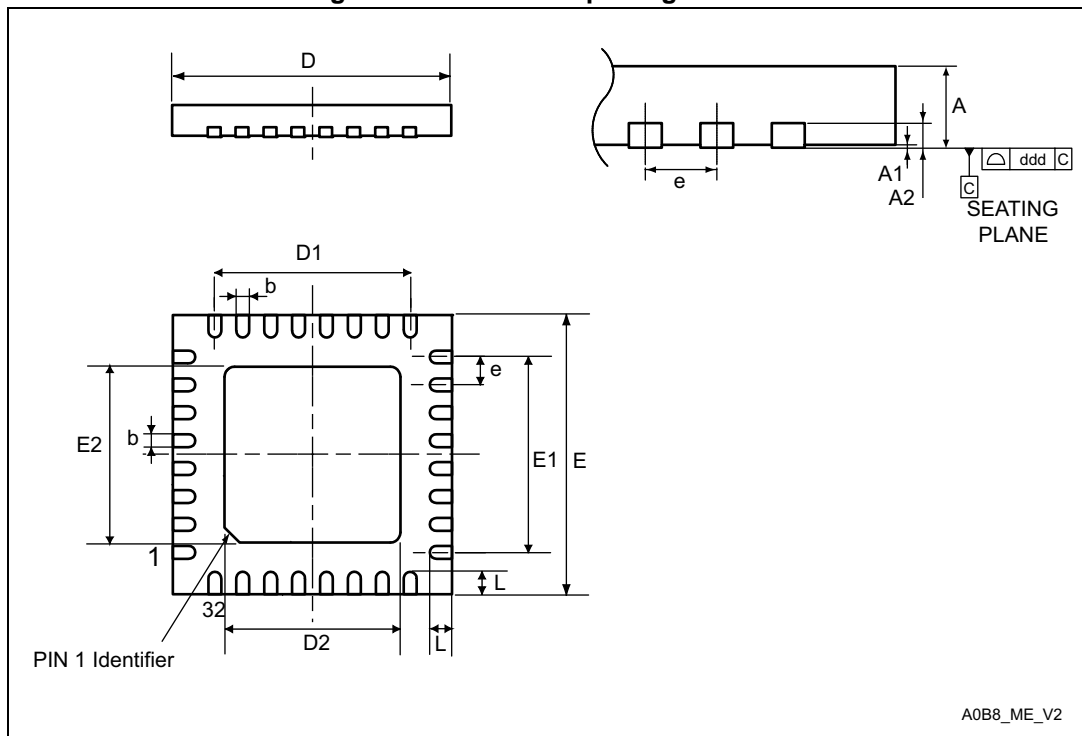
7.4   LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 42. LQFP32 package outline

1.   Drawing is not to scale.

Figure 45. UFQFPN32 package outline

1. Drawing is not to scale.

2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.

3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table: Pin definitions*.