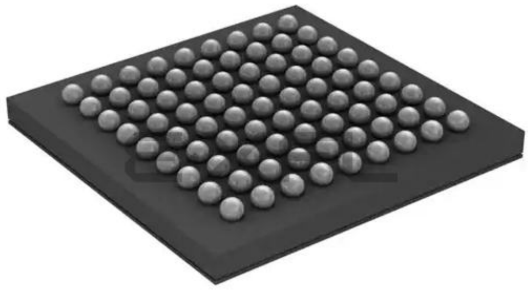

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-UFBGA, WLCSP
Supplier Device Package	81-WLCSP (4.04x3.95)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413mgy6tr

3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C and I^2CFMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- DAC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter
- SAI.

3.10 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 15 input capture/output compare/PWMs

TIM2. TIM3, TIM4 and TIM5 general-purpose timers can operate together or in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM output.

TIM2. TIM3, TIM4 and TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13 and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13 and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM2. TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

3.22.3 Basic timer (TIM6, TIM7)

TIM6 and TIM7 timers are basic 16-bit timers. They support independent DMA request generation.

3.22.4 Low-power timer (LPTIM1)

The low-power timer (LPTIM1) features an independent clock and runs in Stop mode if it is clocked by LSE, LSI or by an external clock. LPTIM1 is able to wakeup the devices from Stop mode.

The low-power timer main features are the following:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB1 clock
  - External clock source over LPTIM1 input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode
- Active in Stop mode.

3.22.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-
-	-	-	-	-	E4	15	PF5	I/O	FT	-	TIM5_CH3, FSMC_A5, EVENTOUT	-
-	-	D8	10	F2	D2	16	VSS	S	-	-	-	-
-	-	E8	11	G2	D3	17	VDD	S	-	-	-	-
-	-	-	-	-	F3	18	PF6	I/O	FT	-	TRACED0, TIM10_CH1, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT	-
-	-	-	-	-	F2	19	PF7	I/O	FT	-	TRACED1, TIM11_CH1, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	G3	20	PF8	I/O	FT	-	SAI1_SCK_B, UART8_RX, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	G2	21	PF9	I/O	FT	-	SAI1_FS_B, UART8_TX, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	G1	22	PF10	I/O	FT	-	TIM1_ETR, TIM5_CH4, EVENTOUT	-
5	5	E9	12	F1	D1	23	PH0 - OSC_IN	I/O	FT	(6)	EVENTOUT	OSC_IN
6	6	F9	13	G1	E1	24	PH1 - OSC_OUT	I/O	FT	(6)	EVENTOUT	OSC_OUT
7	7	G9	14	H2	F1	25	NRST	I/O	RST	-	-	NRST
-	8	F8	15	H1	H1	26	PC0	I/O	FT	-	LPTIM1_IN1, DFSDM2_CKIN4, SAI1_MCLK_B, EVENTOUT	ADC1_IN10, WKUP2

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
28	36	H1	54	K10	L12	76	PB15	I/O	FTf	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	NC	55	-	L9	77	PD8	I/O	FT	(2)	USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT	-
-	-	F2	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	G1	57	J12	J9	79	PD10	I/O	FT	(7)	USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	NC	58	J11	H9	80	PD11	I/O	FT	(2)	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	NC	59	J10	L10	81	PD12	I/O	FTf	(2)	TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	NC	60	H12	K10	82	PD13	I/O	FTf	(2)	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	NC	61	H11	K11	85	PD14	I/O	FTf	(2)	TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT	-

Table 13. STM32F413xG/H register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 0x5006 0BFF	RNG
	0x5004 0000 - 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 4000 - 0X4002 5FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage on RST, FT and TC pins[7]	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	- 0.3	-	V_{DDA} + 0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P_D	Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7[8]	UFQFPN48	-	-	625	mW
		WLCSP81	-	-	504	
		LQFP64	-	-	426	
		LQFP100	-	-	465	
		LQFP144		-	571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	417	
	Power dissipation at TA = 125°C for range 3[8]	UFQFPN48	-	-	156	
		WLCSP81	-	-	126	
		LQFP64	-	-	106	
		LQFP100	-	-	116	
		LQFP144	-	-	143	
		UFBGA100	-	-	088	
		UFBGA144	-	-	104	
T_A	Ambient temperature for range 6	Maximum power dissipation	–40	-	85	°C
		Low power dissipation[9]	–40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	–40	-	105	
		Low power dissipation[9]	–40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	–40	-	125	
		Low power dissipation[9]	–40	-	130	
T_J	Junction temperature range	Range 6	–40	-	105	
		Range 7	–40	-	125	
		Range 3	–40	-	130	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 75: ADC characteristics*.
3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF}+ < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB}. For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required.
(some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Note: This feature is only available for UFBGA100 and UFBGA144 packages.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage @ 3.3V.

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60(1)	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	

Table 29. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max[1]				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled[2]	100	42.3	45.08	45.76	47.88	51.71	mA
			84	34.6	36.87	37.58	39.64	43.32	
			64	25.5	27.18	27.93	29.90	33.23	
			50	20.2	21.55	22.50	24.34	27.73	
			25	10.9	11.61	12.87	14.72	18.08	
			20	9.3	9.86	11.20	13.13	16.41	
		HSI, PLL OFF, all peripherals enabled	16	6.9	7.37	8.81	10.72	14.04	
			1	1.2	1.83	3.09	4.83	8.19	
		External clock, PLL ON[2] all peripherals disabled	100	24.7	26.76	27.84	29.93	33.66	
			84	20.5	22.18	23.25	25.33	28.98	
			64	15.9	17.13	18.23	20.18	23.46	
			50	12.7	13.68	14.95	16.71	20.13	
			25	7.1	7.57	9.01	10.88	14.25	
			20	6.1	6.61	7.98	9.80	13.11	
		HSI, PLL OFF, all peripherals disabled	16	4.5	5.00	6.44	8.33	11.63	
			1	1.0	1.61	2.94	4.65	8.06	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 30. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	42.9	45.86	45.76	47.88	51.71	mA
			84	35.4	37.90	38.16	40.01	43.26	
			64	26.2	28.19	28.74	30.37	33.54	
			50	20.7	22.32	22.50	24.34	27.73	
			25	11.1	11.87	12.87	14.72	18.08	
			20	9.4	10.05	11.26	13.16	16.46	
		HSI, PLL OFF, all peripherals enabled	16	7.1	7.72	9.06	10.90	14.29	
			1	1.2	1.84	3.10	4.84	8.20	
		External clock, PLL ON(2) all peripherals disabled	100	25.4	27.83	27.84	29.93	33.66	
			84	21.4	23.44	24.10	25.77	29.04	
			64	16.6	18.31	19.17	20.72	23.86	
			50	13.2	15.10	14.95	16.71	20.13	
			25	7.2	7.90	9.01	10.88	14.25	
			20	6.2	6.83	8.05	9.88	13.15	
		HSI, PLL OFF, all peripherals disabled	16	4.8	5.37	6.70	8.52	11.89	
			1	1.0	1.62	2.96	4.67	8.07	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)

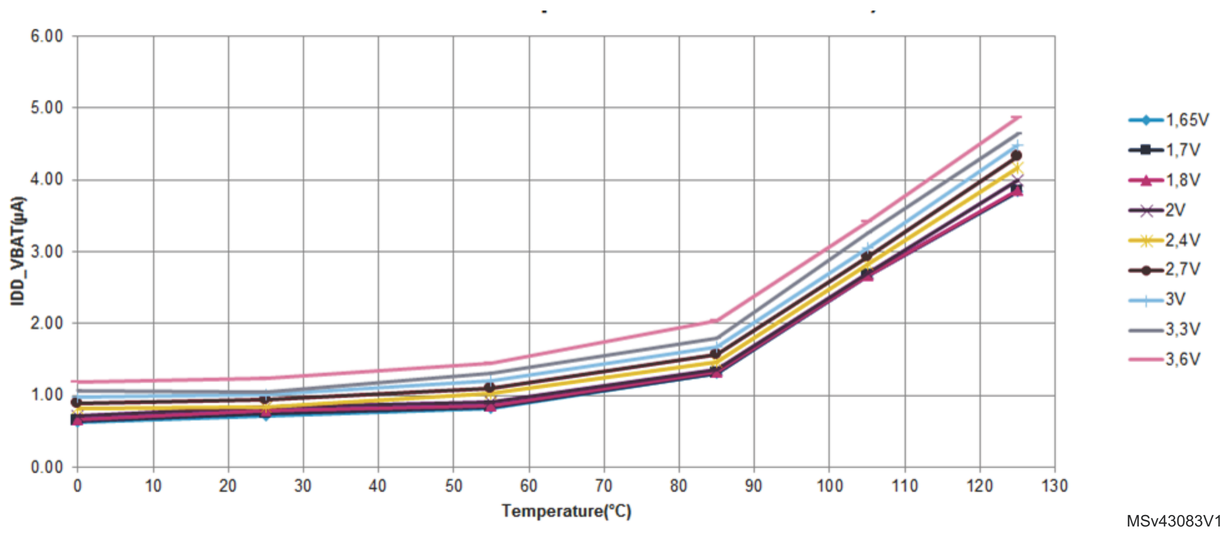
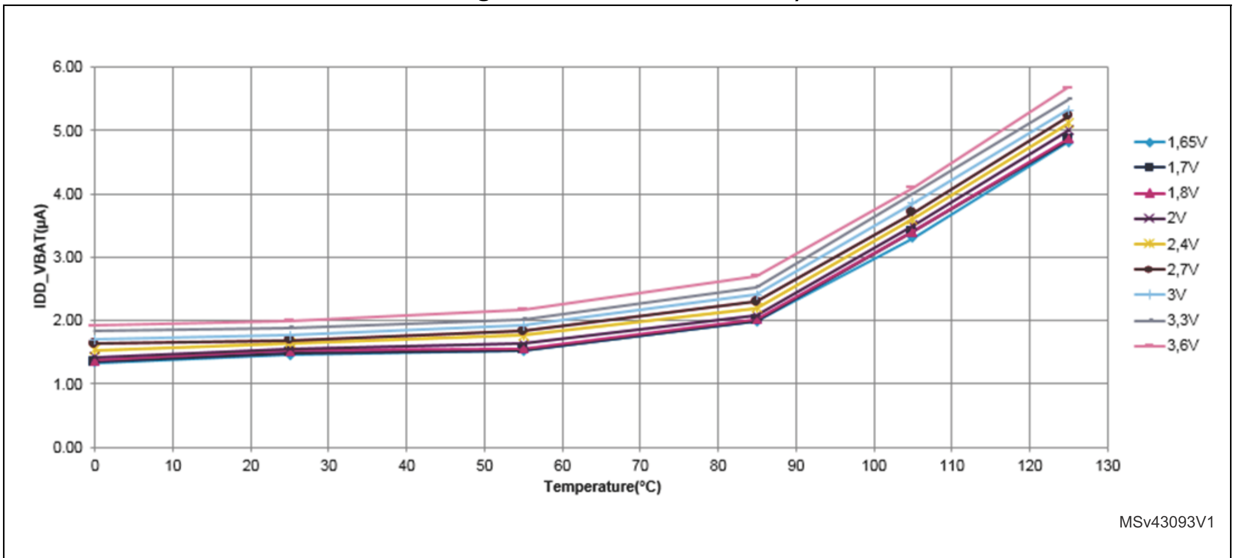


Figure 25. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 39: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 71. QSPI dynamic characteristics in DDR mode[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low time	-	$t_{(CK)}$ / 2 - 1	-	$t_{(CK)}$ / 2	ns
$t_{w(CKL)}$			$t_{(CK)}$ / 2	-	$t_{(CK)}$ / 2 + 1	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	2.7 V < V_{DD} < 3.6 V	0.5	-	-	
		1.71 V < V_{DD} < 3.6 V	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<3.6 V	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	9	
		1.71 V<V_{DD}<3.6 V	-	8.5	11.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	7.5	-	-	

1. Guaranteed by characterization results.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 72. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$[1]	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 73. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.[1]	Typ.	Max.[1]	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0[2]	-	3.6	V
	V_{DI}[3]	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}[3]	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}[3]	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V[4]	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}[4]	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 75* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

Table 75. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA} - V_{REF+} < 1.2$ V	$1.7^{(1)}$	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} - V_{REF+} < 1.2$ V	$1.7^{(1)}$	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	V
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.7^{(1)}$ to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(2)}$	External input impedance	See *Equation 1* for details	-	-	50	kΩ
$R_{ADC}^{(2)(4)}$	Sampling switch resistance	-	-	-	6	kΩ
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	4	7	pF
$t_{lat}^{(2)}$	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	$3^{(5)}$	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	$2^{(5)}$	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	-	2	3	µs
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 86. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	-	3	6	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

Table 94. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4 * T_{HCLK} - 1$	$4 * T_{HCLK} + 1$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FSMC_NWE low time	$2 * T_{HCLK} - 0.5$	$2 * T_{HCLK} - 0.5$	
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 0.5$	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	0.5	
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}	$T_{HCLK} + 1$	
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high)	$T_{HCLK} + 0.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 2.5$	
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$9 * T_{HCLK} - 1$	$9 * T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$7 * T_{HCLK} - 0.5$	$7 * T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6 * T_{HCLK} + 2$	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * T_{HCLK} - 1$	-	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 57 through *Figure 60* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Table 100. SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	1	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	12	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	10.5	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	1	-	-	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	2	3	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	1	-	-	ns

1. Guaranteed by characterization results.
2. V_{DD} = 2.7 to 3.6 V.

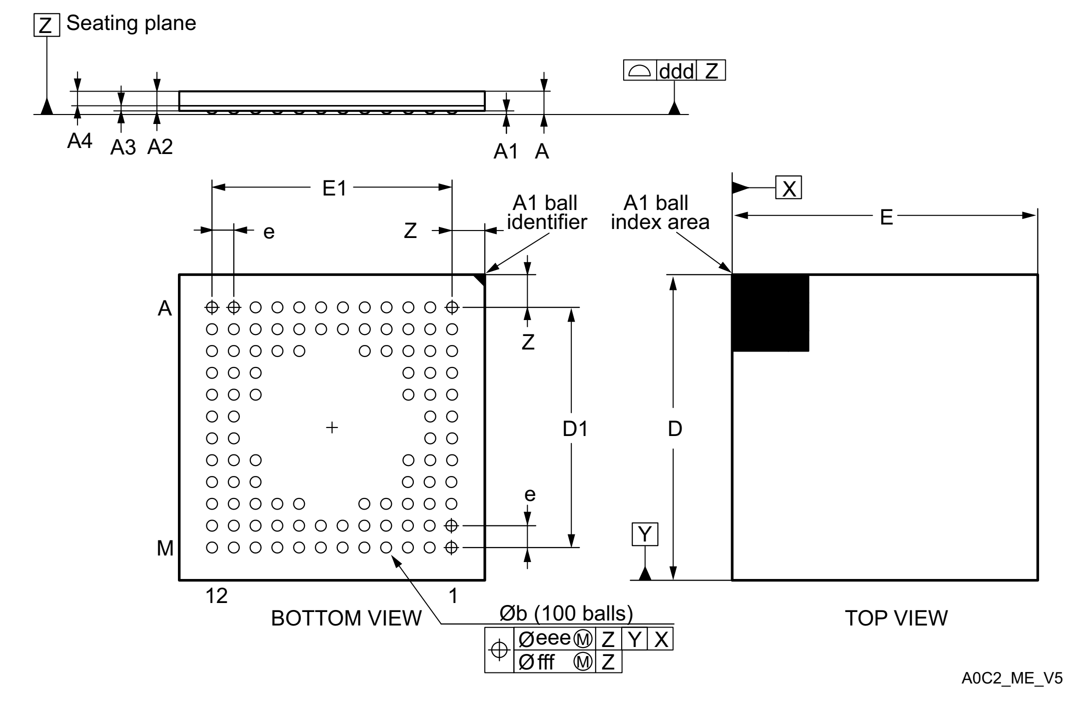
Table 101. eMMC characteristics V_{DD} = 1.7 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	15	15.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	13	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20 pF.

7.6 UFBGA100 package information

Figure 78. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 17: General operating conditions*.

The maximum chip-junction temperature, T_J max., in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (PD max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- PD max is the sum of P_{INT} max and $P_{I/O}$ max (PD max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm	35	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm	47	
	Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	48	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm	57	
	Thermal resistance junction-ambient WLCSP81 - 4.039 x 3.951 mm	39.7	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm	32	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Appendix B Application block diagrams

B.1 Sensor Hub application example

Figure 84. Sensor Hub application example