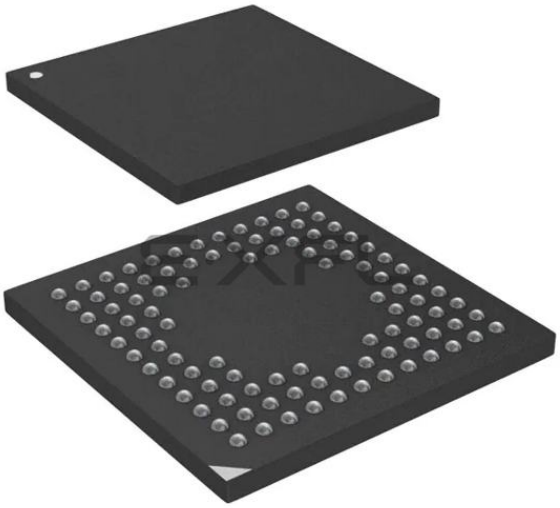

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413vgh6

List of figures

Figure 2. Compatible board design for LQFP64 package

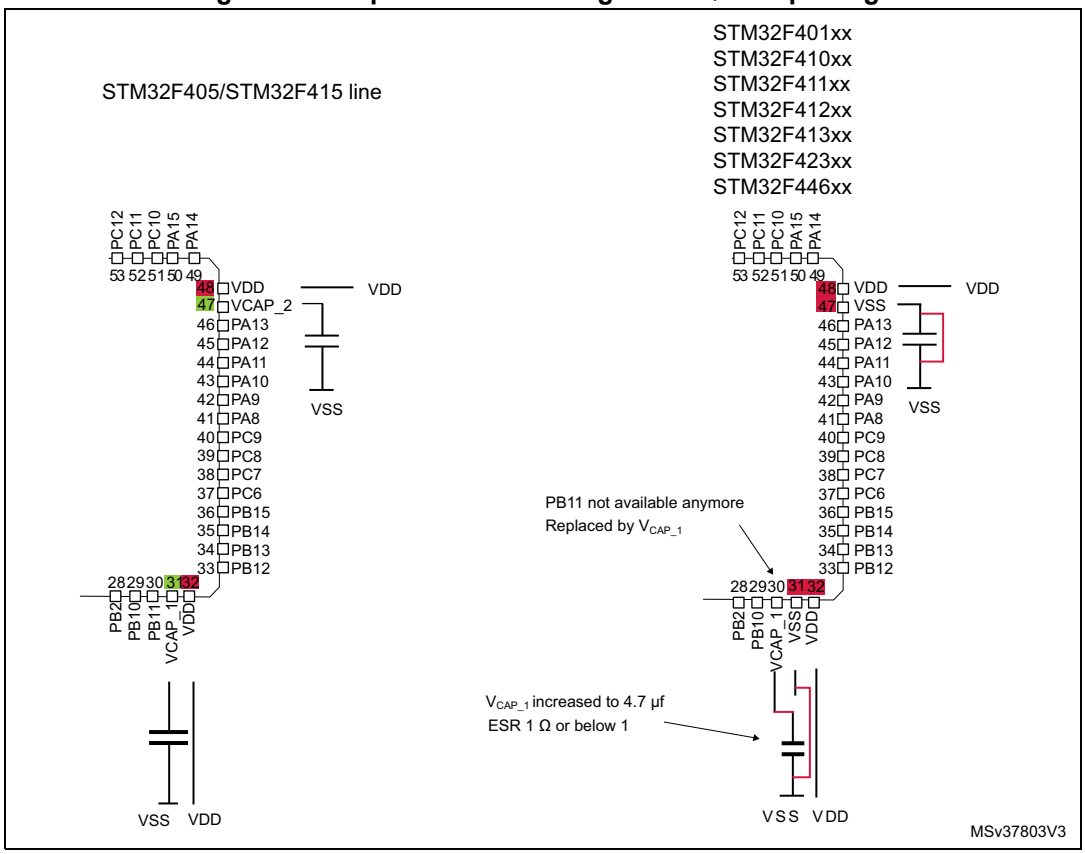
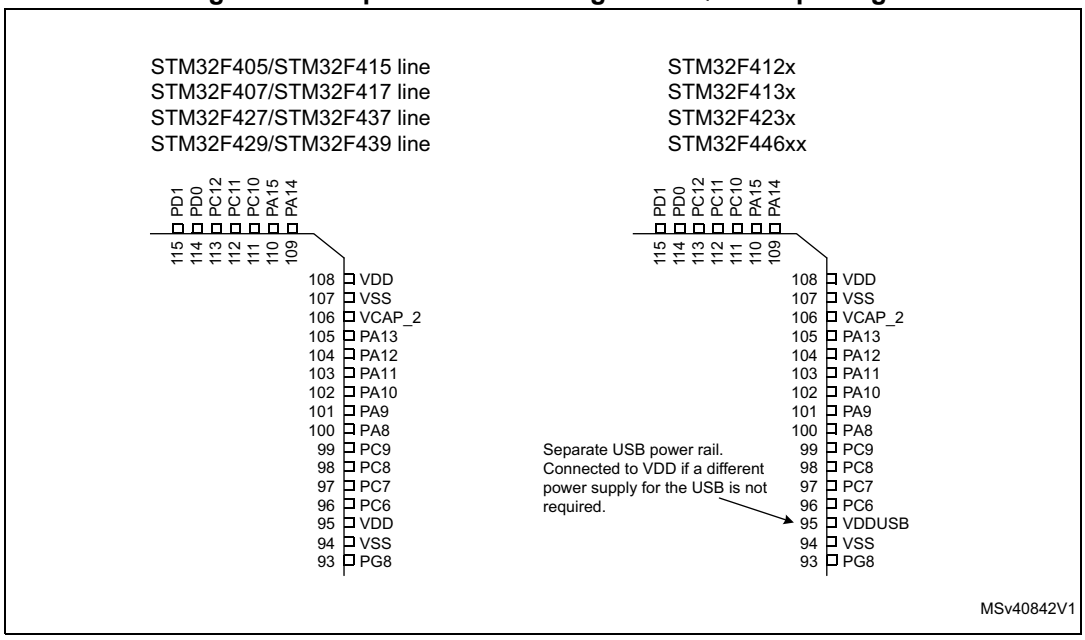


Figure 3. Compatible board design for LQFP144 package



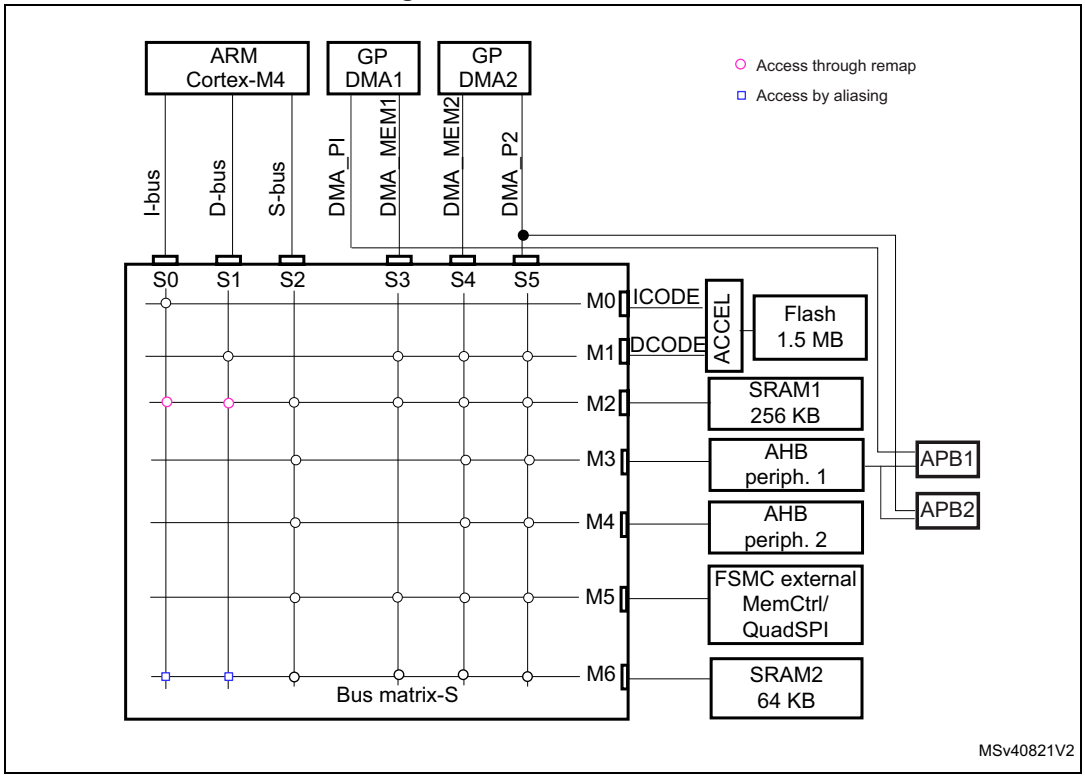
3.7 Embedded SRAM

All devices embed 320 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states.

3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



CPU can access SRAM1 memory via S-bus, when SRAM1 is mapped at the address range: 0x2000 0000 to 0x2003 FFFF.

CPU can access SRAM2 memory via S-bus, when SRAM2 is mapped at the address range: 0x2004 0000 to 0x2004 FFFF.

CPU can access SRAM1 memory via I-bus and D-bus, when SRAM1 is remapped at address 0x0000 0000 either by booting from RAM memory or by the remap mode.

CPU can access SRAM2 memory via I-bus and D-bus, when SRAM2 is mapped at the address range: 0x1000 0000 to 0x1000 FFFF.

Performance boosts up, when the CPU access SRAM memory via the I-bus.

3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
LQFP64	Yes	No	Yes	No
WLCSP81	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		
UFBGA144	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.19 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.20: Low-power modes*).

Table 10. STM32F413xG/H pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	1	B2	A3	1	PE2	I/O	FT	(2)	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, SAI1_MCLK_A, QUADSPI_BK1_IO2, UART10_RX, FSMC_A23, EVENTOUT	-
-	-	NC	2	A1	A2	2	PE3	I/O	FT	(2)	TRACED0, SAI1_SD_B, UART10_TX, FSMC_A19, EVENTOUT	-
-	-	NC	3	B1	B2	3	PE4	I/O	FT	(2)(3)	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, SAI1_SD_A, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	NC	4	C2	B3	4	PE5	I/O	FT	(2)	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	NC	5	D2	B4	5	PE6	I/O	FT	(2)(3)	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, SAI1_FS_A, FSMC_A22, EVENTOUT	-
1	1	B9	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	C8	7	C1	A1	7	PC13-ANTI_TAMP	I/O	FT	(4)(5)	EVENTOUT	TAMP_1
3	3	C9	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(4)(5)(6)	EVENTOUT	OSC32_IN
4	4	D9	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(4)(6)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
18	26	E4	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_IN8
19	27	G5	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_IN9
20	28	H5	37	L6	J5	48	PB2	I/O	FT	-	LPTIM1_OUT, DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	G4	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-
-	-	-	-	-	M6	54	PF14	I/O	FTf	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FTf	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, UART9_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, UART9_TX, FSMC_A11, EVENTOUT	-
-	-	NC	38	M7	M7	58	PE7	I/O	FT	(2)	TIM1_ETR, DFSDM1_DATIN2, UART7_Rx, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
21	29	H3	47	L10	M9	69	PB10	I/O	FTf	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, USART3_TX, I2CFMP4_SCL, DFSDM2_CKOUT, SDIO_D7, EVENTOUT	-
-	-	NC	-	K9	M10	70	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, I2S2_CKIN, USART3_RX, EVENTOUT	-
22	30	H2	48	L11	H7	71	VCAP_1	S	-	-	-	-
23	31	J2	49	F12	-	-	VSS	S	-	-	-	-
24	32	J1	50	G12	G7	72	VDD	S	-	-	-	-
25	33	F3	51	L12	M11	73	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, USART3_CK, CAN2_RX, DFSDM1_DATIN1, UART5_RX, FSMC_D13/FSMC_DA13, EVENTOUT	-
26	34	G2	52	K12	M12	74	PB13	I/O	FT	-	TIM1_CH1N, I2CFMP1_SMBA, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, USART3_CTS, CAN2_TX, DFSDM1_CKIN1, UART5_TX, EVENTOUT	-
27	35	E3	53	K11	L11	75	PB14	I/O	FTf	-	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0/FSMC_DA0, SDIO_D6, EVENTOUT	-

Table 13. STM32F413xG/H register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 0x5006 0BFF	RNG
	0x5004 0000 - 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 4000 - 0X4002 5FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 18: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A=85 °C	T_A=105 °C	T_A=125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	32.9	34.96	35.30	37.21	40.79	mA
			84	26.5	28.13	28.58	30.50	33.96	
			64	18.3	19.44	20.11	21.76	25.03	
			50	14.4	15.28	16.12	17.95	21.11	
			25	7.5	8.10	9.35	11.09	14.38	
			20	6.4	6.99	8.17	9.96	13.17	
		HSI, PLL off, all peripherals enabled(2)(3)	16	4.6	5.17	6.42	8.28	11.46	
			1	0.7	1.28	2.64	4.30	7.66	
		External clock, PLL ON, all peripherals disabled(3)	100	15.4	16.43	17.35	19.17	22.85	
			84	12.4	13.28	14.32	16.12	19.67	
			64	8.7	9.36	10.38	12.06	15.31	
			50	6.9	7.47	8.54	10.36	13.49	
			25	3.7	4.27	5.47	7.17	10.45	
			20	3.2	3.72	5.01	6.67	10.02	
		HSI, PLL off, all peripherals disabled(3)	16	2.3	2.80	4.05	5.90	9.07	
			1	0.6	1.14	2.51	4.16	7.51	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB1	AHB-APB1 bridge	0.90	0.88	0.81	µA/MHz
	TIM2	13.08	12.48	11.16	
	TIM3	9.98	9.50	8.50	
	TIM4	9.88	9.43	8.44	
	TIM5	13.14	12.52	11.19	
	TIM6	1.94	1.86	1.66	
	TIM7	1.86	1.79	1.56	
	TIM12	5.56	5.29	4.72	
	TIM13	3.44	3.29	2.94	
	TIM14	3.66	3.48	3.09	
	LPTIM1	7.34	7.00	6.25	
	WWDG	0.64	0.62	0.53	
	SPI2/I2S2	3.02	2.88	2.56	
	SPI3/I2S3	3.06	2.90	2.59	
	USART2	3.30	3.14	2.81	
	USART3	3.32	3.14	2.81	
	UART4	3.18	3.02	2.69	
	UART5	3.26	3.10	2.75	
	I2C1	3.20	3.05	2.72	
	I2C2	3.30	3.14	2.81	
	I2C3	3.26	3.10	2.78	
	I2CFMP1	5.22	4.98	4.44	
	CAN1	5.58	5.31	4.75	
	CAN2	5.14	4.88	4.38	
	CAN3	5.70	5.43	4.84	
	PWR	0.90	0.86	0.75	
	DAC1	2.14	2.05	1.81	
	UART7	3.08	2.93	2.59	
	UART8	3.10	2.95	2.63	

Figure 27. High-speed external clock source AC timing diagram

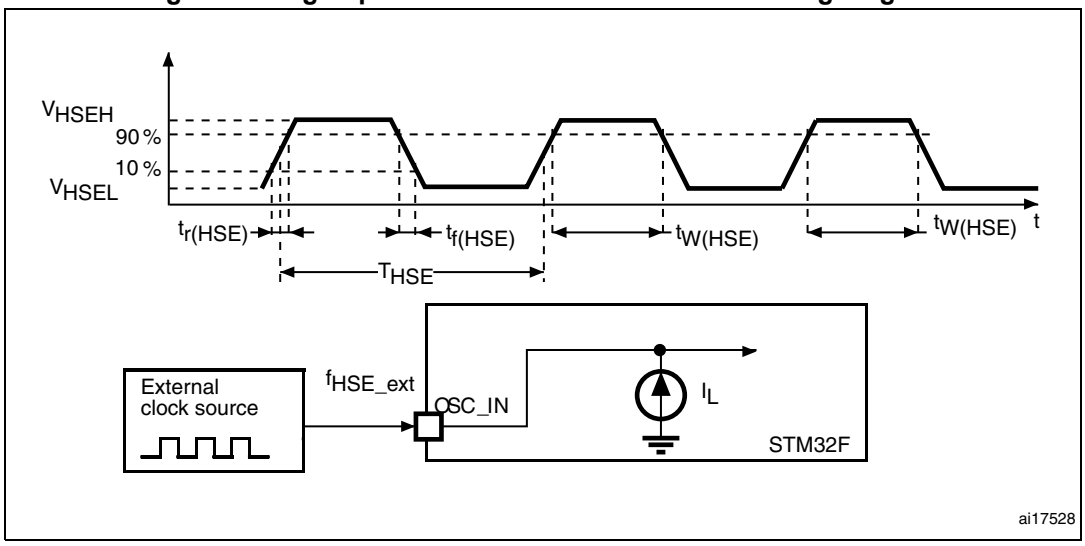
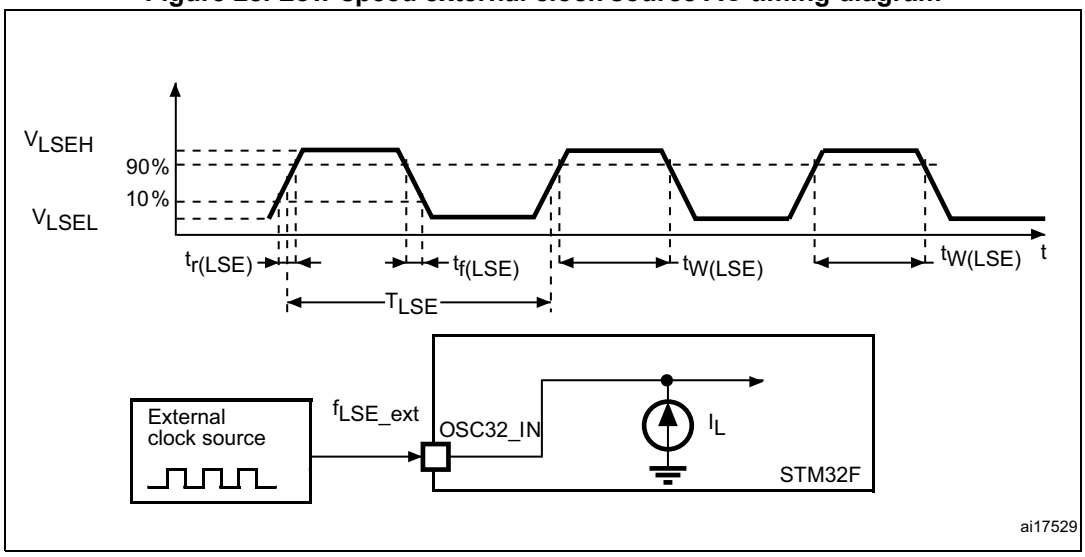


Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 58. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0, PDR_ON, BYPASS_REG	- 0	0	mA
	Injected current on NRST	- 0	NA	
	Injected current on PE6, PC13, PC14, PC15, PF0, PF1, PF2, PC0, PC1, PC2, PC3	- 0	NA	
	Injected current on any other FT and FTf pins	- 5	NA	
	Injected current on any other pins	- 5	+ 5	

1. NA = not applicable.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 59. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa, TC and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.3V_{DD}$(1)	V
	BOOT0 I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	-	-	$0.1V_{DD}$+0.1(2)	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C	-	-		
V_{IH}	FT, TTa, TC and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.7V_{DD}$(1)	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	$0.17V_{DD}$+0.7(2)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C				
V_{HYS}	FT, TTa, TC and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	10% V_{DD}(2)(3)	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	0.1	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C				

6.3.19 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 64*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

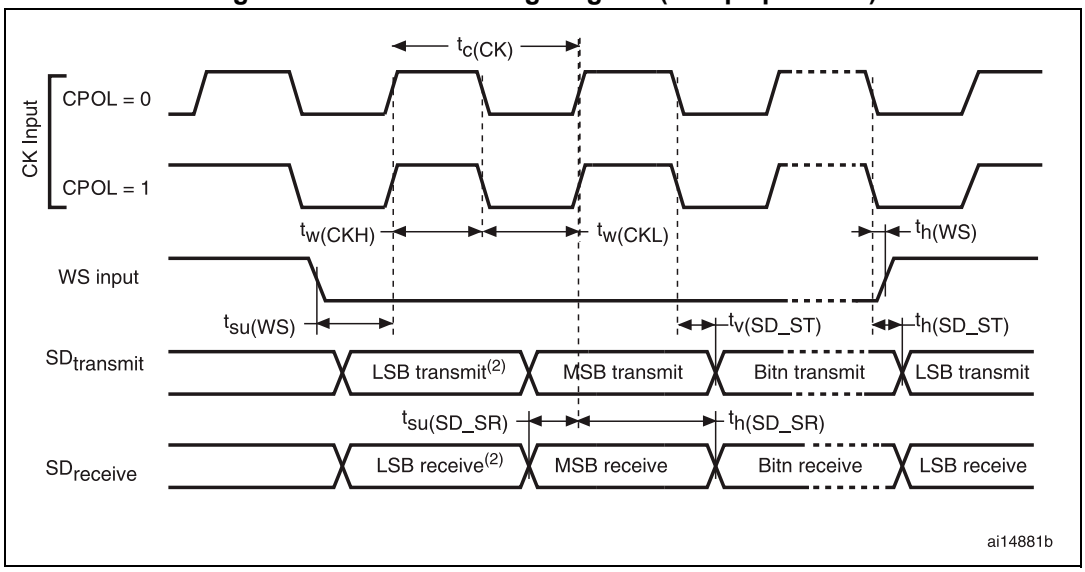
The I^2C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I^2C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

Table 64. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.70	-	1.30	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.60	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	
$t_{v(SDA,ACK)}$	SDA data hold time	-	3.45(3)	-	0.90(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	0.100	-	0.30	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.60	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.70	-	1.3	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	-	-	0.05	0.10(5)	
C_b	Capacitive load for each bus line	-	400	-	400	pF

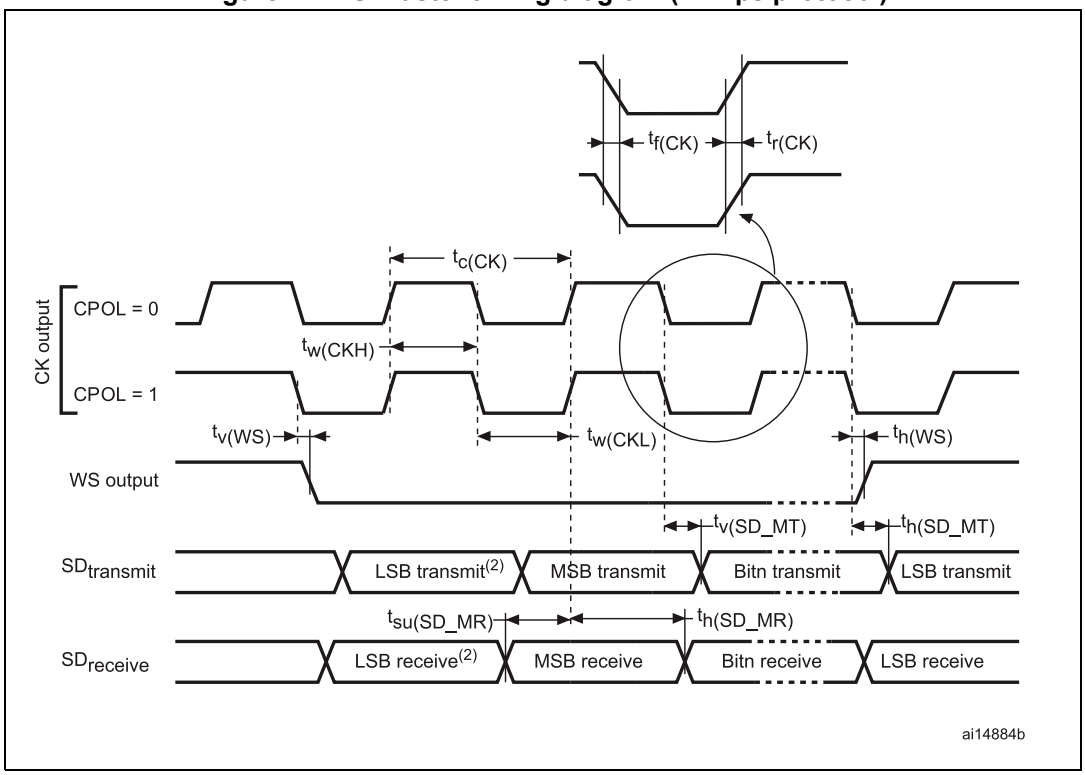
1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max)

Figure 43. I²S slave timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 44. I²S master timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 58. Synchronous multiplexed PSRAM write timings

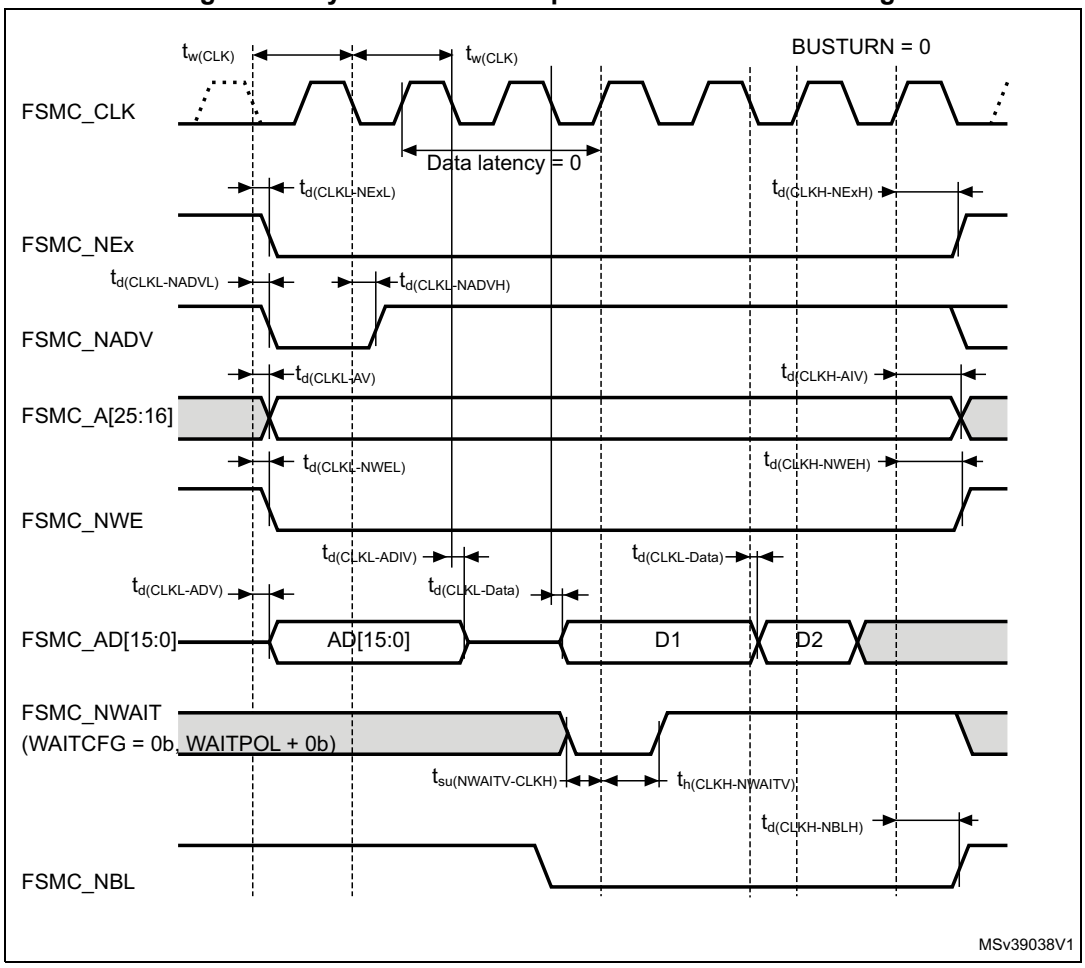


Figure 64. WLCSP81- 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

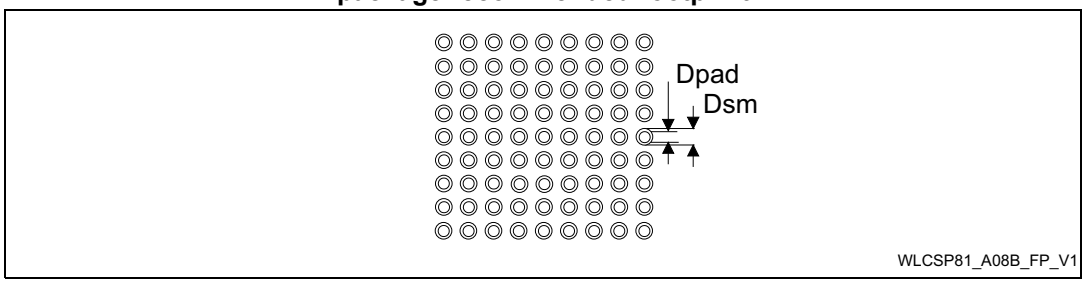


Table 104. WLCSP81 recommended PCB design rules (0.4 mm pitch)

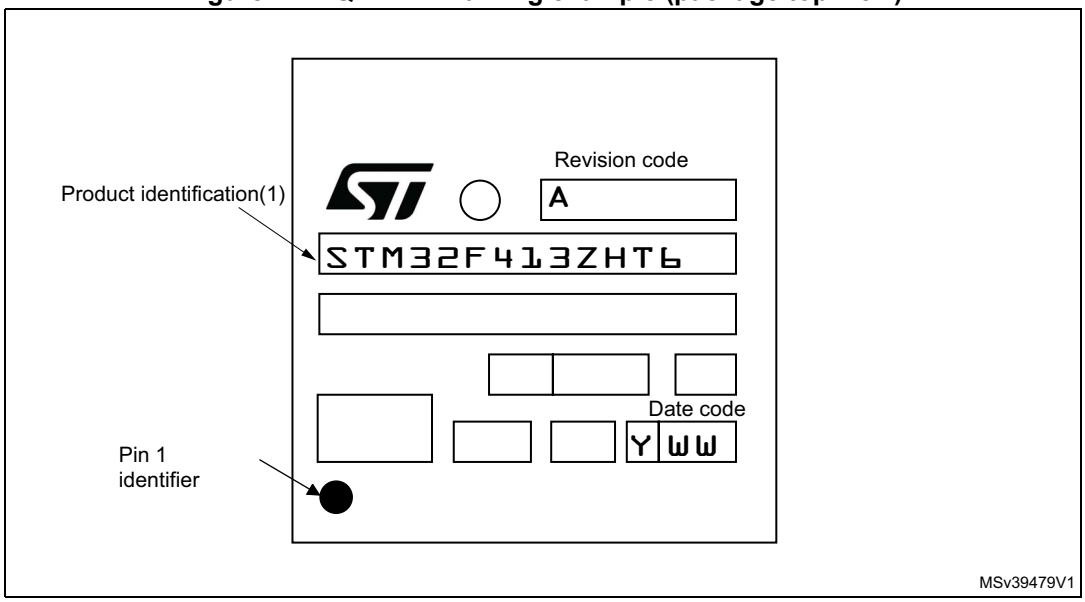
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 77. LQFP144 marking example (package top view)



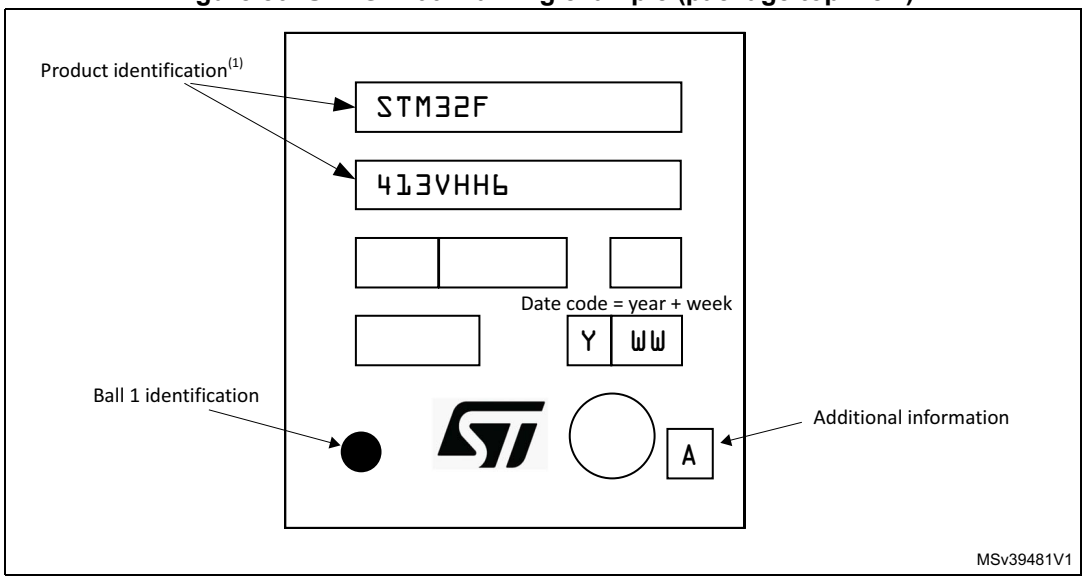
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking for UFBGA100

The following figure gives an example of topside marking and ball 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

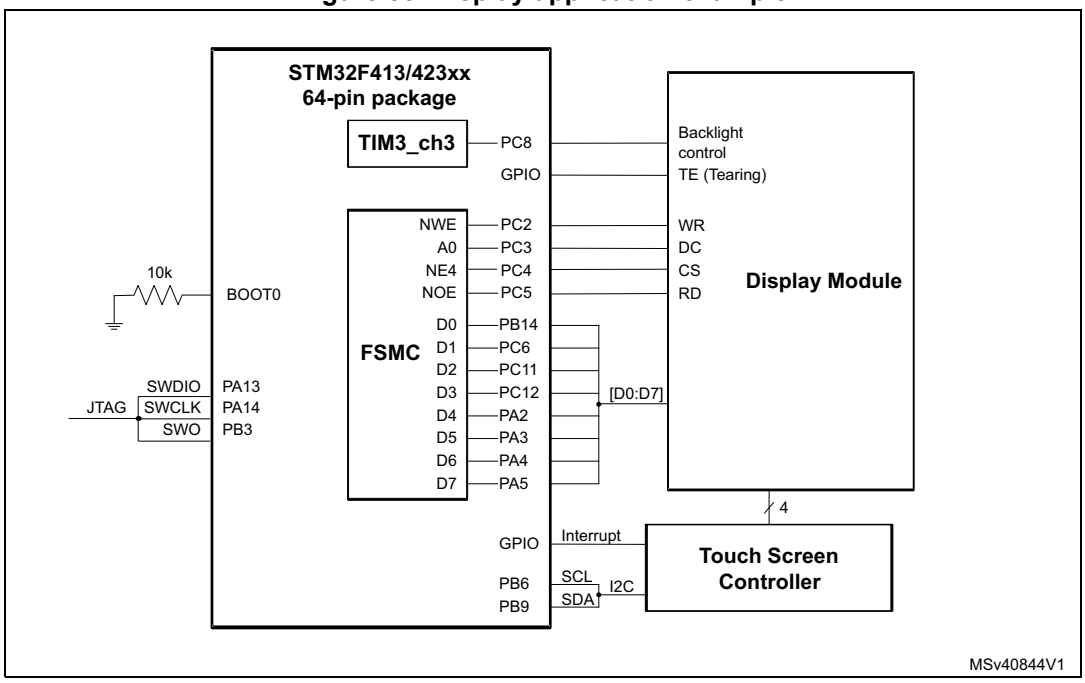
Figure 80. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

B.2 Display application example

Figure 85. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

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