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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413vgt6

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the VBAT pin.

3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.
- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).
- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.21 V_{BAT} operation

The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.22 Timers and watchdogs

The devices embed two advanced-control timer, ten general-purpose timers, two basic timers, one low-power timer, two watchdog timers and a SysTick timer.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control and general-purpose timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen-tary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	50	100
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	50	100

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-
-	-	-	-	-	E4	15	PF5	I/O	FT	-	TIM5_CH3, FSMC_A5, EVENTOUT	-
-	-	D8	10	F2	D2	16	VSS	S	-	-	-	-
-	-	E8	11	G2	D3	17	VDD	S	-	-	-	-
-	-	-	-	-	F3	18	PF6	I/O	FT	-	TRACED0, TIM10_CH1, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT	-
-	-	-	-	-	F2	19	PF7	I/O	FT	-	TRACED1, TIM11_CH1, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	G3	20	PF8	I/O	FT	-	SAI1_SCK_B, UART8_RX, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	G2	21	PF9	I/O	FT	-	SAI1_FS_B, UART8_TX, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	G1	22	PF10	I/O	FT	-	TIM1_ETR, TIM5_CH4, EVENTOUT	-
5	5	E9	12	F1	D1	23	PH0 - OSC_IN	I/O	FT	(6)	EVENTOUT	OSC_IN
6	6	F9	13	G1	E1	24	PH1 - OSC_OUT	I/O	FT	(6)	EVENTOUT	OSC_OUT
7	7	G9	14	H2	F1	25	NRST	I/O	RST	-	-	NRST
-	8	F8	15	H1	H1	26	PC0	I/O	FT	-	LPTIM1_IN1, DFSDM2_CKIN4, SAI1_MCLK_B, EVENTOUT	ADC1_IN10, WKUP2

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	18	H7	27	-	-	38	VSS	S	-	-	-	-
-	-	F6	-	E3	H5	-	BYPASS_ REG	I	FT	-	-	-
-	19	J8	28	-	F4	39	VDD	S	-	-	-	-
14	20	E5	29	M3	J3	40	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6/FSMC_DA6, EVENTOUT	ADC1_IN4, DAC_OUT1
15	21	G6	30	K4	K3	41	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7/FSMC_DA7, EVENTOUT	ADC1_IN5, DAC_OUT2
16	22	F5	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, DFSDM2_CKIN1, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_IN6
17	23	J7	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, DFSDM2_DATIN1, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_IN7
-	24	H6	33	K5	J4	44	PC4	I/O	FT	-	DFSDM2_CKIN2, I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_IN14
-	25	J6	34	L5	K4	45	PC5	I/O	FT	-	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_IN15

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	62	H10	K12	86	PD15	I/O	FTf	(2)	TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-	-	-	-
-	-	F1	-	-	C11	95	VDDUSB	S	-	-	-	-
-	37	D5	63	E12	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT	-
-	38	D4	64	E11	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

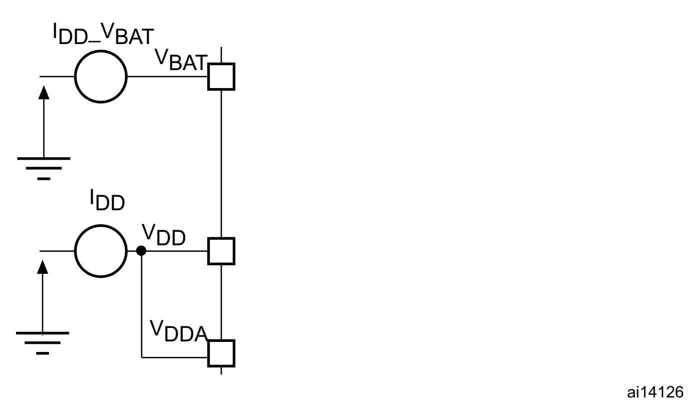
Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, UART10_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, UART10_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FTf	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, UART7_RX, I2C2_SDA, SAI1_SD_A, CAN3_RX, EVENTOUT	-
40	56	B5	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, UART7_TX, I2C3_SDA, SAI1_SCK_A, CAN3_TX, SDIO_D0, EVENTOUT	-

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/LPTIM1	TIM3/4/5	DFSDM2/TIM8/9/10/11	I2C1/2/3/I2CFMP1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/I2S4	SPI2/I2S2/SPI3/I2S3/SPI4/I2S4/SPI5/I2S5/DFSDM1/2	SPI3/I2S3/SAI1/DFSDM2/USART1/USART2/USART3	DFSDM1/USART3/4/5/6/7/8/CAN1	I2C2/I2C3/I2CFMP1/CAN1/2/TIM12/13/14/QUADSPI	SAI1/DFSDM1/DFSDM2/QUADSPI/FSMC/OTG1_FS	UART4/UART5/UART9/UART10/CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CKIN4	-	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATIN4	-	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATIN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CKIN7	-	SPI2_MOSI/ I2S2_SD	-	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM2_CKIN2	-	I2S1_MCK	-	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENTOUT
	PC5	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	-	FSMC_D1/ FSMC_DA1	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	-	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/ FSMC_DA2	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/ FSMC_DA3	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{DD}, V_{DDUSB} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT and TC pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS}–0.3	4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, $V_{DDA,}$ V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	33.3	35.32(3)	35.65	37.65	41.26(3)	mA
			84	26.8	28.45(3)	28.97	30.82	34.39(3)	
			64	18.6	19.74(3)	20.35	22.11	25.35(3)	
			50	14.6	15.57	16.41	18.21	21.46	
			25	7.8	8.37	9.64	11.32	14.68	
			20	6.7	7.25	8.40	10.25	13.45	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	4.6	4.96	6.39	8.20	11.54	
			1	0.8	0.86	2.51	4.34	7.65	
		External clock, PLL ON, all peripherals disabled(2)	100	15.7	16.74(3)	17.62	19.50	23.16(3)	
			84	12.7	13.57(3)	14.60	16.38	19.98(3)	
			64	9.0	9.62(3)	10.60	12.37	15.58(3)	
			50	7.1	7.69	8.79	10.63	13.79	
			25	4.0	4.52	5.68	7.44	10.68	
			20	3.4	4.03	5.23	6.90	10.27	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.3	2.44	4.00	5.81	9.13	
			1	0.6	0.70	2.35	4.18	7.49	

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

Table 28. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max[1]				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled[2][3]	100	36.1	38.48	39.08	40.91	44.59	mA
			84	30.6	32.60	33.14	35.10	38.56	
			64	23.9	25.67	26.27	27.94	31.19	
			50	18.9	20.32	21.04	22.85	26.10	
			25	10.8	11.63	12.75	14.56	17.87	
			20	9.2	9.84	11.06	12.98	16.23	
		HSI, PLL OFF, all peripherals enabled[2][3]	16	7.1	7.69	9.02	10.87	14.25	
			1	1.2	1.84	3.10	4.84	8.20	
		External clock, PLL ON[3] all peripherals disabled	100	18.6	20.33	21.23	23.15	26.71	
			84	16.5	18.09	19.01	20.81	24.29	
			64	14.3	15.76	16.67	18.28	21.50	
			50	11.5	12.57	13.53	15.33	18.49	
			25	7.0	7.67	8.90	10.76	14.05	
			20	6.0	6.68	7.87	9.65	12.96	
		HSI, PLL OFF, all peripherals disabled[3]	16	4.8	5.33	6.66	8.49	11.86	
			1	1.0	1.62	2.95	4.66	8.06	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 39: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
V_{DD} is the MCU supply voltage
f_{SW} is the I/O switching frequency
C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 39. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.89	1.82	1.64	µA/MHz
	GPIOB	1.75	1.68	1.52	
	GPIOC	1.70	1.64	1.48	
	GPIOD	1.72	1.65	1.48	
	GPIOE	1.78	1.71	1.55	
	GPIOF	1.68	1.62	1.45	
	GPIOG	1.66	1.61	1.44	
	GPIOH	0.72	0.69	0.63	
	CRC	0.30	0.30	0.28	
	DMA1(1)	1.75N + 3.14	1.66N + 3.00	1.49N + 2.70	
	DMA2(1)	1.79N + 3.29	1.71N + 3.14	1.53N + 2.82	
AHB2	RNG	0.72	0.70	0.63	µA/MHz
	USB_OTG_FS	19.26	18.37	16.47	
AHB3	FSMC	5.42	5.18	4.64	µA/MHz
	QSPI	10.33	9.86	8.84	

Table 75. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S[2]	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}[2]	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}[2]	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 75*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

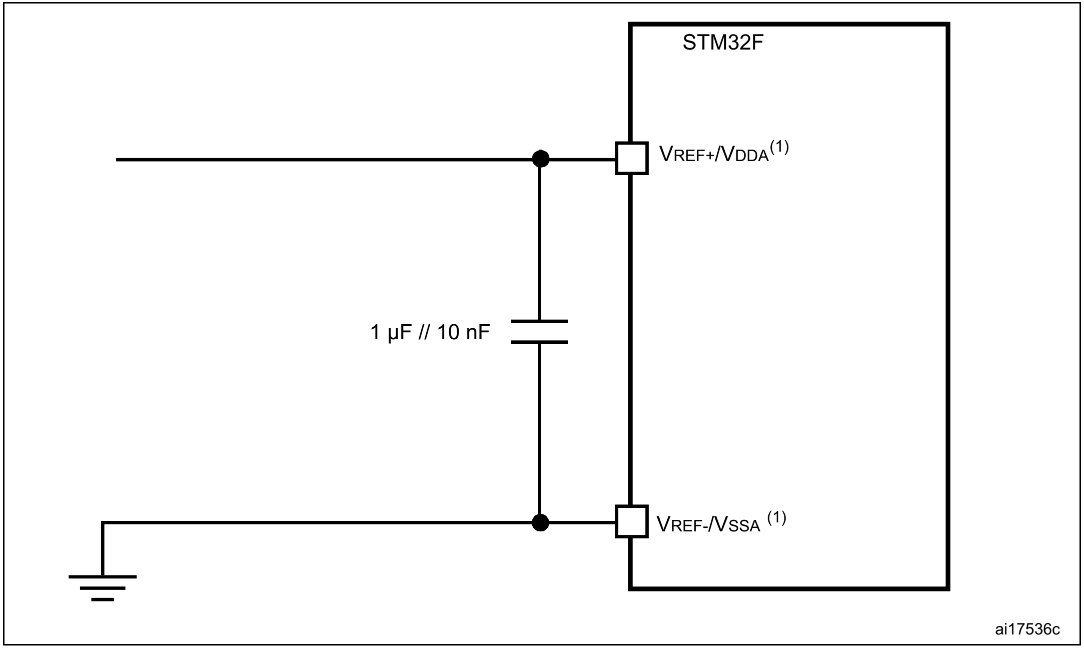
The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 76. ADC accuracy at f_{ADC} = 18 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max[2]	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results.

Figure 51. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 Temperature sensor characteristics

Table 81. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 82. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

6.3.22 V_{BAT} monitoring characteristics

Table 83. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 84* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 84. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +125 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

Table 85. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

6.3.24 DAC electrical characteristics

Table 86. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	-		1.7[(1)]	-	3.6	V	
V_{REF+}	Reference supply voltage	-		1.7[(1)]	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	-		0	-	0	V	-
R_{LOAD}[(2)]	Resistive load	DAC output buffer ON	R_{LOAD} connected to V_{SSA}	5	-	-	kΩ	-
			R_{LOAD} connected to V_{DDA}	25	-	-	kΩ	-
R_O[(2)]	Impedance output with buffer OFF	-		-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}[(2)]	Capacitive load	-		-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min[(2)]	Lower DAC_OUT voltage with buffer ON	-		0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max[(2)]	Higher DAC_OUT voltage with buffer ON	-		-	-	V_{DDA} – 0.2	V	
DAC_OUT min[(2)]	Lower DAC_OUT voltage with buffer OFF	-		-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max[(2)]	Higher DAC_OUT voltage with buffer OFF	-		-	-	V_{REF+} – 1LSB	V	
I_{VREF+}[(4)]	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-		-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}[(4)]	DAC DC VDDA current consumption in quiescent mode[(3)]	-		-	280	380	µA	With no load, middle code (0x800) on the inputs
		-		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Table 86. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
DNL[(4)]	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL[(4)]	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset[(4)]	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error[(4)]	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$[(4)]	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD[(4)]	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate[(2)]	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}[(4)]	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ [(2)]	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

Figure 56. Asynchronous multiplexed PSRAM/NOR write waveforms

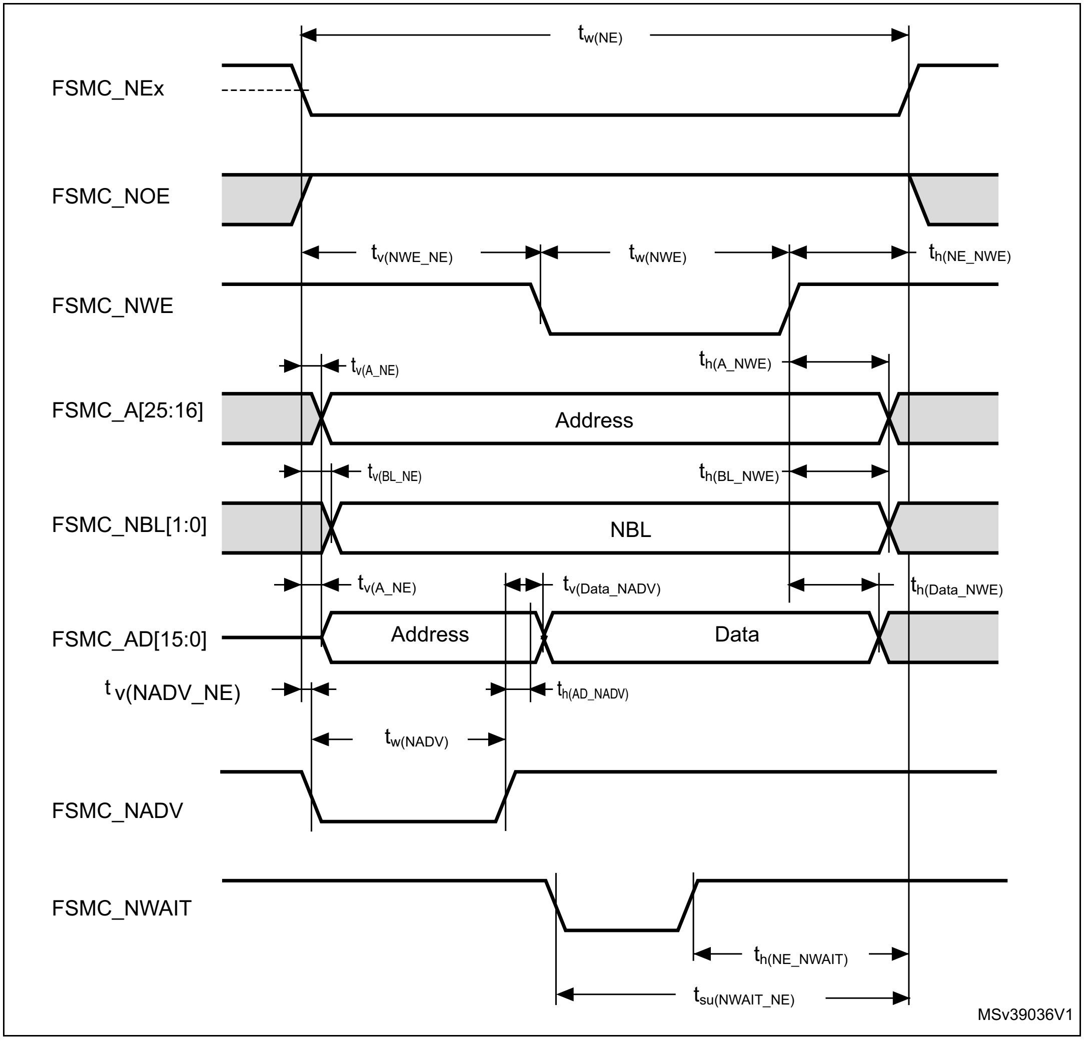


Table 100. SD / MMC characteristics[(1)(2)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	1	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	12	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	10.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	1	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	2	3	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	1	-	-	

1. Guaranteed by characterization results.
2. V_{DD} = 2.7 to 3.6 V.

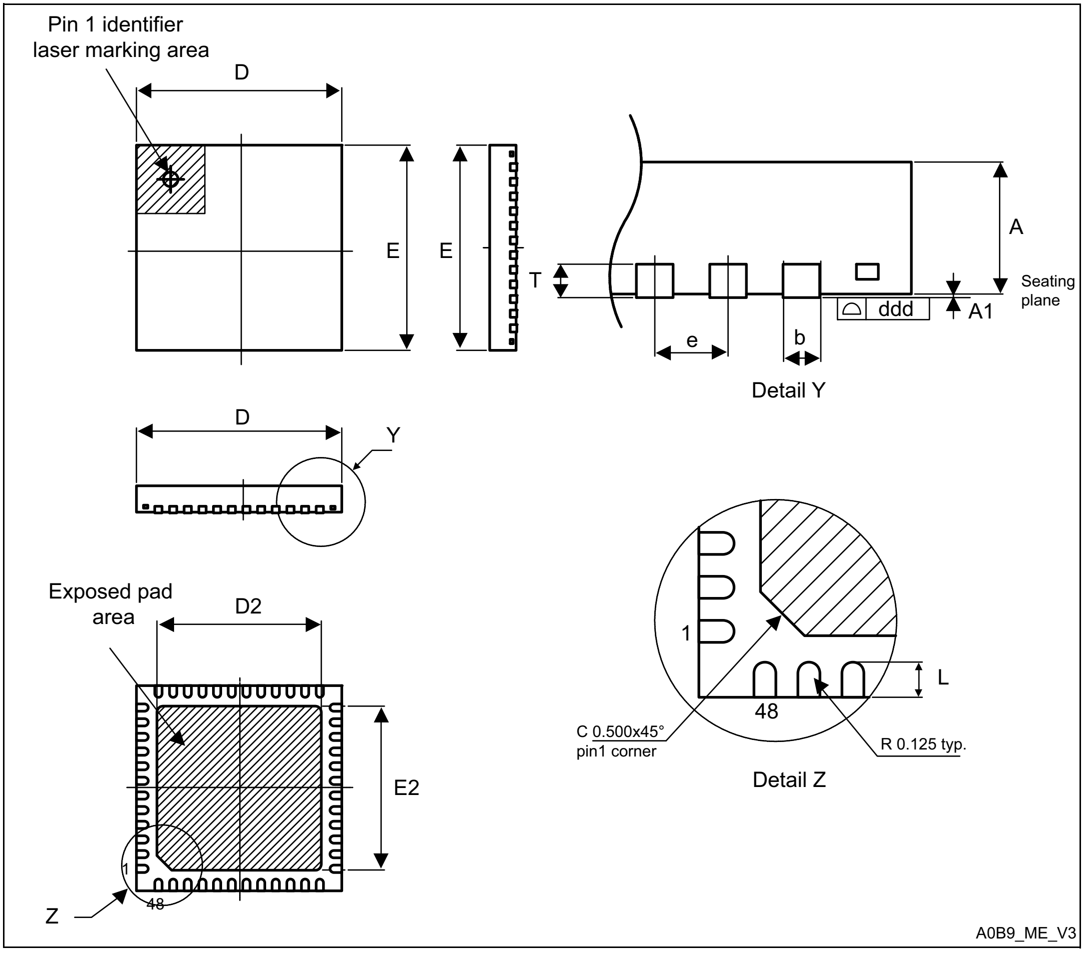
Table 101. eMMC characteristics V_{DD} = 1.7 V to 1.9 V[(1)(2)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	15	15.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	13	-	-	

1. Guaranteed by characterization results.
2. C_{LOAD} = 20 pF.

7.2 UFQFPN48 package information

Figure 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.