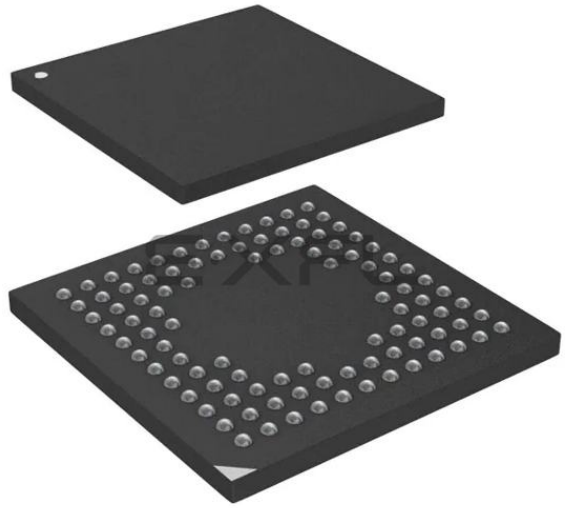


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413vhh6

2.1 Compatibility with STM32F4 series

The STM32F413xG/H are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F413xG/H can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

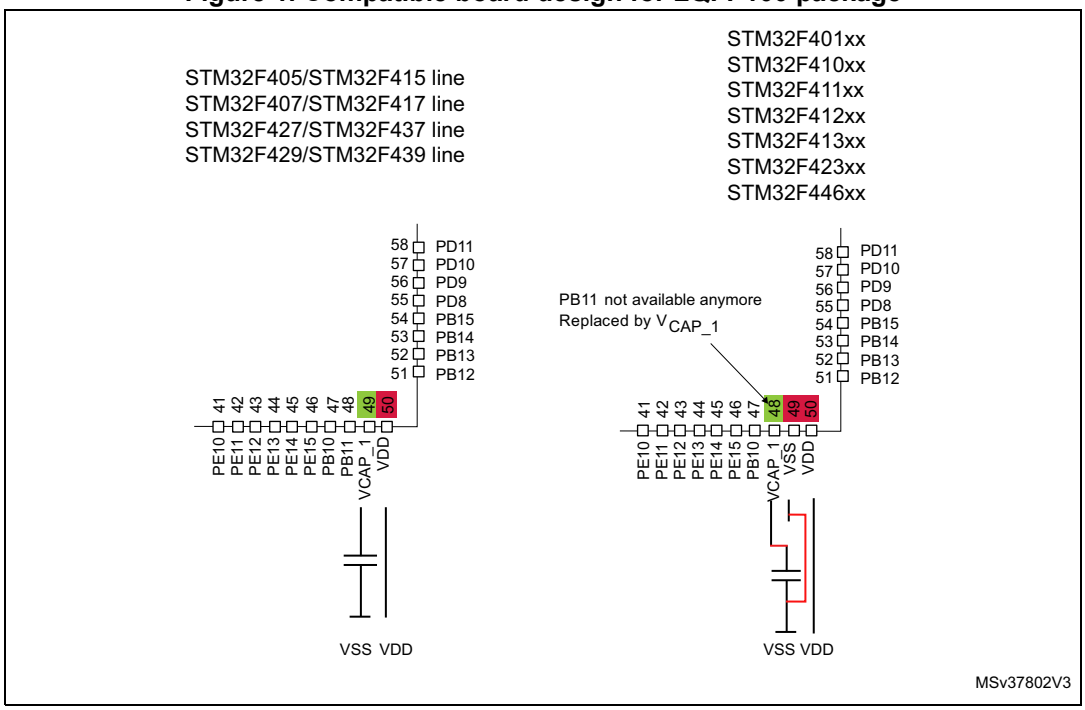
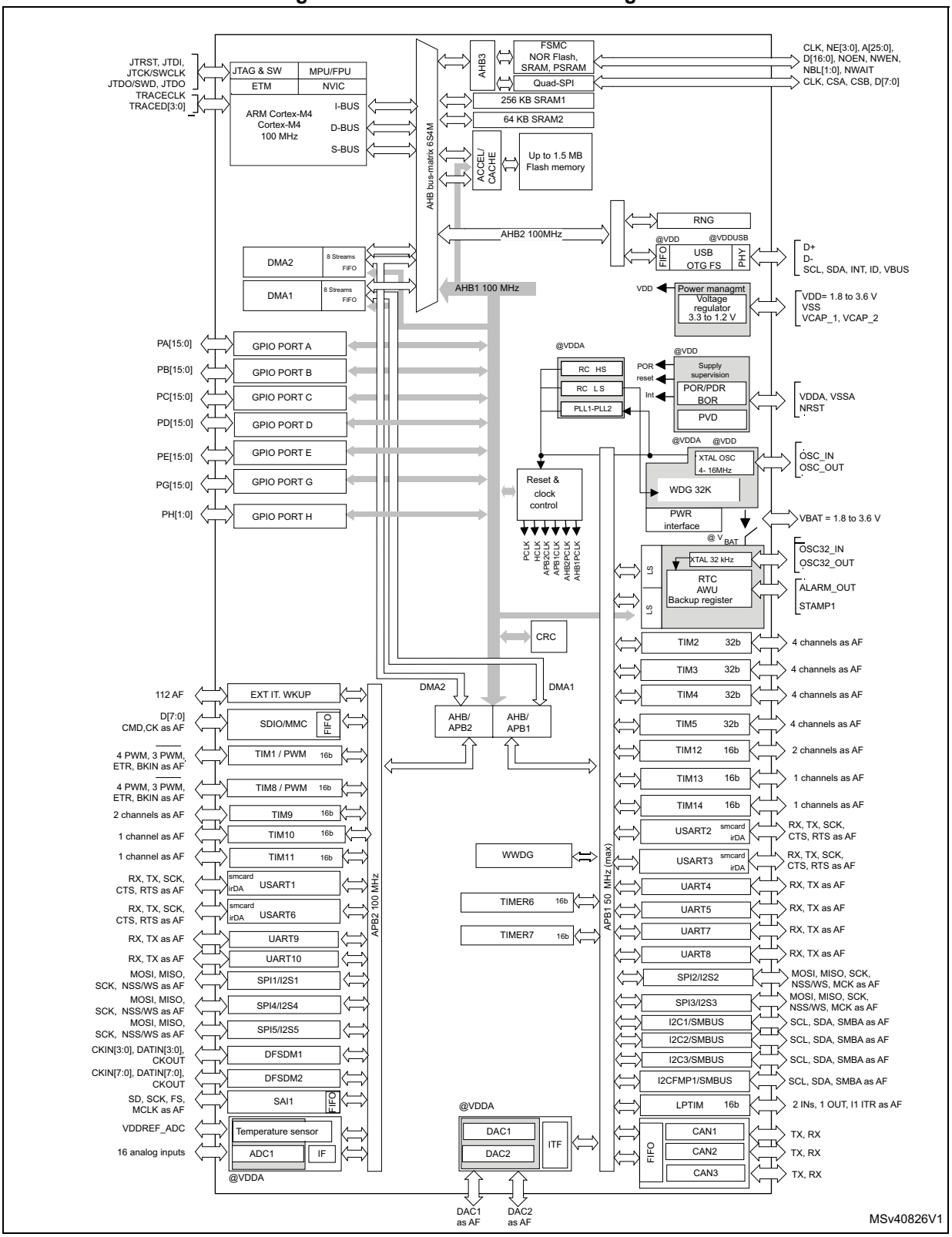


Figure 4. STM32F413xG/H block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

The strong benefits of such mechanism coupled with DFSDM are:

- Possibility to place the digital microphones close to each other
- No need for external delay lines
- The delay tuning is done in hardware, preventing the use of MIPs crunching algorithms
- Possibility to change the delay tuning on the fly
- The low power consumption and CPU time released due to the DFSDM hardware PDM to PCM conversion

The impacted audio application are beam forming and sound source localization

3.31 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.32 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2, and 512 bytes for CAN3.

3.33 Universal serial bus on-the-go full-speed (USB_OTG_FS)

The devices embed a USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with USB 2.0 and OTG 1.0 specifications. It features software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock, which is generated by a PLL connected to the HSE oscillator. The Battery Charging Detection (BCD) can detect and identify the type of port it is connected to (standard USB or charger). The charging type can also be detected: Dedicated Charging Port (DCP), Charging Downstream Port (CDP) and Standard Downstream Port (SDP).

Some packages provide a dedicated USB power rail allowing to supply the USB from a different voltage that the rest of the device. As an example, the device can be powered with the minimum specified supply voltage while the USB runs at the level defined by the standard.

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	18	H7	27	-	-	38	VSS	S	-	-	-	-
-	-	F6	-	E3	H5	-	BYPASS_ REG	I	FT	-	-	-
-	19	J8	28	-	F4	39	VDD	S	-	-	-	-
14	20	E5	29	M3	J3	40	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6/FSMC_DA6, EVENTOUT	ADC1_IN4, DAC_OUT1
15	21	G6	30	K4	K3	41	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7/FSMC_DA7, EVENTOUT	ADC1_IN5, DAC_OUT2
16	22	F5	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, DFSDM2_CKIN1, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_IN6
17	23	J7	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, DFSDM2_DATIN1, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_IN7
-	24	H6	33	K5	J4	44	PC4	I/O	FT	-	DFSDM2_CKIN2, I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_IN14
-	25	J6	34	L5	K4	45	PC5	I/O	FT	-	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_IN15

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	62	H10	K12	86	PD15	I/O	FTf	(2)	TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-	-	-	-
-	-	F1	-	-	C11	95	VDDUSB	S	-	-	-	-
-	37	D5	63	E12	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT	-
-	38	D4	64	E11	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CKIN4	-	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATIN4	-	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATIN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CKIN7	-	SPI2_MOSI/ I2S2_SD	-	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM2_CKIN2	-	I2S1_MCK	-	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENTOUT
	PC5	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	-	FSMC_D1/ FSMC_DA1	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	-	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/ FSMC_DA2	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/ FSMC_DA3	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_ AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_ AF
PortH	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 18: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A=85 °C	T_A=105 °C	T_A=125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	32.9	34.96	35.30	37.21	40.79	mA
			84	26.5	28.13	28.58	30.50	33.96	
			64	18.3	19.44	20.11	21.76	25.03	
			50	14.4	15.28	16.12	17.95	21.11	
			25	7.5	8.10	9.35	11.09	14.38	
			20	6.4	6.99	8.17	9.96	13.17	
		HSI, PLL off, all peripherals enabled(2)(3)	16	4.6	5.17	6.42	8.28	11.46	
			1	0.7	1.28	2.64	4.30	7.66	
		External clock, PLL ON, all peripherals disabled(3)	100	15.4	16.43	17.35	19.17	22.85	
			84	12.4	13.28	14.32	16.12	19.67	
			64	8.7	9.36	10.38	12.06	15.31	
			50	6.9	7.47	8.54	10.36	13.49	
			25	3.7	4.27	5.47	7.17	10.45	
			20	3.2	3.72	5.01	6.67	10.02	
		HSI, PLL off, all peripherals disabled(3)	16	2.3	2.80	4.05	5.90	9.07	
			1	0.6	1.14	2.51	4.16	7.51	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 39: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 39. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.89	1.82	1.64	µA/MHz
	GPIOB	1.75	1.68	1.52	
	GPIOC	1.70	1.64	1.48	
	GPIOD	1.72	1.65	1.48	
	GPIOE	1.78	1.71	1.55	
	GPIOF	1.68	1.62	1.45	
	GPIOG	1.66	1.61	1.44	
	GPIOH	0.72	0.69	0.63	
	CRC	0.30	0.30	0.28	
	DMA1(1)	1.75N + 3.14	1.66N + 3.00	1.49N + 2.70	
	DMA2(1)	1.79N + 3.29	1.71N + 3.14	1.53N + 2.82	
AHB2	RNG	0.72	0.70	0.63	µA/MHz
	USB_OTG_FS	19.26	18.37	16.47	
AHB3	FSMC	5.42	5.18	4.64	µA/MHz
	QSPI	10.33	9.86	8.84	

6.3.9 Internal clock source characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

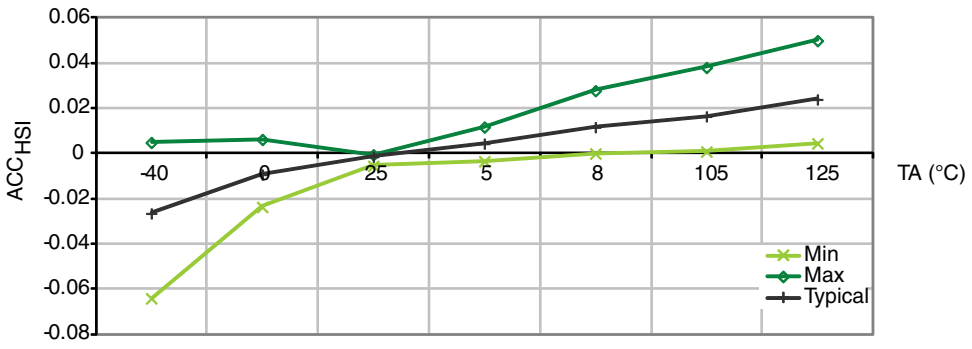
High-speed internal (HSI) RC oscillator

Table 45. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = – 40 to 125 °C(3)	–8	-	6.75	%
		T_A = – 40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design
3. Based on characterization
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization results.

Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

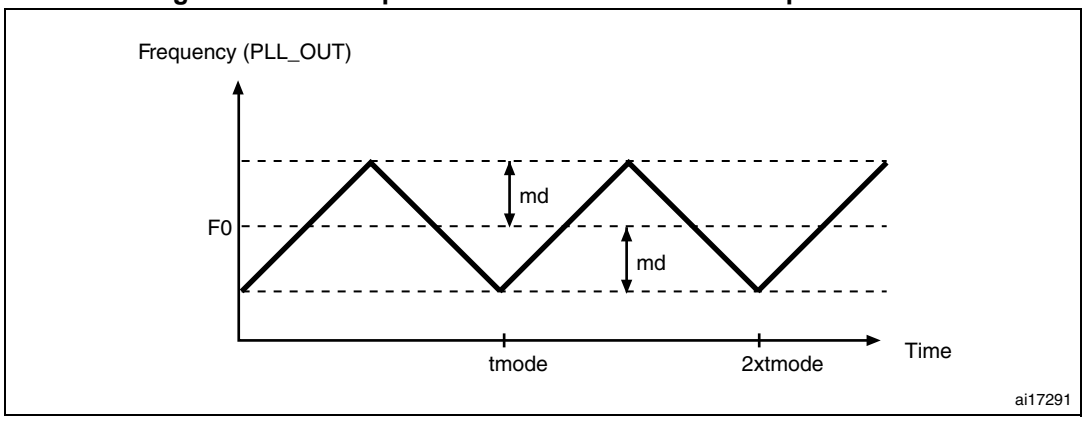
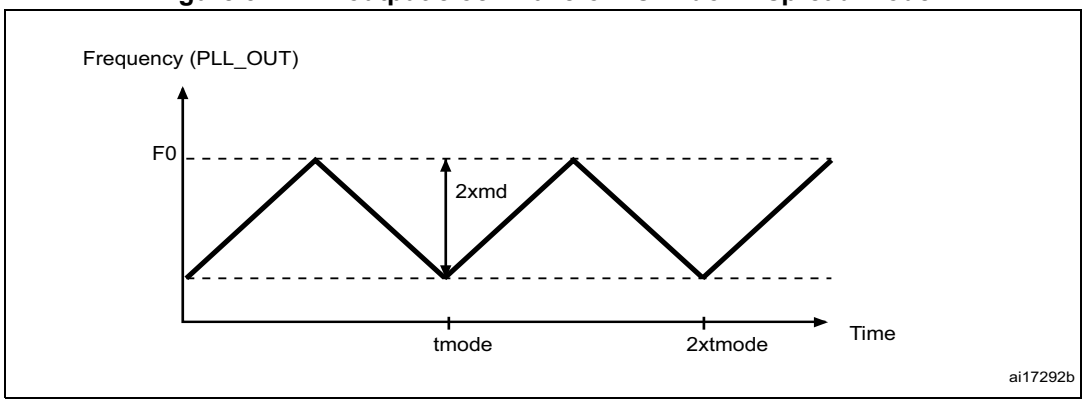


Figure 34. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 50. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 77. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, V_{DDA} –V_{REF} < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results.

Table 78. ADC accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results.

Table 79. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization results.

Table 80. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

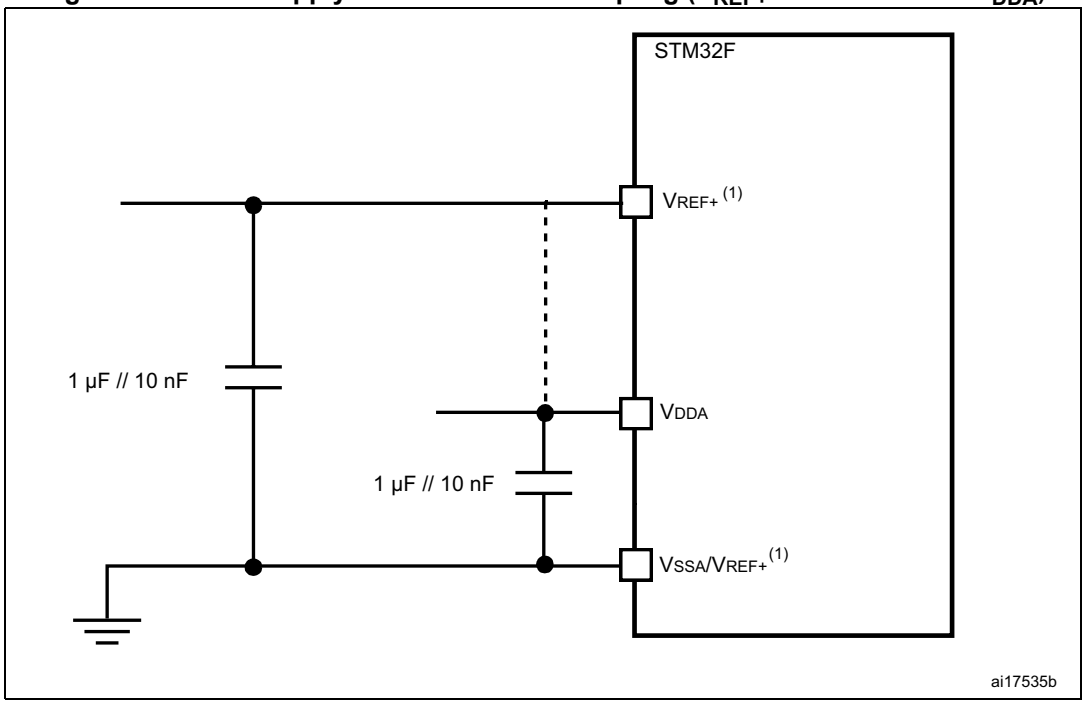
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization results.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 50* or *Figure 51*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 50. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3 * t_{HCLK} - 1$	$3 * t_{HCLK} + 1$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2 * t_{HCLK}$	$2 * t_{HCLK} + 0.5$	
$t_{w(NOE)}$	FSMC_NOE low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	0.5	
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1$	
$t_{h(AD\_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high)	$t_{HCLK} + 0.5$	-	
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	$t_{HCLK} - 0.5$	-	
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$t_{HCLK} - 2$	-	
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$t_{HCLK} - 2$	-	
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	

1. C_L = 30 pF.
2. Based on characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8 * t_{HCLK} - 1$	$8 * t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5 * t_{HCLK} - 1.5$	$5 * t_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5 * t_{HCLK} + 1.5$	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 1$	-	

1. C_L = 30 pF.
2. Based on characterization.

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FSMC_CLK = 90 MHz).

Figure 57. Synchronous multiplexed NOR/PSRAM read timings

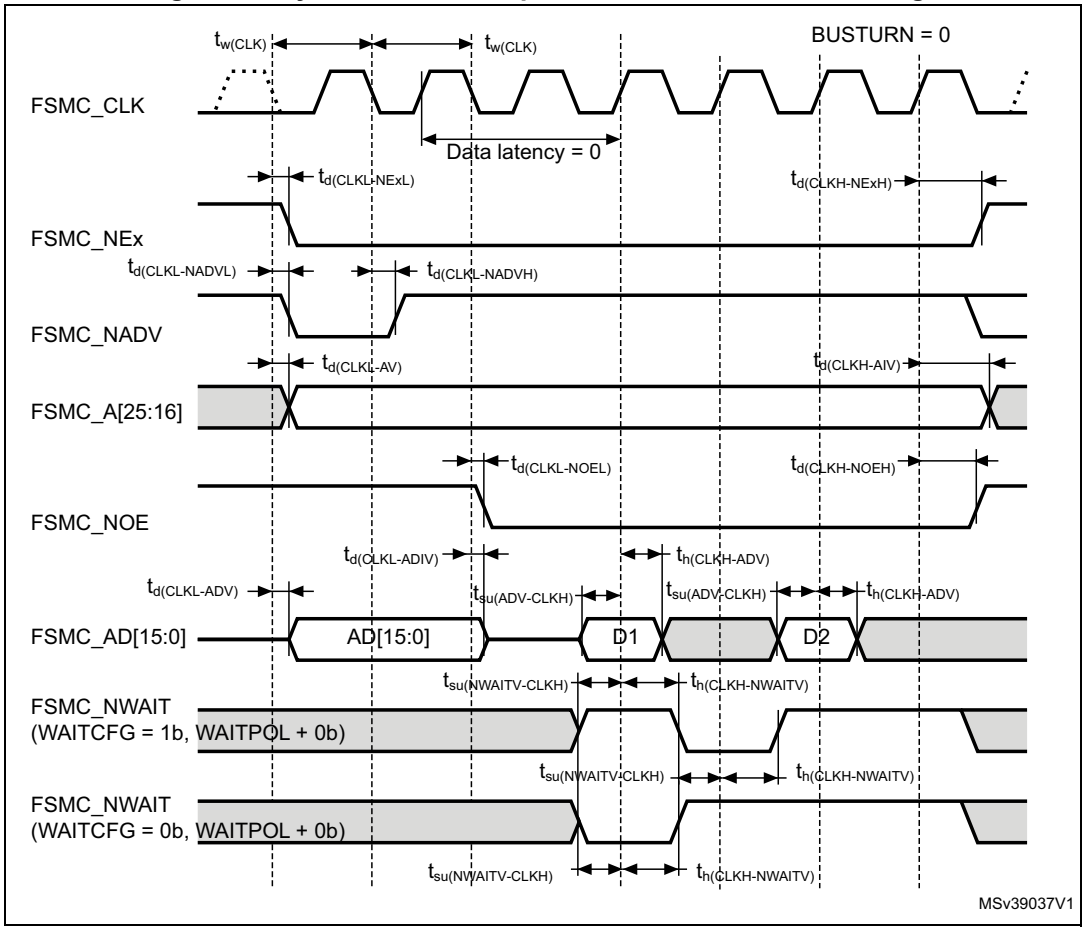
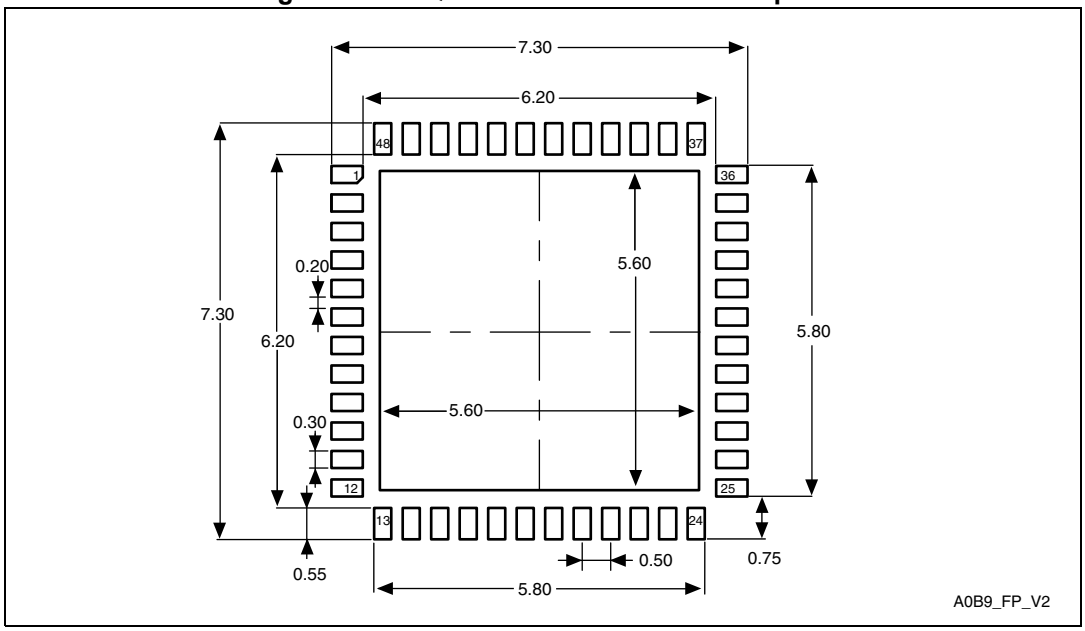


Table 105. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

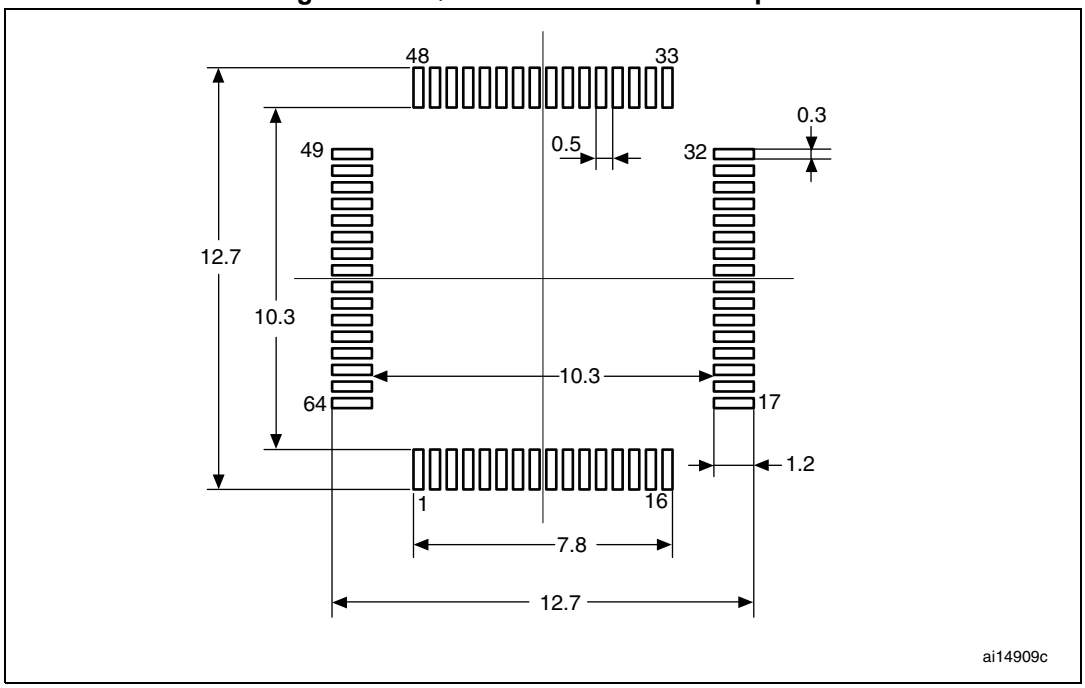
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

Figure 70. LQFP64 recommended footprint



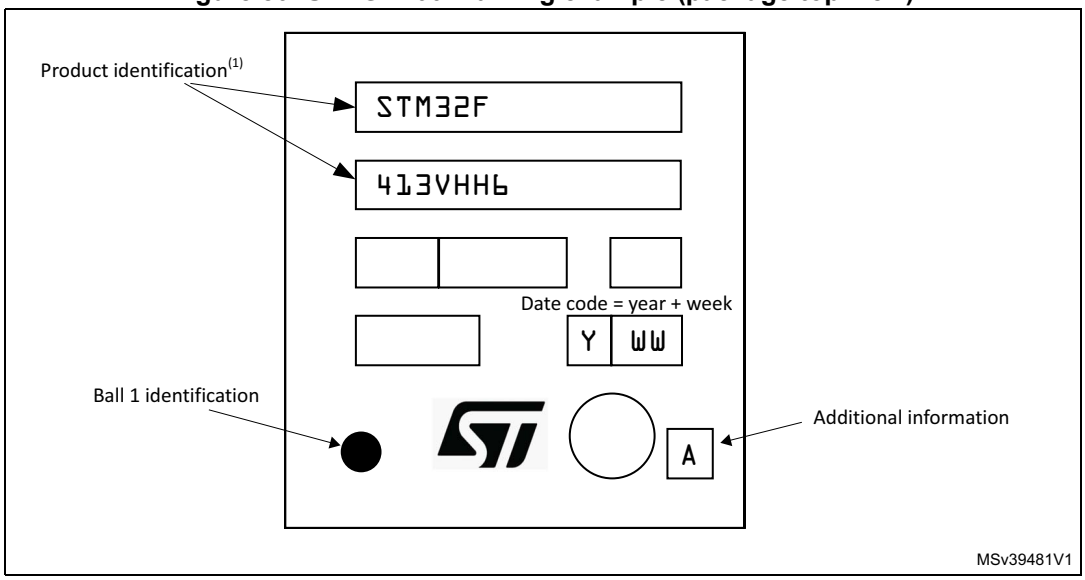
1. Dimensions are in millimeters.

Device marking for UFBGA100

The following figure gives an example of topside marking and ball 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 80. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.