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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413vht6

3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
LQFP64	Yes	No	Yes	No
WLCSP81	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		
UFBGA144	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.19 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.20: Low-power modes*).

The main USB OTG FS features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Support of session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed when bus-powered devices are connected
- Link Power Management (LPM)
- Battery Charging Detection (BCD) supporting DCP, CDP and SDP

3.34 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.35 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.36 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

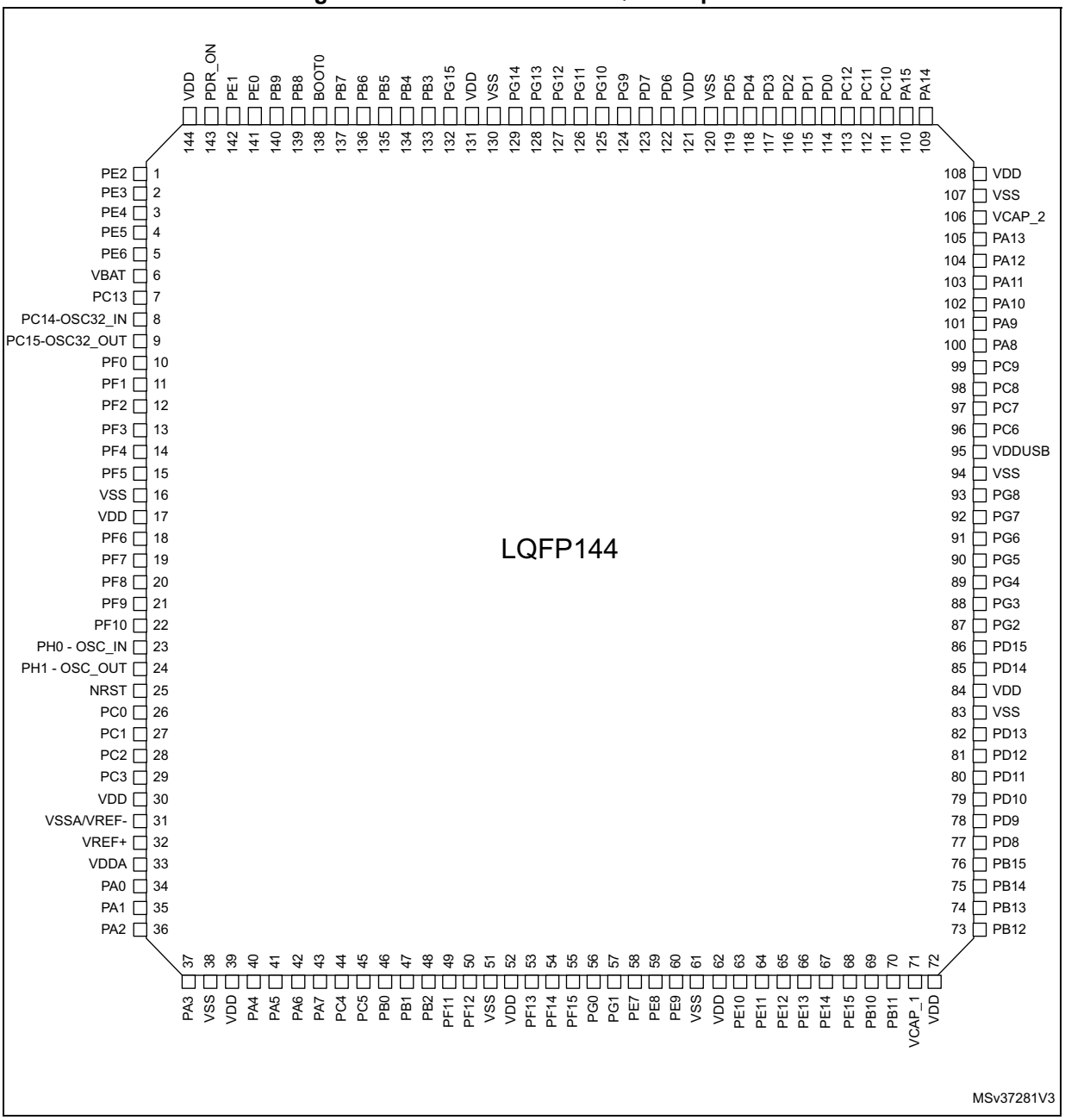
3.37 Digital to analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This digital interface supports the following features:

- Two DAC output channels

Figure 15. STM32F413xG/H LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F413xG/H pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	1	B2	A3	1	PE2	I/O	FT	(2)	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, SAI1_MCLK_A, QUADSPI_BK1_IO2, UART10_RX, FSMC_A23, EVENTOUT	-
-	-	NC	2	A1	A2	2	PE3	I/O	FT	(2)	TRACED0, SAI1_SD_B, UART10_TX, FSMC_A19, EVENTOUT	-
-	-	NC	3	B1	B2	3	PE4	I/O	FT	(2)(3)	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, SAI1_SD_A, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	NC	4	C2	B3	4	PE5	I/O	FT	(2)	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	NC	5	D2	B4	5	PE6	I/O	FT	(2)(3)	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, SAI1_FS_A, FSMC_A22, EVENTOUT	-
1	1	B9	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	C8	7	C1	A1	7	PC13-ANTI_TAMP	I/O	FT	(4)(5)	EVENTOUT	TAMP_1
3	3	C9	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(4)(5)(6)	EVENTOUT	OSC32_IN
4	4	D9	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(4)(6)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
28	36	H1	54	K10	L12	76	PB15	I/O	FTf	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	NC	55	-	L9	77	PD8	I/O	FT	(2)	USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT	-
-	-	F2	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	G1	57	J12	J9	79	PD10	I/O	FT	(7)	USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	NC	58	J11	H9	80	PD11	I/O	FT	(2)	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	NC	59	J10	L10	81	PD12	I/O	FTf	(2)	TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	NC	60	H12	K10	82	PD13	I/O	FTf	(2)	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	NC	61	H11	K11	85	PD14	I/O	FTf	(2)	TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	62	H10	K12	86	PD15	I/O	FTf	(2)	TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-	-	-	-
-	-	F1	-	-	C11	95	VDDUSB	S	-	-	-	-
-	37	D5	63	E12	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT	-
-	38	D4	64	E11	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, UART10_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, UART10_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FTf	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, UART7_RX, I2C2_SDA, SAI1_SD_A, CAN3_RX, EVENTOUT	-
40	56	B5	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, UART7_TX, I2C3_SDA, SAI1_SCK_A, CAN3_TX, SDIO_D0, EVENTOUT	-

Table 11. FSMC pin definition (continued)

Pins	FSMC		64 pins	81 pins	100 pins	144 pins
	LCD/NOR/ PSRAM/SRAM	NOR/PSRAM Mux				
PA3	D5	DA5	Yes	Yes	Yes	Yes
PA4	D6	DA6	Yes	Yes	Yes	Yes
PA5	D7	DA7	Yes	Yes	Yes	Yes
PC4	NE4	NE4	Yes	Yes	Yes	Yes
PC5	NOE	NOE	Yes	Yes	Yes	Yes
PF12	A6	-	-	-	-	Yes
PF13	A7	-	-	-	-	Yes
PF14	A8	-	-	-	-	Yes
PF15	A9	-	-	-	-	Yes
PG0	A10	-	-	-	-	Yes
PG1	A11	-	-	-	-	Yes
PE7	D4	DA4	-	-	Yes	Yes
PE8	D5	DA5	-	-	Yes	Yes
PE9	D6	DA6	-	Yes	Yes	Yes
PE10	D7	DA7	-	Yes	Yes	Yes
PE11	D8	DA8	-	Yes	Yes	Yes
PE12	D9	DA9	-	Yes	Yes	Yes
PE13	D10	DA10	-	Yes	Yes	Yes
PE14	D11	DA11	-	Yes	Yes	Yes
PE15	D12	DA12	-	Yes	Yes	Yes
PB12	D13	DA13	Yes	Yes	Yes	Yes
PB14	D0	DA0	Yes	Yes	Yes	Yes
PD8	D13	DA13	-	-	-	Yes
PD9	D14	DA14	-	Yes	Yes	Yes
PD10	D15	DA15	-	Yes	Yes	Yes
PD11	A16	A16	-	-	Yes	Yes
PD12	A17	A17	-	-	Yes	Yes
PD13	A18	A18	-	-	Yes	Yes
PD14	D0	DA0	-	-	Yes	Yes
PD15	D1	DA1	-	-	Yes	Yes
PG2	A12	-	-	-	-	Yes
PG3	A13	-	-	-	-	Yes
PG4	A14	-	-	-	-	Yes

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CKIN4	-	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATIN4	-	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATIN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CKIN7	-	SPI2_MOSI/ I2S2_SD	-	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM2_CKIN2	-	I2S1_MCK	-	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENTOUT
	PC5	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	-	FSMC_D1/ FSMC_DA1	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	-	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/ FSMC_DA2	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/ FSMC_DA3	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_ AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_ AF
PortH	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	33.3	35.32(3)	35.65	37.65	41.26(3)	mA
			84	26.8	28.45(3)	28.97	30.82	34.39(3)	
			64	18.6	19.74(3)	20.35	22.11	25.35(3)	
			50	14.6	15.57	16.41	18.21	21.46	
			25	7.8	8.37	9.64	11.32	14.68	
			20	6.7	7.25	8.40	10.25	13.45	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	4.6	4.96	6.39	8.20	11.54	
			1	0.8	0.86	2.51	4.34	7.65	
		External clock, PLL ON, all peripherals disabled(2)	100	15.7	16.74(3)	17.62	19.50	23.16(3)	
			84	12.7	13.57(3)	14.60	16.38	19.98(3)	
			64	9.0	9.62(3)	10.60	12.37	15.58(3)	
			50	7.1	7.69	8.79	10.63	13.79	
			25	4.0	4.52	5.68	7.44	10.68	
			20	3.4	4.03	5.23	6.90	10.27	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.3	2.44	4.00	5.81	9.13	
			1	0.6	0.70	2.35	4.18	7.49	

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	30.2	32.03	32.71	34.69	38.46	mA
			84	24.3	25.77	26.58	28.47	32.16	
			64	16.8	17.80	18.66	20.53	23.85	
			50	13.2	14.05	15.12	16.85	20.27	
			25	7.1	7.62	8.92	10.81	14.11	
			20	6.1	6.69	7.95	9.72	13.09	
		HSI, PLL OFF, all peripherals enabled(2)	16	4.4	4.99	6.28	8.18	11.45	
			1	0.9	1.50	2.88	4.58	8.00	
		External clock, PLL ON(4) all peripherals disabled(2)	100	12.6	13.46	14.75	16.68	20.54	
			84	10.2	10.90	12.25	14.10	17.84	
			64	7.2	7.70	8.95	10.81	14.14	
			50	5.7	6.26	7.56	9.26	12.72	
			25	3.2	3.77	5.11	6.82	10.26	
			20	2.9	3.41	4.79	6.49	9.92	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.1	2.63	3.91	5.80	9.06	
			1	0.8	1.34	2.72	4.42	7.86	

1. Guaranteed by characterization results..
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	30.7	32.85(4)	33.30	35.37	39.08	mA
			84	24.7	26.48	27.15	28.94	32.65	
			64	17.2	18.36	19.14	20.88	24.29	
			50	13.6	14.54	15.45	17.27	20.58	
			25	7.4	7.97	9.23	11.05	14.42	
			20	6.4	6.99	8.18	10.03	13.32	
		HSI, PLL OFF, all peripherals enabled(3)	16	4.5	5.04	6.32	8.23	11.50	
			1	1.0	1.50	2.89	4.59	8.01	
		External clock, PLL ON(2) all peripherals disabled(3)	100	13.1	14.36	15.33	17.25	20.98	
			84	10.7	11.67	12.73	14.56	18.21	
			64	7.5	8.23	9.40	11.13	14.52	
			50	6.1	6.74	7.89	9.61	12.98	
			25	3.5	4.19	5.37	7.08	10.48	
			20	3.2	3.71	5.02	6.72	10.15	
		HSI, PLL OFF, all peripherals disabled(3)	16	2.1	2.67	3.95	5.84	9.10	
			1	0.8	1.35	2.72	4.43	7.87	

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. Tested in production.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 33. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions	Parameter	Typ(1)	Max(1)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	111.7	157.9	713.7	1323.5	2315.1	µA
		Low power regulator usage	42.3	80.1	594.1	1167.6	2097.6	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	77.9	113.1	568.3	1073.6	1883.7	
		Low power regulator usage	19.7	55.8	561.3	1123.2	2026.0	
		Low power low voltage regulator usage	15.3	46.3	490.8	991.3	1793.9	

1. Guaranteed by characterization results.

Table 34. Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V

Symbol	Conditions	Parameter	Typ	Max(1)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	114.4	161.6(2)	723.0	1339.0	2342.7(2)	µA
		Low power regulator usage	44.1	82.5(2)	600.6	1179.3	2119.1	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	80.6	116.7	572.3	1079.2	1896.3	
		Low power regulator usage	21.4	58.9	567.9	1134.5	2049.6	
		Low power low voltage regulator usage	17.0	49.0(2)	497.4	1003.6	1817.0(2)	

1. Guaranteed by characterization results.
2. Tested in production.

Table 35. Typical and maximum current consumption in Standby mode - V_{DD}= 1.7 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	2.3	3.7	15.9	32.5	76.8	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	2.9	4.3	16.5	33.1	77.4	
		RTC and LSE OFF	1.1	2.5	14.7	31.3	75.6	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization results.

Table 36. Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	3.7	5.2	20.6	40.5	82.7	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	4.5	6.0	21.4	41.3	83.5	
		RTC and LSE OFF	2.5	4.0	19.4	39.3	81.5(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, not tested in production unless otherwise specified.
3. Tested in production.

Table 37. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions(1)	Typ				Max(2)			Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V			
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.84	1.04	1.24	3.00	5.00	10.00	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.51	1.64	1.89	2.00	3.80	5.80	11.60	
		RTC and LSE OFF	0.03	0.03	0.04	0.04	2.00	4.00	8.00	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

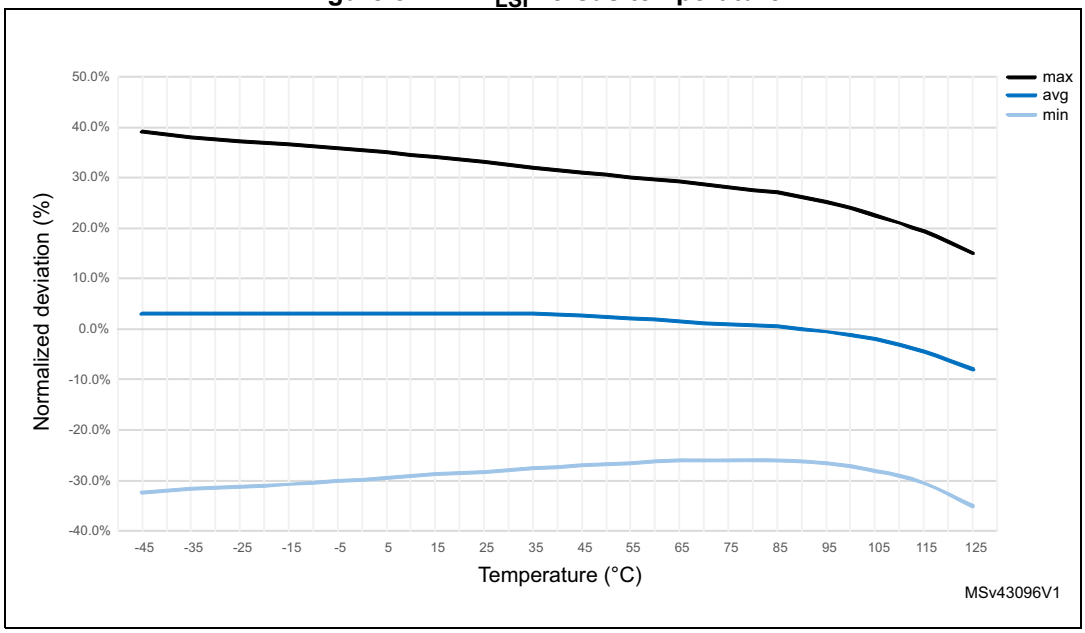
Low-speed internal (LSI) RC oscillator

Table 46. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} (2)	Frequency	16.1	32.0	47.0	kHz
$t_{su(LSI)}$ (3)	LSI oscillator startup time	-	15.0	40.0	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 32. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 47* and *Table 48* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 47. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLP_OUT}	PLLP multiplier output clock	-		24	-	100	
f_{PLLQ_OUT}	48 MHz PLLQ multiplier output clock	-		-	48	75	
f_{PLLR_OUT}	PLLR multiplier output clock for I2S and SAI	-		-	-	216	
f_{VCO_OUT}	PLL VCO output	-		100	-	432	
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples.		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 55: EMI characteristics for LQFP144*). It is available only on the main PLL.

Table 49. SSCG parameter constraints

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	(Modulation period) * (Increment Step)	-	-	2^{15}-1	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126 md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

FMPI^{2}C characteristics

The following table presents FMPI^{2}C characteristics.

Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

Table 66. FMPI^{2}C characteristics(1)

	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	18	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-0	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(2)	pF

1. Based on characterization results.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

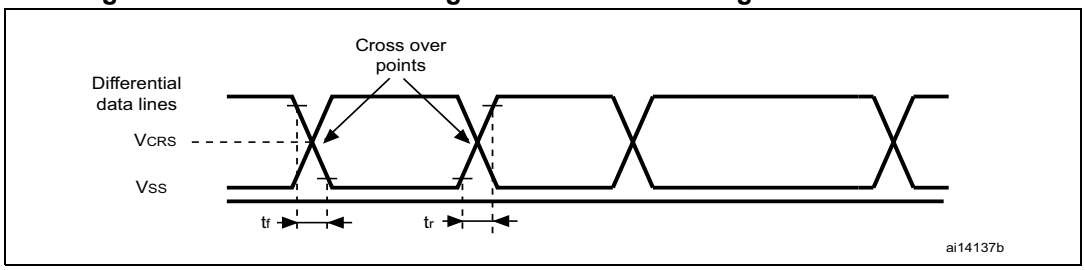


Table 74. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).