What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413zgj6

Figure 9. Startup in regulator OFF: slow V_{DD} slope power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization

MSv31179V2
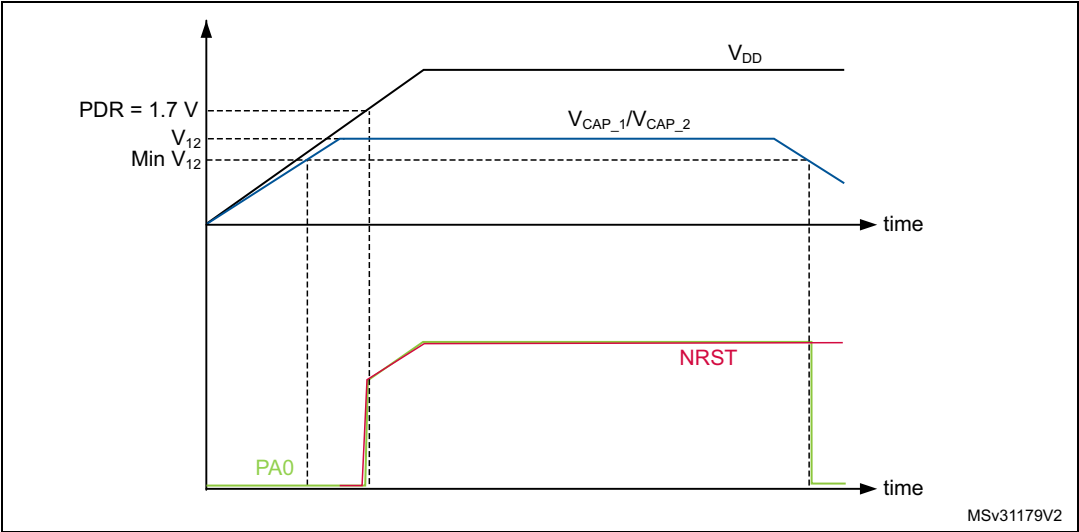
1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization

MSv31180V1
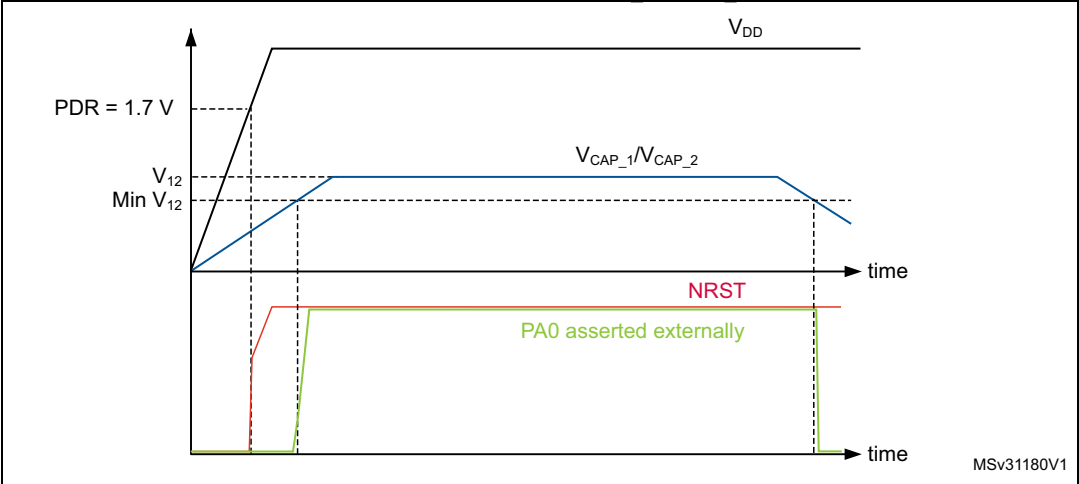
1. This figure is valid whatever the internal reset mode (ON or OFF).

- 8-bit or 12-bit output mode
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference (V_{REF+})

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.38   Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.39   Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.40   Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F413xG/H through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 18: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, f_{PCLK1} = f_{HCLK}/2, and f_{PCLK2} = f_{HCLK}.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max[1]				Unit
				T_A= 25 °C	T_A= 25 °C	T_A=85 °C	T_A=105 °C	T_A=125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled[2][3]	100	32.9	34.96	35.30	37.21	40.79	mA
			84	26.5	28.13	28.58	30.50	33.96	
			64	18.3	19.44	20.11	21.76	25.03	
			50	14.4	15.28	16.12	17.95	21.11	
			25	7.5	8.10	9.35	11.09	14.38	
			20	6.4	6.99	8.17	9.96	13.17	
		HSI, PLL off, all peripherals enabled[2][3]	16	4.6	5.17	6.42	8.28	11.46	
			1	0.7	1.28	2.64	4.30	7.66	
		External clock, PLL ON, all peripherals disabled[3]	100	15.4	16.43	17.35	19.17	22.85	
			84	12.4	13.28	14.32	16.12	19.67	
			64	8.7	9.36	10.38	12.06	15.31	
			50	6.9	7.47	8.54	10.36	13.49	
			25	3.7	4.27	5.47	7.17	10.45	
			20	3.2	3.72	5.01	6.67	10.02	
		HSI, PLL off, all peripherals disabled[3]	16	2.3	2.80	4.05	5.90	9.07	
			1	0.6	1.14	2.51	4.16	7.51	

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V$_{DD}$ = 1.7 V

Symbol	Parameter	Conditions	f$_{HCLK}$ (MHz)	Typ	Max[1]				Unit
				T$_A$ = 25 °C	T$_A$ = 25 °C	T$_A$ = 85 °C	T$_A$ = 105 °C	T$_A$ = 125 °C	
I$_{DD}$	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled[2][3]	100	30.2	32.03	32.71	34.69	38.46	mA
			84	24.3	25.77	26.58	28.47	32.16	
			64	16.8	17.80	18.66	20.53	23.85	
			50	13.2	14.05	15.12	16.85	20.27	
			25	7.1	7.62	8.92	10.81	14.11	
			20	6.1	6.69	7.95	9.72	13.09	
		HSI, PLL OFF, all peripherals enabled[2]	16	4.4	4.99	6.28	8.18	11.45	
			1	0.9	1.50	2.88	4.58	8.00	
		External clock, PLL ON[4] all peripherals disabled[2]	100	12.6	13.46	14.75	16.68	20.54	
			84	10.2	10.90	12.25	14.10	17.84	
			64	7.2	7.70	8.95	10.81	14.14	
			50	5.7	6.26	7.56	9.26	12.72	
			25	3.2	3.77	5.11	6.82	10.26	
			20	2.9	3.41	4.79	6.49	9.92	
		HSI, PLL OFF, all peripherals disabled[2]	16	2.1	2.63	3.91	5.80	9.06	
			1	0.8	1.34	2.72	4.42	7.86	

1. Guaranteed by characterization results..

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

Table 38. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

Table 48. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock[1]	-		0.95[2]	1	2.10	MHz
$f_{PLLI2SQ\_OUT}$	48 MHz PLLI2SQ multiplier output clock	-		-	48	75	
$f_{PLLI2SR\_OUT}$	PLLI2SR multiplier output clock for I2S and SAI	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	μs
		VCO freq = 432 MHz		100	-	300	
Jitter[3]	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	
$I_{DD(PLLI2S)}$[4]	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$[4]	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.

2. Guaranteed by design.

3. Value given with main PLL running.

4. Guaranteed by characterization results.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 55*. They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	1B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	3B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP81.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Figure 37. Recommended NRST pin protection
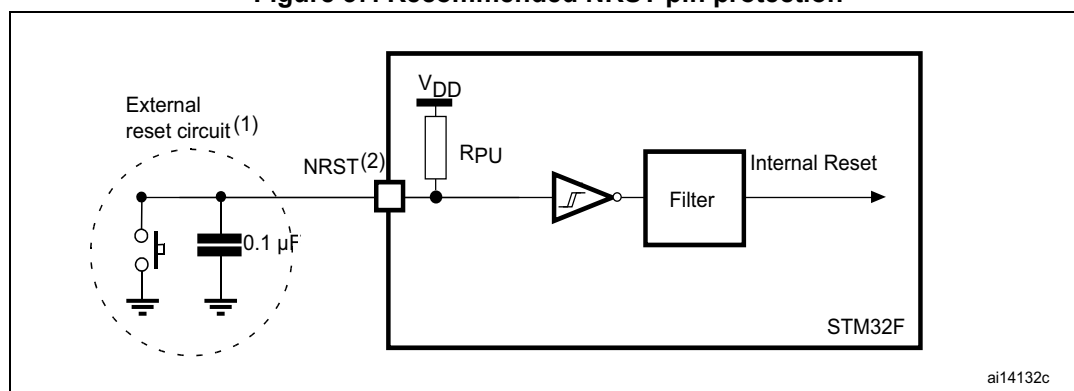
1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 62*. Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in *Table 63* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 63. TIMx characteristics[1][2]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 100 MHz	0	$f_{TIMxCLK}$/2	MHz
			0	50	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 100 MHz	0.0119	780	μs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.

2. Guaranteed by design.

3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

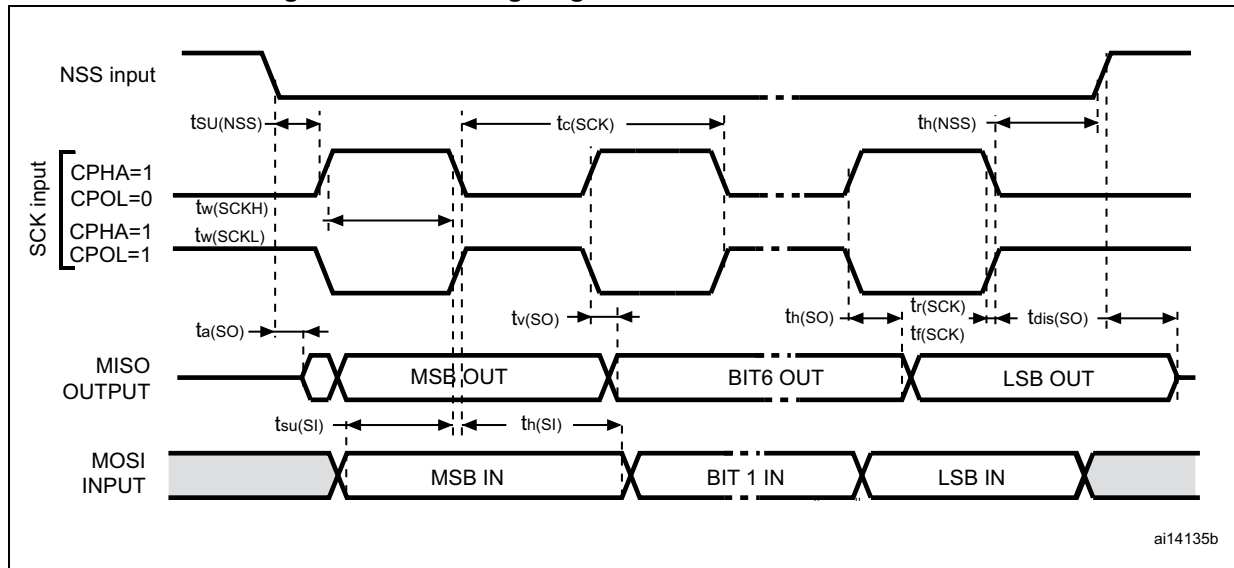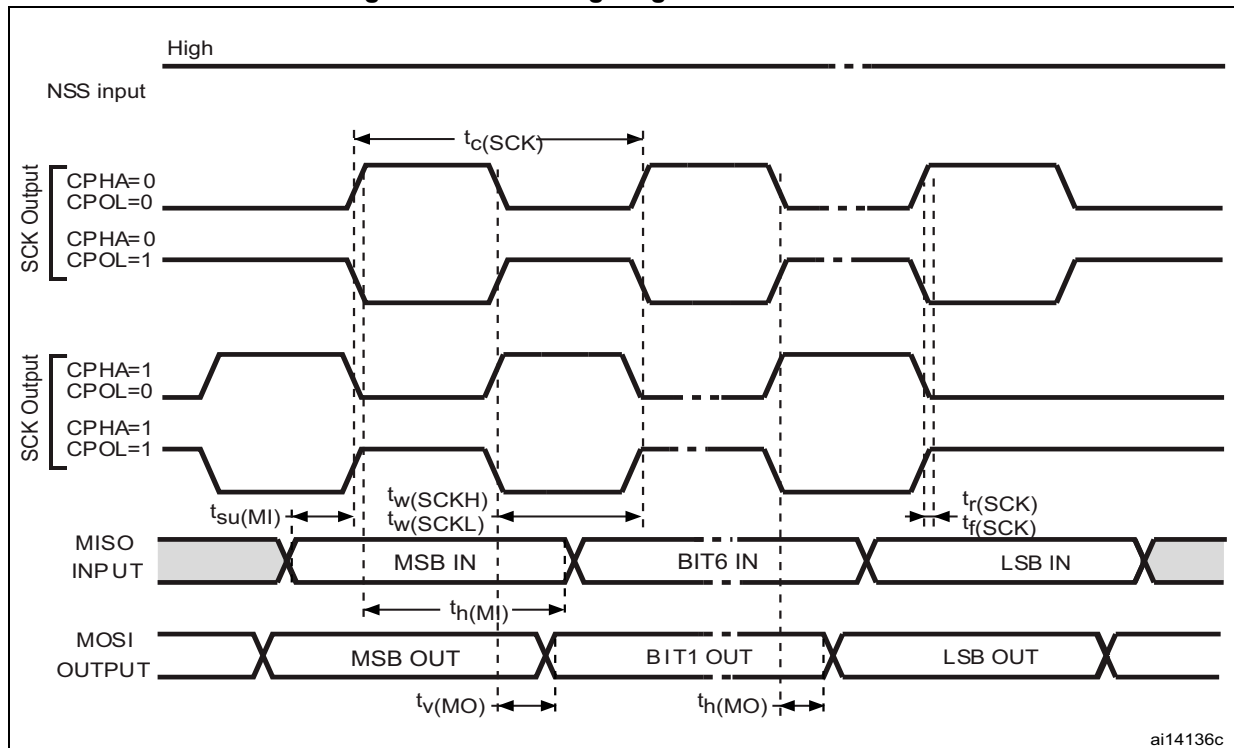**Figure 41. SPI timing diagram - slave mode and CPHA = 1**

Figure 42. SPI timing diagram - master mode

I^{2}S interface characteristics

Unless otherwise specified, the parameters given in *Table 68* for the I^{2}S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 68. I^{2}S dynamic characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 * 8K	256 * Fs[2]	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64 * Fs	MHz
		Slave data: 32 bits	-	64 * Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	1.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	2.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	6	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3.5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.

2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0430 reference manual for more details on the sampling frequency (F_S).

f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.

Table 77. ADC accuracy at f$_{ADC}$ = 30 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max[2]	Unit
ET	Total unadjusted error	f$_{ADC}$ = 30 MHz, R$_{AIN}$ < 10 kΩ, V$_{DDA}$ = 2.4 to 3.6 V, V$_{REF}$ = 1.7 to 3.6 V, V$_{DDA}$ −V$_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V$_{DD}$, frequency and temperature ranges.

2. Guaranteed by characterization results.

Table 78. ADC accuracy at f$_{ADC}$ = 36 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max[2]	Unit
ET	Total unadjusted error	f$_{ADC}$ =36 MHz, V$_{DDA}$ = 2.4 to 3.6 V, V$_{REF}$ = 1.7 to 3.6 V V$_{DDA}$ −V$_{REF}$ < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V$_{DD}$, frequency and temperature ranges.

2. Guaranteed by characterization results.

Table 79. ADC dynamic accuracy at f$_{ADC}$ = 18 MHz - limited test conditions[1]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f$_{ADC}$ =18 MHz V$_{DDA}$ = V$_{REF+}$= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization results.

Table 80. ADC dynamic accuracy at f$_{ADC}$ = 36 MHz - limited test conditions[1]

| Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f$_{ADC}$ = 36 MHz V$_{DDA}$ = V$_{REF+}$ = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 48. ADC accuracy characteristics
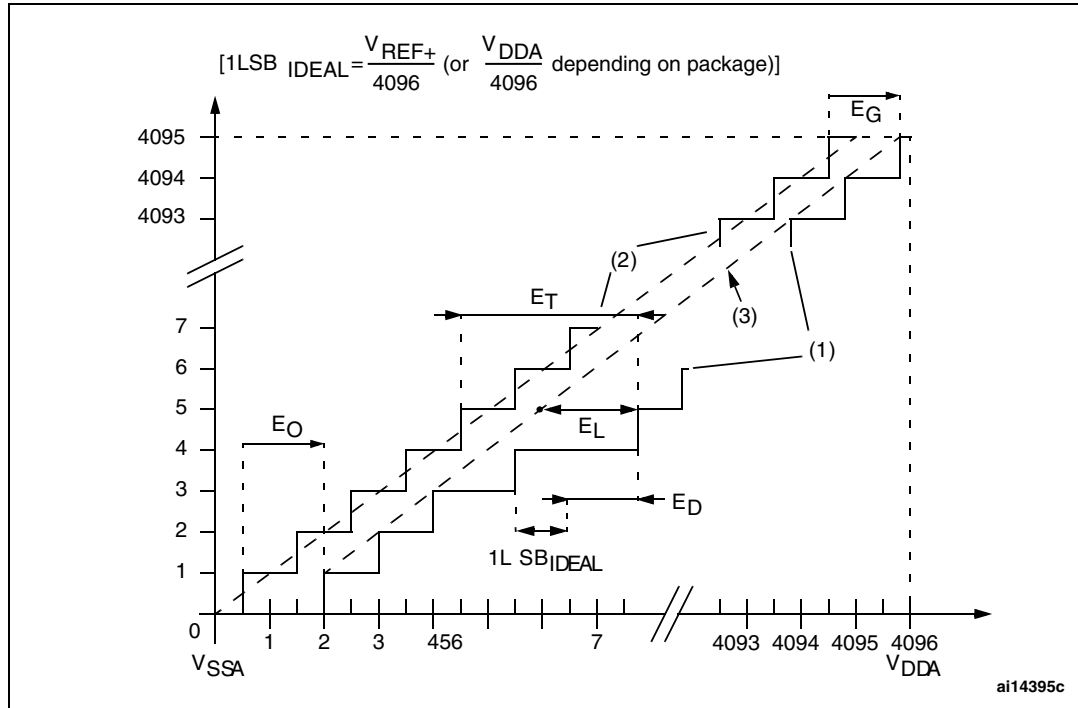
1. See also *Table 77*.

2. Example of an actual transfer curve.

3. Ideal transfer curve.

4. End point correlation line.

5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

6.3.24 DAC electrical characteristics

Table 86. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	-		1.7[1]	-	3.6	V	
V_{REF+}	Reference supply voltage	-		1.7[1]	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	-		0	-	0	V	-
R_{LOAD}[2]	Resistive load	DAC output buffer ON	R_{LOAD} connected to V_{SSA}	5	-	-	kΩ	-
			R_{LOAD} connected to V_{DDA}	25	-	-	kΩ	-
R_O[2]	Impedance output with buffer OFF	-		-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}[2]	Capacitive load	-		-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer ON	-		0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer ON	-		-	-	V_{DDA} − 0.2	V	
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer OFF	-		-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer OFF	-		-	-	V_{REF+} − 1LSB	V	
I_{VREF+}[4]	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-		-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}[4]	DAC DC VDDA current consumption in quiescent mode[3]	-		-	280	380	µA	With no load, middle code (0x800) on the inputs
		-		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Table 87. DFSDM characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < V_{DD} < 3.6 V	t_{CKIN} / 2 - 0.5	t_{CKIN} / 2	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < V_{DD} < 3.6 V	3.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) 1.71 < V_{DD} < 3.6 V	2.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0) 1.71 < V_{DD} < 3.6 V	(CKOUTDIV + 1) * $t_{DFBDMCLK}$	-	(2 * CKOUTDIV) * $t_{DFBDMCLK}$	

1. Data based on characterization results.

Table 105. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. UFQFPN48 recommended footprint
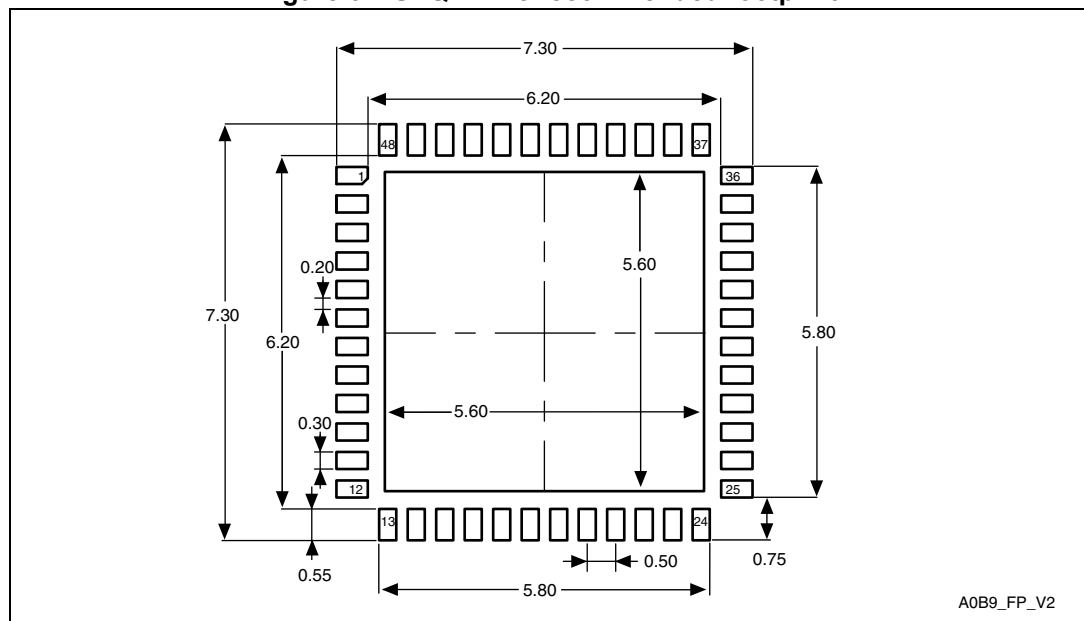
1. Dimensions are in millimeters.

7.5   LQFP144 package information

**Figure 75. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline**
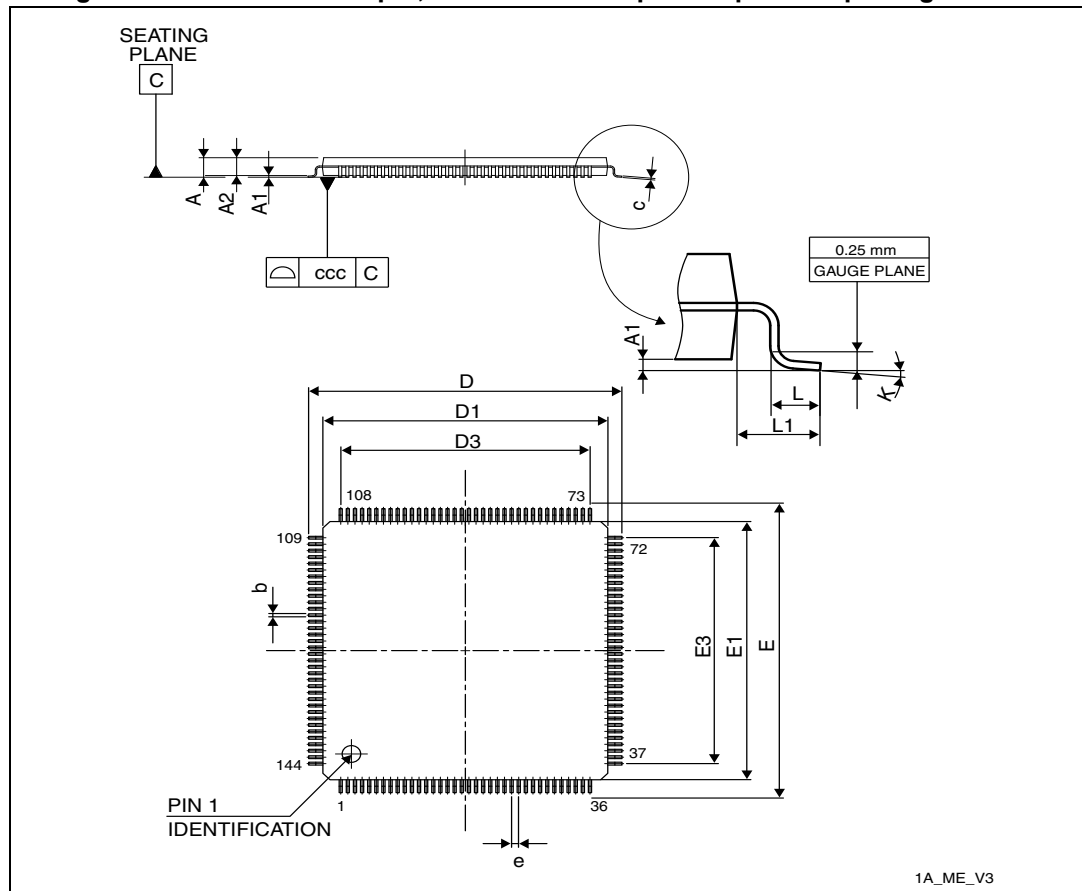
1.   Drawing is not to scale.

Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint

A02Y_FP_V1
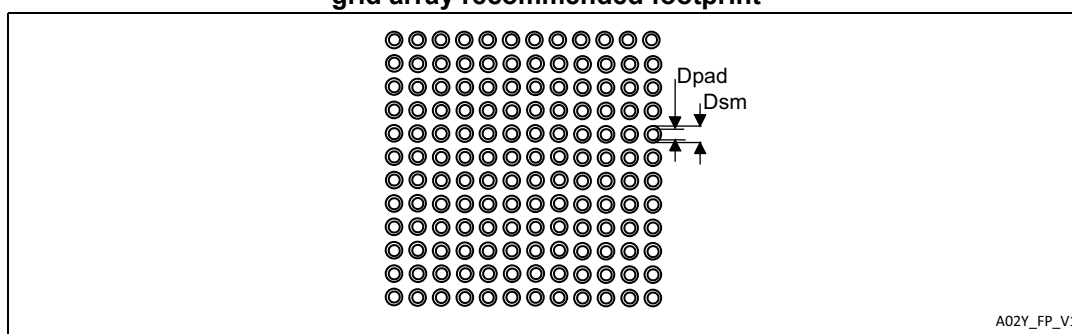
Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)

Note: *Non solder mask defined (NSMD) pads are recommended.*

4 to 6 mils solder paste screen printing process.

Stencil opening is 0.400 mm.

Stencil thickness is between 0.100 mm and 0.125 mm.

Pad trace width is 0.120 mm.

IMPORTANT NOTICE – PLEASE READ CAREFULLY