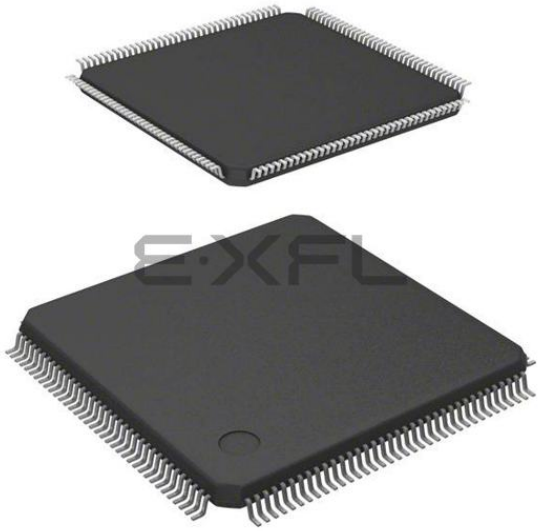

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413zgt6

A dedicated application note (AN4515) describes how to implement the STM32F413xG/H BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1.5 Mbytes of Flash memory available for storing programs and data, plus 512 bytes of one-time programmable (OTP) memory organized in 16 blocks of 32 bytes, each which can be independently locked.

The user Flash memory area can be protected against read operations by an entrusted code (read protection or RDP). Different protection levels are available. The user Flash memory is divided into sectors, which can be individually protected against write operation. Flash sectors can also be protected individually against D-bus read accesses by using the proprietary readout protection (PCROP).

Refer to the product line reference manual for additional information on OTP area and protection features.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.20: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

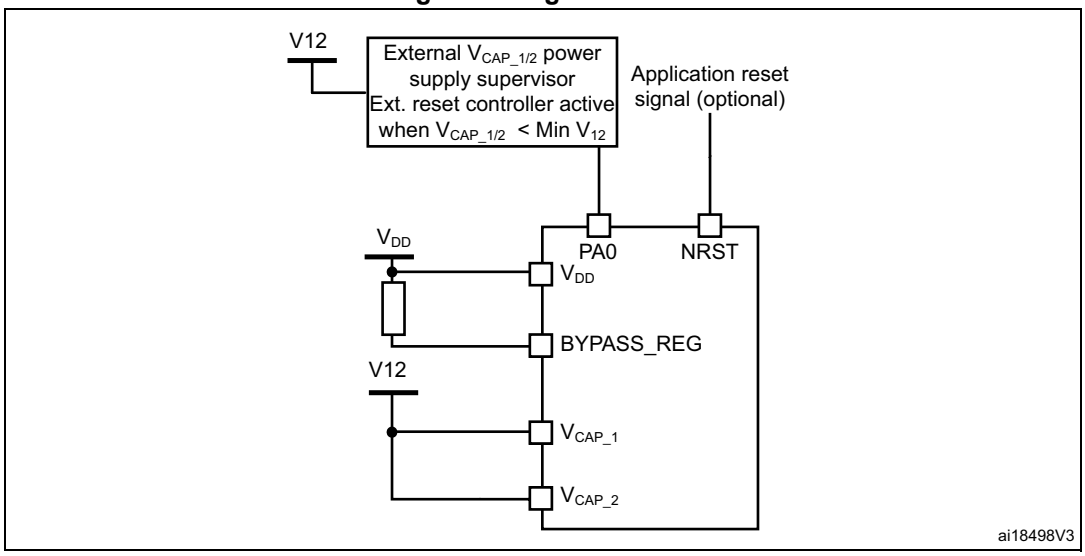
Before disabling the Flash, the code must be executed from the internal RAM.

3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

USART1, USART2, USART3 and USART6 provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 7. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)
USART2	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
USART3	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
UART4	X	-	X	-	X	-	3.12	6.25	APB1 (max. 50 MHz)
UART5	X	-	X	-	X	-	3.12	6.25	APB1 (max. 50 MHz)
USART6	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)
UART7	X	-	X	-	X	-	3.12	6.25	APB1 (max. 50 MHz)
UART8	X	-	X	-	X	-	3.12	6.25	APB1 (max. 50 MHz)
UART9	X	-	X	-	X	-	6.25	12.5	APB2 (max. 100 MHz)
UART10	X	-	X	-	X	-	6.25	12.5	APB2 (max. 100 MHz)

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
18	26	E4	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_IN8
19	27	G5	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_IN9
20	28	H5	37	L6	J5	48	PB2	I/O	FT	-	LPTIM1_OUT, DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	G4	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-
-	-	-	-	-	M6	54	PF14	I/O	FTf	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FTf	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, UART9_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, UART9_TX, FSMC_A11, EVENTOUT	-
-	-	NC	38	M7	M7	58	PE7	I/O	FT	(2)	TIM1_ETR, DFSDM1_DATIN2, UART7_Rx, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	SPI5_SCK/I2S5_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	SPI5_NSS/I2S5_WS	-	DFSDM1_DATIN0	QUADSPI_CLK	-	-	-	-	-	EVENTOUT
	PB2	-	LPTIM1_OUT	-	-	-	-	DFSDM1_CKIN0	-	-	QUADSPI_CLK	-	-	-	-	-	EVENTOUT
	PB3	JTDO-SWO	TIM2_CH2	-	-	I2CFMP1_SDA	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	USART1_RX	UART7_RX	I2C2_SDA	SAI1_SD_A	CAN3_RX	-	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	UART7_TX	I2C3_SDA	SAI1_SCK_A	CAN3_TX	SDIO_D0	-	-	EVENTOUT
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	SAI1_FS_A	UART5_RX	SDIO_D3	-	-	EVENTOUT
	PB6	-	LPTIM1_ETR	TIM4_CH1	-	I2C1_SCL	-	DFSDM2_CKIN7	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	UART5_TX	SDIO_D0	-	-	EVENTOUT
	PB7	-	LPTIM1_IN2	TIM4_CH2	-	I2C1_SDA	-	DFSDM2_DATIN7	USART1_RX	-	-	-	-	FSMC_NL	-	-	EVENTOUT
	PB8	-	LPTIM1_OUT	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	SPI5_MOSI/I2S5_SD	DFSDM2_CKIN1	CAN1_RX	I2C3_SDA	-	UART5_RX	SDIO_D4	-	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM2_DATIN1	-	CAN1_TX	I2C2_SDA	-	UART5_TX	SDIO_D5	-	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	I2S3_MCK	USART3_TX	-	I2CFMP4_SCL	DFSDM2_CKOUT	-	SDIO_D7	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_CKIN	-	USART3_RX	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	SPI4_NSS/I2S4_WS	SPI3_SCK/I2S3_CK	USART3_CK	CAN2_RX	DFSDM1_DATIN1	UART5_RX	FSMC_D13/FSMC_DA13	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2CFMP1_SMBA	SPI2_SCK/I2S2_CK	SPI4_SCK/I2S4_CK	-	USART3_CTS	CAN2_TX	DFSDM1_CKIN1	UART5_TX	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2CFMP1_SDA	SPI2_MISO	I2S2ext_SD	USART3_RTS	DFSDM1_DATIN2	TIM12_CH1	FSMC_D0/FSMC_DA0	-	SDIO_D6	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	I2CFMP1_SCL	SPI2_MOSI/I2S2_SD	-	-	DFSDM1_CKIN2	TIM12_CH2	-	-	SDIO_CK	-	-	EVENTOUT

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port E	PE0	-	-	TIM4_ ETR	DFSDM2_ CKIN4	-	-	-	-	UART8_ Rx	-	-	-	FSMC_ NBL0	-	-	EVENT OUT
	PE1	-	-	-	DFSDM2_ DATIN4	-	-	-	-	UART8_ Tx	-	-	-	FSMC_ NBL1	-	-	EVENT OUT
	PE2	TRACE CLK	-	-	-	-	SPI4_SCK /I2S4_CK	SPI5_SCK/ I2S5_CK	SAI1_ MCLK_A	-	QUADSPI_ BK1_IO2	-	UART10 _RX	FSMC_A23	-	-	EVENT OUT
	PE3	TRACE D0	-	-	-	-	-	-	SAI1_SD_B	-	-	-	UART10 _TX	FSMC_A19	-	-	EVENT OUT
	PE4	TRACE D1	-	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	SAI1_SD_A	DFSDM1_ DATIN3	-	-	-	FSMC_A20	-	-	EVENT OUT
	PE5	TRACE D2	-	-	TIM9_CH1	-	SPI4_MISO	SPI5_MISO	SAI1_SCK_ A	DFSDM1_ CKIN3	-	-	-	FSMC_A21	-	-	EVENT OUT
	PE6	TRACE D3	-	-	TIM9_CH2	-	SPI4_MOSI/ I2S4_SD	SPI5_MOSI/ I2S5_SD	SAI1_FS_A	-	-	-	-	FSMC_A22	-	-	EVENT OUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-	UART7_ Rx	-	QUADSPI_ BK2_IO0	-	FSMC_D4/ FSMC_DA4	-	-	EVENT OUT
	PE8	-	TIM1_ CH1N	-	-	-	-	DFSDM1_ CKIN2	-	UART7_ Tx	-	QUADSPI_ BK2_IO1	-	FSMC_D5/ FSMC_DA5	-	-	EVENT OUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-	-	-	QUADSPI_ BK2_IO2	-	FSMC_D6/ FSMC_DA6	-	-	EVENT OUT
	PE10	-	TIM1_ CH2N	-	DFSDM2_ DATIN0	-	-	-	-	-	-	QUADSPI_ BK2_IO3	-	FSMC_D7/ FSMC_DA7	-	-	EVENT OUT
	PE11	-	TIM1_ CH2	-	DFSDM2_ CKIN0	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	-	-	-	-	FSMC_D8/ FSMC_DA8	-	-	EVENT OUT
	PE12	-	TIM1_ CH3N	-	DFSDM2_ DATIN7	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	-	-	-	FSMC_D9/ FSMC_DA9	-	-	EVENT OUT
	PE13	-	TIM1_ CH3	-	DFSDM2_ CKIN7	-	SPI4_MISO	SPI5_MISO	-	-	-	-	-	FSMC_D10/ FSMC_DA10	-	-	EVENT OUT
	PE14	-	TIM1_ CH4	-	-	-	SPI4_MOSI/ I2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	DFSDM2_ DATIN1	-	FSMC_D11/F SMC_DA11	-	-	EVENT OUT
	PE15	-	TIM1_ BKIN	-	-	-	-	-	-	-	-	DFSDM2_ CKIN1	-	FSMC_D12/ FSMC_DA12	-	-	EVENT OUT

6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Note: This feature is only available for UFBGA100 and UFBGA144 packages.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage @ 3.3V.

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60(1)	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	39.9	42.46	43.17	45.32	49.19	mA
			84	32.6	34.71	35.45	37.58	41.24	
			64	24.2	25.86	26.73	28.47	31.96	
			50	19.7	21.01	22.00	23.74	27.26	
			25	10.8	11.55	12.83	14.66	18.03	
			20	9.2	9.82	11.16	13.09	16.36	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.8	7.33	8.77	10.69	14.00	
			1	1.2	1.83	3.08	4.83	8.19	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.3	24.11	25.26	27.35	31.11	
			84	18.5	20.00	21.15	23.20	26.87	
			64	14.6	15.81	17.02	18.74	22.20	
			50	12.2	13.14	14.45	16.18	19.66	
			25	7.0	7.52	8.95	10.84	14.19	
			20	6.0	6.58	7.95	9.74	13.07	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.5	4.97	6.40	8.30	11.59	
			1	1.0	1.61	2.94	4.65	8.05	

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 29. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	42.3	45.08	45.76	47.88	51.71	mA
			84	34.6	36.87	37.58	39.64	43.32	
			64	25.5	27.18	27.93	29.90	33.23	
			50	20.2	21.55	22.50	24.34	27.73	
			25	10.9	11.61	12.87	14.72	18.08	
			20	9.3	9.86	11.20	13.13	16.41	
		HSI, PLL OFF, all peripherals enabled	16	6.9	7.37	8.81	10.72	14.04	
			1	1.2	1.83	3.09	4.83	8.19	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.76	27.84	29.93	33.66	
			84	20.5	22.18	23.25	25.33	28.98	
			64	15.9	17.13	18.23	20.18	23.46	
			50	12.7	13.68	14.95	16.71	20.13	
			25	7.1	7.57	9.01	10.88	14.25	
			20	6.1	6.61	7.98	9.80	13.11	
		HSI, PLL OFF, all peripherals disabled	16	4.5	5.00	6.44	8.33	11.63	
			1	1.0	1.61	2.94	4.65	8.06	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB1	AHB-APB1 bridge	0.90	0.88	0.81	µA/MHz
	TIM2	13.08	12.48	11.16	
	TIM3	9.98	9.50	8.50	
	TIM4	9.88	9.43	8.44	
	TIM5	13.14	12.52	11.19	
	TIM6	1.94	1.86	1.66	
	TIM7	1.86	1.79	1.56	
	TIM12	5.56	5.29	4.72	
	TIM13	3.44	3.29	2.94	
	TIM14	3.66	3.48	3.09	
	LPTIM1	7.34	7.00	6.25	
	WWDG	0.64	0.62	0.53	
	SPI2/I2S2	3.02	2.88	2.56	
	SPI3/I2S3	3.06	2.90	2.59	
	USART2	3.30	3.14	2.81	
	USART3	3.32	3.14	2.81	
	UART4	3.18	3.02	2.69	
	UART5	3.26	3.10	2.75	
	I2C1	3.20	3.05	2.72	
	I2C2	3.30	3.14	2.81	
	I2C3	3.26	3.10	2.78	
	I2CFMP1	5.22	4.98	4.44	
	CAN1	5.58	5.31	4.75	
	CAN2	5.14	4.88	4.38	
	CAN3	5.70	5.43	4.84	
	PWR	0.90	0.86	0.75	
	DAC1	2.14	2.05	1.81	
	UART7	3.08	2.93	2.59	
	UART8	3.10	2.95	2.63	

6.3.10 PLL characteristics

The parameters given in *Table 47* and *Table 48* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 47. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLP_OUT}	PLLP multiplier output clock	-		24	-	100	
f_{PLLQ_OUT}	48 MHz PLLQ multiplier output clock	-		-	48	75	
f_{PLLR_OUT}	PLLR multiplier output clock for I2S and SAI	-		-	-	216	
f_{VCO_OUT}	PLL VCO output	-		100	-	432	
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples.		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 58. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0, PDR_ON, BYPASS_REG	- 0	0	mA
	Injected current on NRST	- 0	NA	
	Injected current on PE6, PC13, PC14, PC15, PF0, PF1, PF2, PC0, PC1, PC2, PC3	- 0	NA	
	Injected current on any other FT and FTf pins	- 5	NA	
	Injected current on any other pins	- 5	+ 5	

1. NA = not applicable.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.16 I/O port characteristics

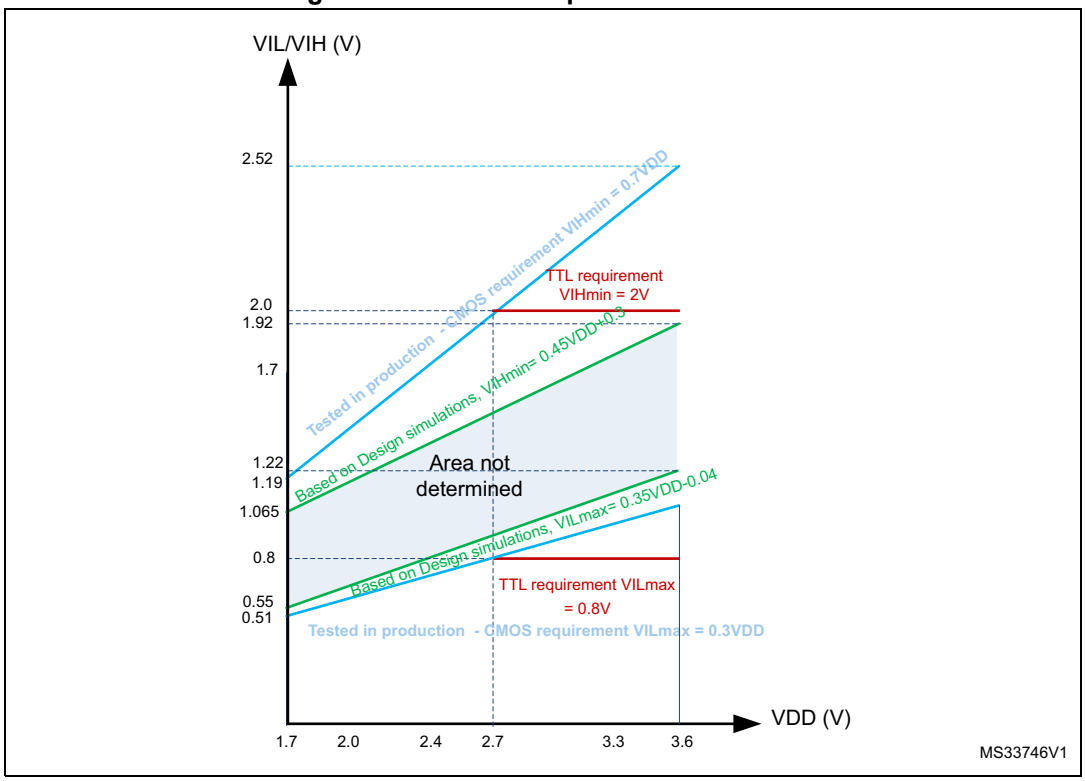
General input/output characteristics

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 59. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa, TC and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.3V_{DD}$(1)	V
	BOOT0 I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	-	-	$0.1V_{DD}$+0.1(2)	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C	-	-		
V_{IH}	FT, TTa, TC and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.7V_{DD}$(1)	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	$0.17V_{DD}$+0.7(2)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C				
V_{HYS}	FT, TTa, TC and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	10% V_{DD}(2)(3)	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤125 °C	0.1	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤125 °C				

Figure 35. FT/TC I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 15*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 15*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 67. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7	12.5	ns
		Slave mode (after enable edge), 1.71 V < V_{DD} < 3.6 V	-	7	19	
$t_{v(MO)}$		Master mode	-	2	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	ns
$t_{h(MO)}$		Master mode	1.5	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0

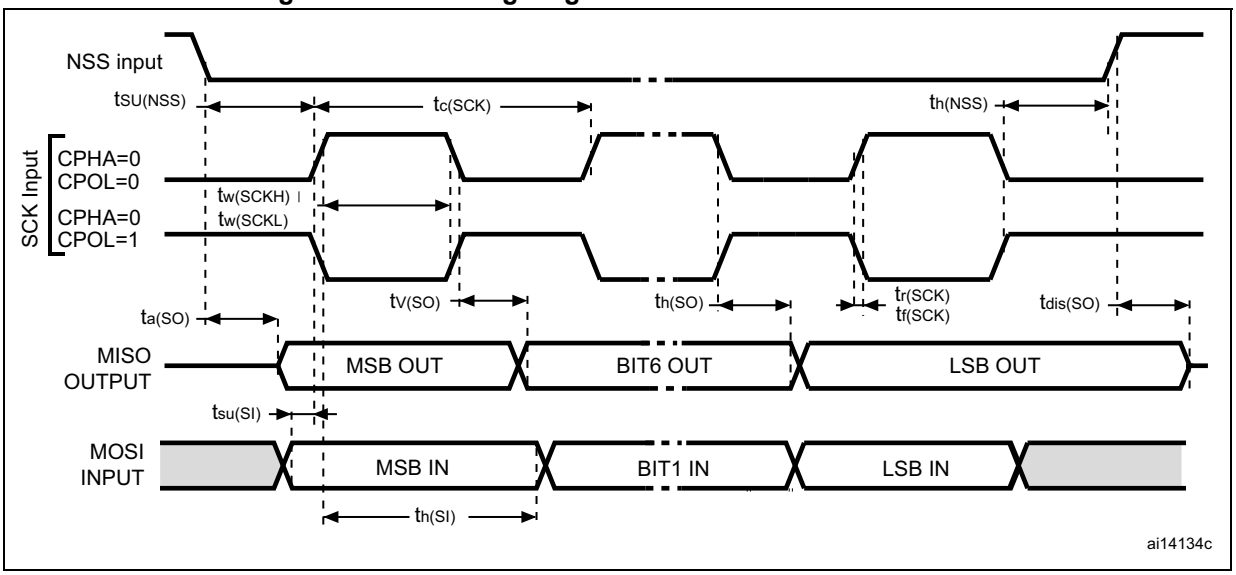


Table 71. QSPI dynamic characteristics in DDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low time	-	$t_{(CK)}$ / 2 - 1	-	$t_{(CK)}$ / 2	ns
$t_{w(CKL)}$			$t_{(CK)}$ / 2	-	$t_{(CK)}$ / 2 + 1	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	2.7 V < V_{DD} < 3.6 V	0.5	-	-	
		1.71 V < V_{DD} < 3.6 V	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<3.6 V	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	9	
		1.71 V<V_{DD}<3.6 V	-	8.5	11.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	7.5	-	-	

1. Guaranteed by characterization results.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 72. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 73. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.

Figure 60. Synchronous non-multiplexed PSRAM write timings

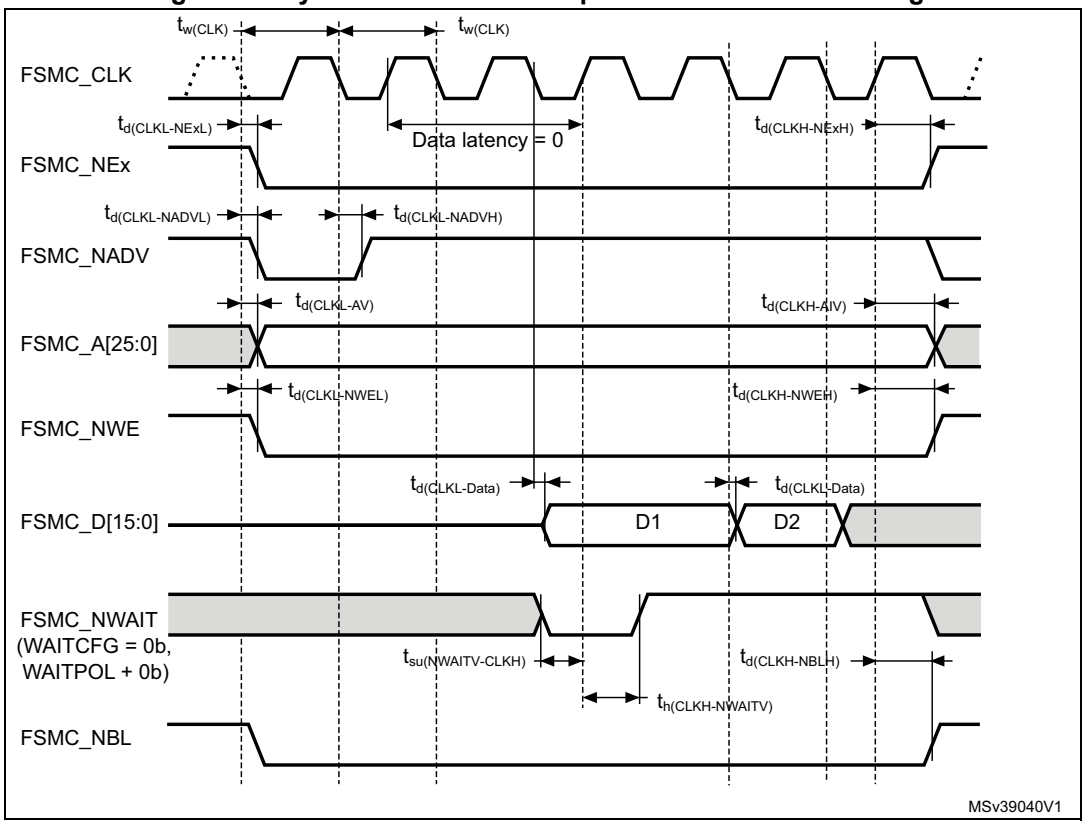


Table 99. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	2 * T_{HCLK} - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 1	-	
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK} + 1	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

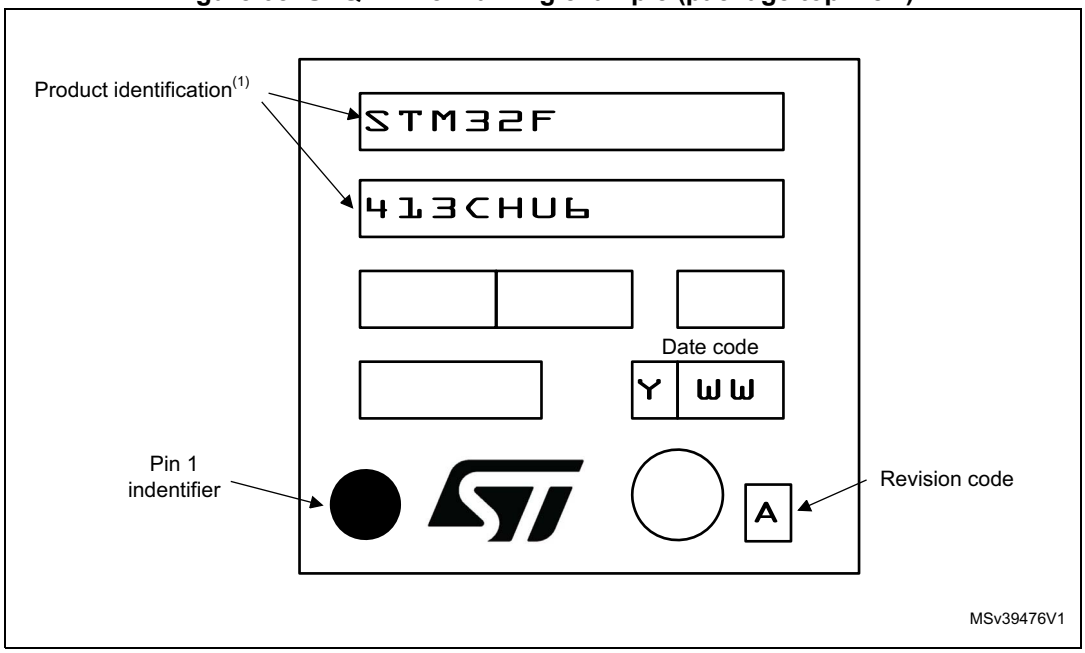
1. C_L = 30 pF.
2. Guaranteed by characterization results.

Device marking for UFQFPN48

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 68. UFQFPN48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.