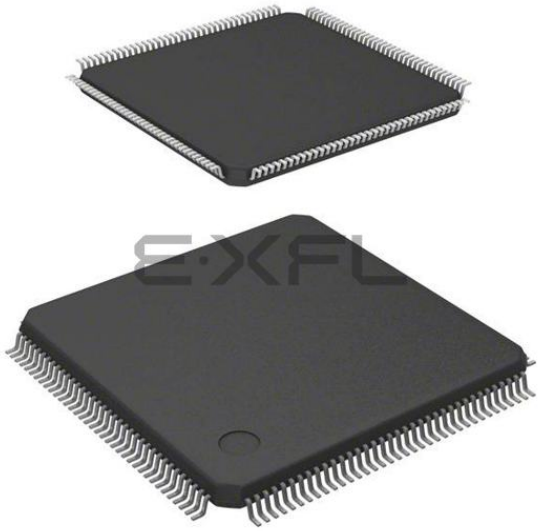

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413zht3

Figure 2. Compatible board design for LQFP64 package

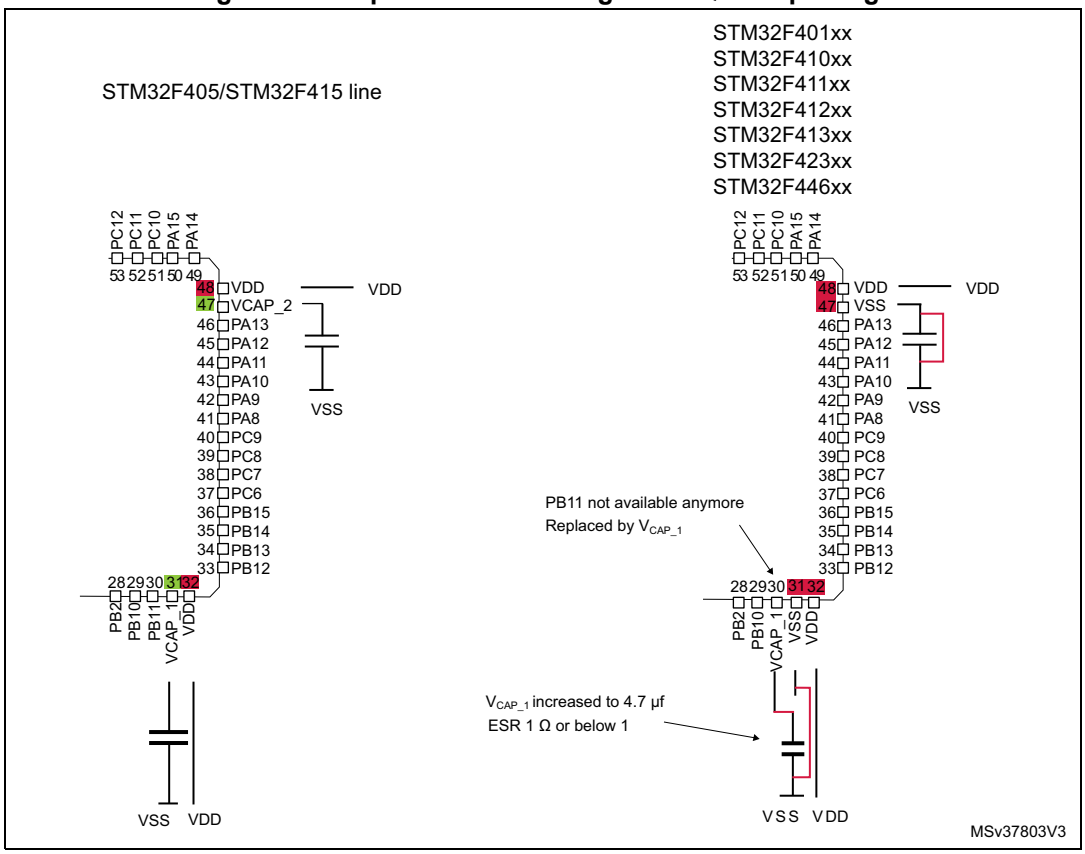
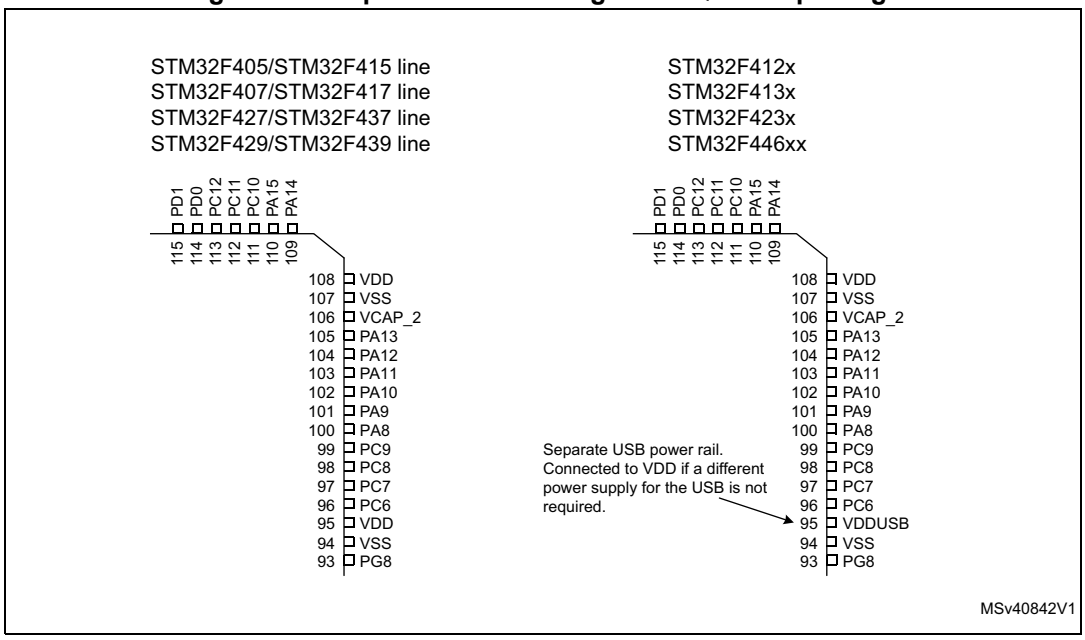


Figure 3. Compatible board design for LQFP144 package



A dedicated application note (AN4515) describes how to implement the STM32F413xG/H BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1.5 Mbytes of Flash memory available for storing programs and data, plus 512 bytes of one-time programmable (OTP) memory organized in 16 blocks of 32 bytes, each which can be independently locked.

The user Flash memory area can be protected against read operations by an entrusted code (read protection or RDP). Different protection levels are available. The user Flash memory is divided into sectors, which can be individually protected against write operation. Flash sectors can also be protected individually against D-bus read accesses by using the proprietary readout protection (PCROP).

Refer to the product line reference manual for additional information on OTP area and protection features.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.20: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Different sources can also be selected for the SAI. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or CODEC output).

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

3.29 Digital filter for sigma-delta modulators (DFSDM)

The device embeds two DFSDMs:

- DFSDM1 has 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 2 internal parallel inputs support.
- DFSDM2 features 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 4 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. It is also possible to introduce a programmable delay between different microphones (beamforming feature). DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

Table 8. DFSDM feature comparison

DFSDM instance	External input serial channels	External input parallel channels	Digital filters
DFSDM1	4	2	2
DFSDM2	8	4	4

3.30 Dynamic tuning of PDM delays for sound source localization

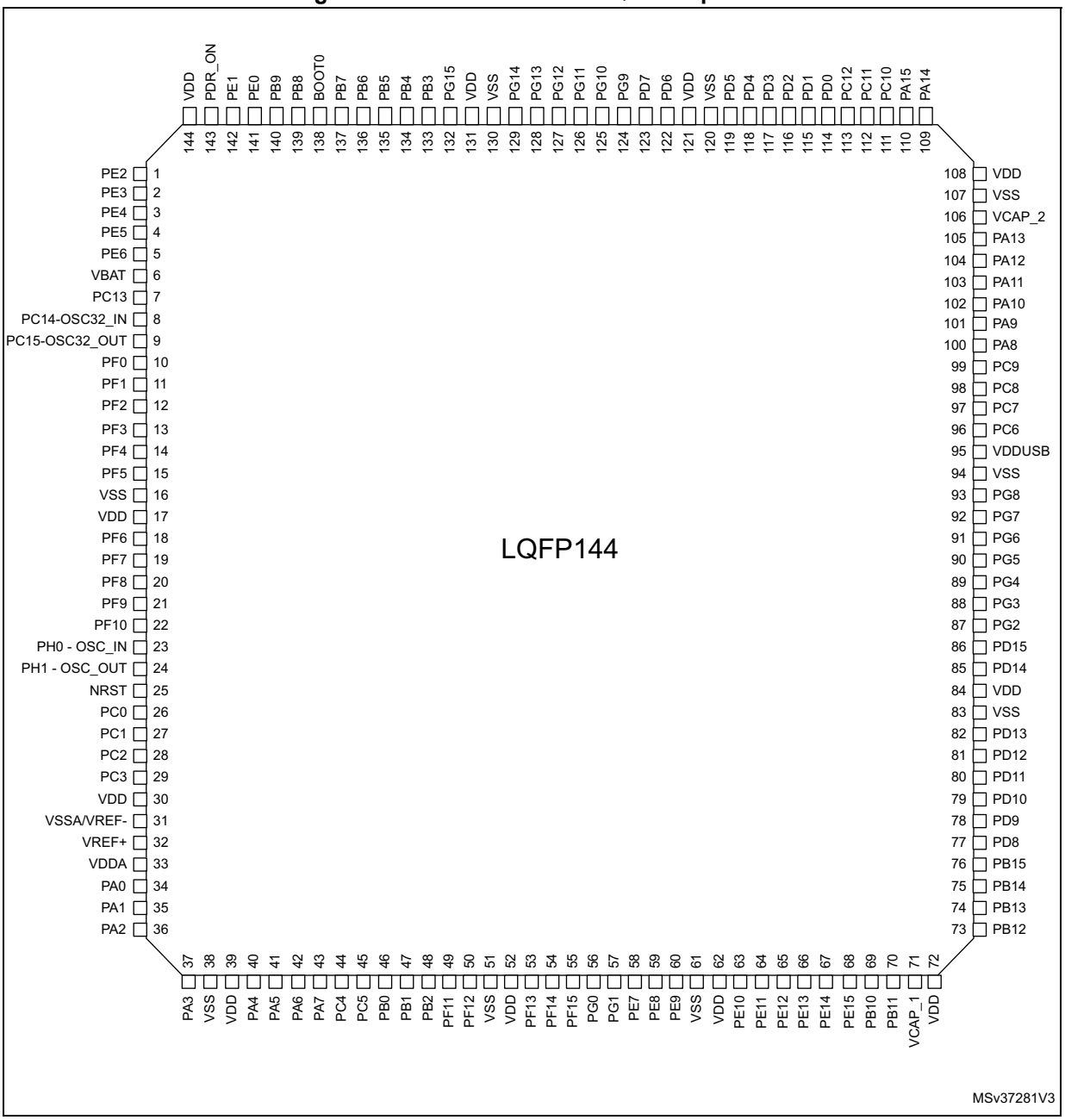
A mechanism is implemented on top of the DFSDM allowing to dynamically tune PDM delays of each microphone without the need to add external delay lines.

Audio application with several microphones require strong microphones placement constraints, as the distance between the microphones must be a multiple of v/F where v is the speed of the sound and F is the PCM sampling frequency.

The designed mechanism removes this constraint by programming delays for each digital microphone with the granularity of the PDM clock rate prior to the conversion into PCM rate.

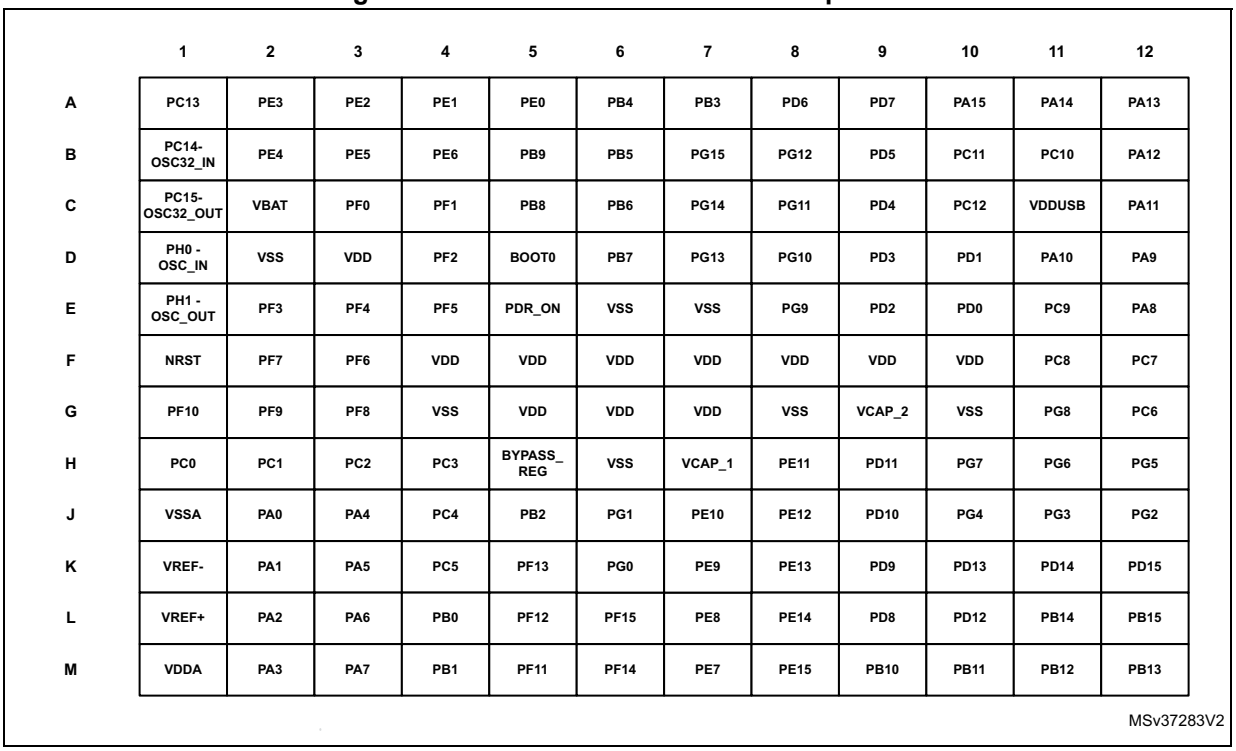
The tuning delay is performed by a clock skipping technique.

Figure 15. STM32F413xG/H LQFP144 pinout



1. The above figure shows the package top view.

Figure 17. STM32F413xG/H UFBGA144 pinout



	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	PG7	PG6	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv37283V2

1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, I2C FM+ option
	TC	Standard 3.3 V I/O
	TTa	3.3 V tolerant I/O directly connected to DAC
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	62	H10	K12	86	PD15	I/O	FTf	(2)	TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-	-	-	-
-	-	F1	-	-	C11	95	VDDUSB	S	-	-	-	-
-	37	D5	63	E12	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT	-
-	38	D4	64	E11	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-

Table 10. STM32F413xG/H pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
41	57	A6	91	C5	B6	135	PB5	I/O	FT	-	LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SAI1_FS_A, UART5_RX, SDIO_D3, EVENTOUT	-
42	58	B6	92	B5	C6	136	PB6	I/O	FT	-	LPTIM1_ETR, TIM4_CH1, I2C1_SCL, DFSDM2_CKIN7, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, UART5_TX, SDIO_D0, EVENTOUT	-
43	59	B7	93	B4	D6	137	PB7	I/O	FT	-	LPTIM1_IN2, TIM4_CH2, I2C1_SDA, DFSDM2_DATIN7, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	A7	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C6	95	A3	C5	139	PB8	I/O	FT	-	LPTIM1_OUT, TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, DFSDM2_CKIN1, CAN1_RX, I2C3_SDA, UART5_RX, SDIO_D4, EVENTOUT	-
46	62	D6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM2_DATIN1, CAN1_TX, I2C2_SDA, UART5_TX, SDIO_D5, EVENTOUT	-
-	-	NC	97	C3	A5	141	PE0	I/O	FT	(2)	TIM4_ETR, DFSDM2_CKIN4, UART8_Rx, FSMC_NBL0, EVENTOUT	-
-	-	NC	98	A2	A4	142	PE1	I/O	FT	(2)	DFSDM2_DATIN4, UART8_Tx, FSMC_NBL1, EVENTOUT	-
47	63	A8	99	D3	E6	-	VSS	S	-	-	-	-

Table 13. STM32F413xG/H register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6800- 0x4001 FFFF	Reserved
	0x4001 6400 - 0x4001 67FF	DFSDM2
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5C00 - 0x4001 5FFF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1/2/3
	0x4001 1C00 - 0x4001 1FFF	UART10
	0x4001 1800 - 0x4001 1BFF	UART9
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage on RST, FT and TC pins(7)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	- 0.3	-	V_{DDA} + 0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P_D	Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7(8)	UFQFPN48	-	-	625	mW
		WLCSP81	-	-	504	
		LQFP64	-	-	426	
		LQFP100	-	-	465	
		LQFP144		-	571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	417	
	Power dissipation at TA = 125°C for range 3(8)	UFQFPN48	-	-	156	
		WLCSP81	-	-	126	
		LQFP64	-	-	106	
		LQFP100	-	-	116	
		LQFP144	-	-	143	
		UFBGA100	-	-	088	
		UFBGA144	-	-	104	
T_A	Ambient temperature for range 6	Maximum power dissipation	–40	-	85	°C
		Low power dissipation(9)	–40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	–40	-	105	
		Low power dissipation(9)	–40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	–40	-	125	
		Low power dissipation(9)	–40	-	130	
T_J	Junction temperature range	Range 6	–40	-	105	
		Range 7	–40	-	125	
		Range 3	–40	-	130	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 75: ADC characteristics*.
3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF}+ < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB}. For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required.
(some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 18: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A=85 °C	T_A=105 °C	T_A=125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	32.9	34.96	35.30	37.21	40.79	mA
			84	26.5	28.13	28.58	30.50	33.96	
			64	18.3	19.44	20.11	21.76	25.03	
			50	14.4	15.28	16.12	17.95	21.11	
			25	7.5	8.10	9.35	11.09	14.38	
			20	6.4	6.99	8.17	9.96	13.17	
		HSI, PLL off, all peripherals enabled(2)(3)	16	4.6	5.17	6.42	8.28	11.46	
			1	0.7	1.28	2.64	4.30	7.66	
		External clock, PLL ON, all peripherals disabled(3)	100	15.4	16.43	17.35	19.17	22.85	
			84	12.4	13.28	14.32	16.12	19.67	
			64	8.7	9.36	10.38	12.06	15.31	
			50	6.9	7.47	8.54	10.36	13.49	
			25	3.7	4.27	5.47	7.17	10.45	
			20	3.2	3.72	5.01	6.67	10.02	
		HSI, PLL off, all peripherals disabled(3)	16	2.3	2.80	4.05	5.90	9.07	
			1	0.6	1.14	2.51	4.16	7.51	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

Table 36. Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)				Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	3.7	5.2	20.6	40.5	82.7	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	4.5	6.0	21.4	41.3	83.5	
		RTC and LSE OFF	2.5	4.0	19.4	39.3	81.5(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, not tested in production unless otherwise specified.
3. Tested in production.

Table 37. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions(1)	Typ				Max(2)			Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V			
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.84	1.04	1.24	3.00	5.00	10.00	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.51	1.64	1.89	2.00	3.80	5.80	11.60	
		RTC and LSE OFF	0.03	0.03	0.04	0.04	2.00	4.00	8.00	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

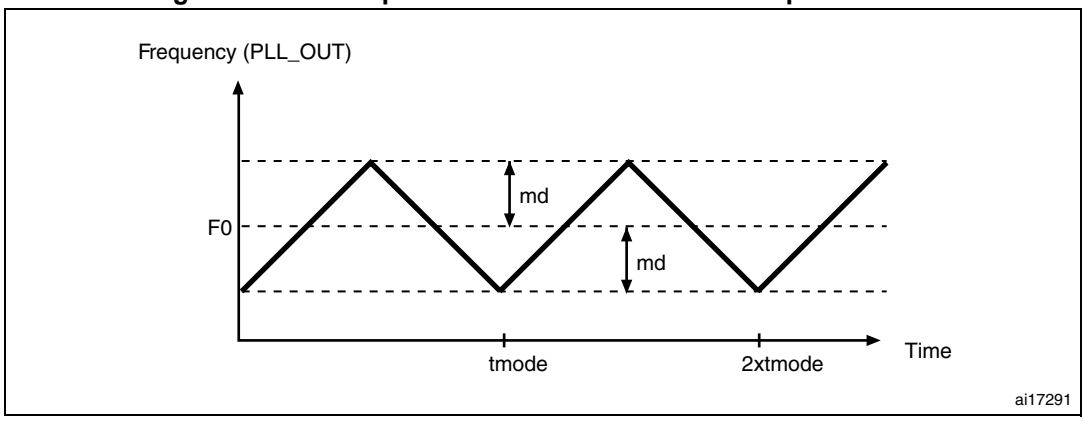
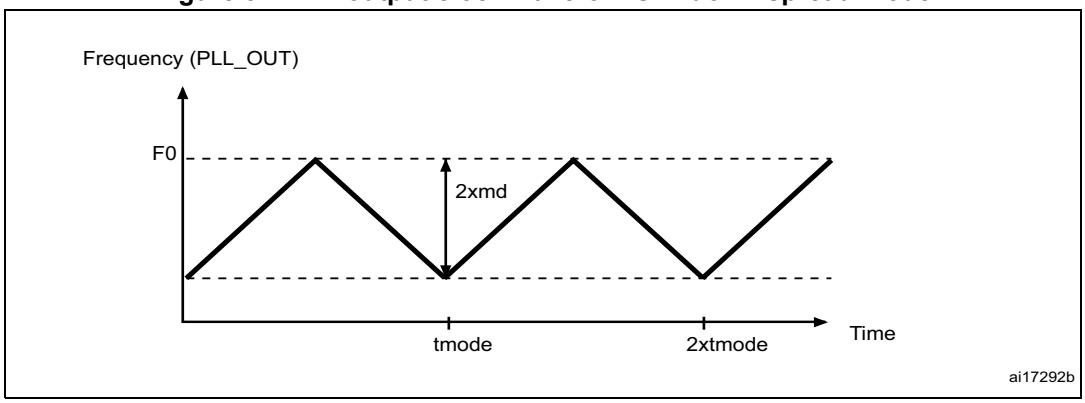


Figure 34. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 50. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

FMPI^{2}C characteristics

The following table presents FMPI^{2}C characteristics.

Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

Table 66. FMPI^{2}C characteristics(1)

	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	18	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-0	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(2)	pF

1. Based on characterization results.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

SAI characteristics

Unless otherwise specified, the parameters given in *Table 69* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 69. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256 * 8K	256 * Fs(2)	MHz
F_{SCK}	SAI clock frequency	Master data: 32 bits	-	128 * Fs	MHz
		Slave data: 32 bits	-	128 * Fs	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V <= V_{DD} <= 3.6 V	-	19	ns
		Master mode 1.71 V <= V_{DD} <= 3.6 V	-	28	
$t_{h(FS)}$	FS hold time	Master mode	13	-	
		Slave mode	0	-	
$t_{su(FS)}$	FS setup time	Slave mode	3	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V <= V_{DD} <= 3.6 V	-	15	
		Slave transmitter (after enable edge) 1.71 V <= V_{DD} <= 3.6 V	-	28	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V <= V_{DD} <= 3.6 V	-	15	
		Master transmitter (after enable edge) 1.71 V <= V_{DD} <= 3.6 V	-	29	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	13	-	

1. Guaranteed by characterization results.
2. 256 * Fs maximum corresponds to 45 MHz (APB2 maximum frequency)

Table 75. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 75*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 76. ADC accuracy at f_{ADC} = 18 MHz(1)

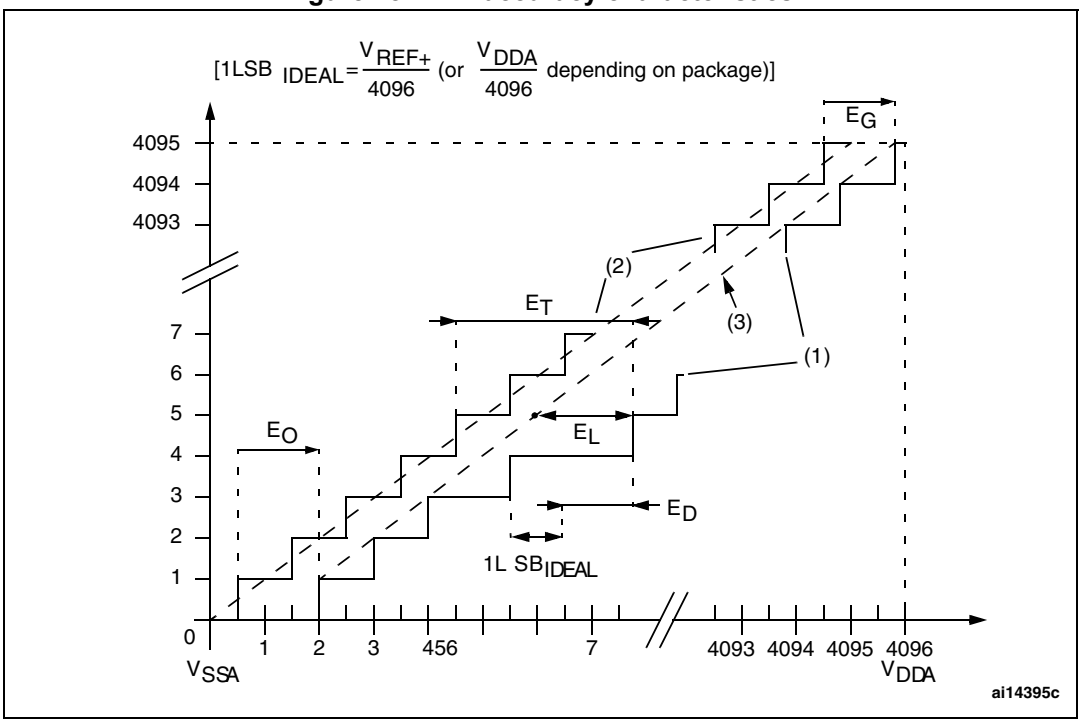
Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 48. ADC accuracy characteristics



1. See also *Table 77*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 86. DAC characteristics (continued)

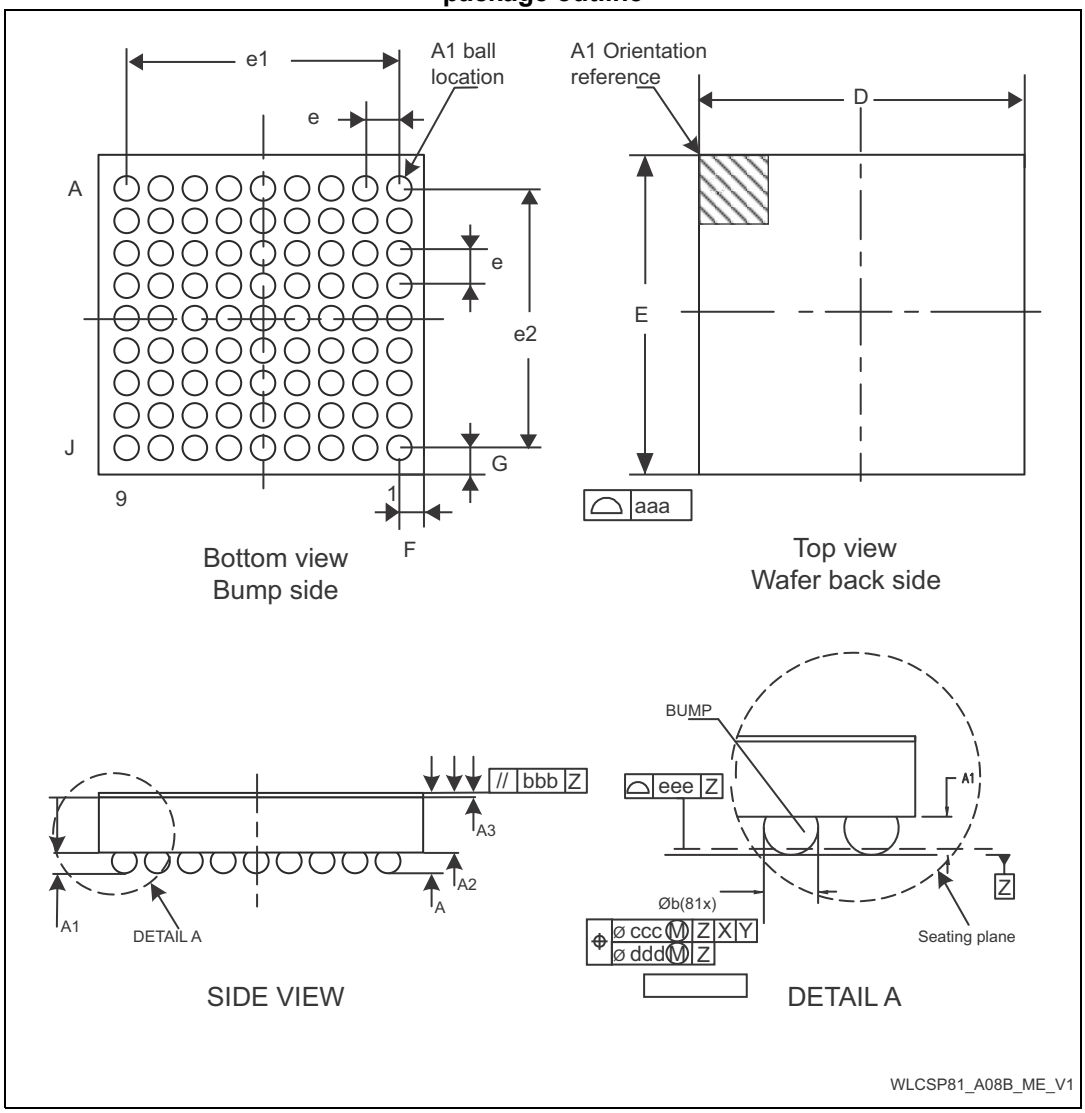
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 WLCSP81 package information

Figure 63. WLCSP81 - 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint

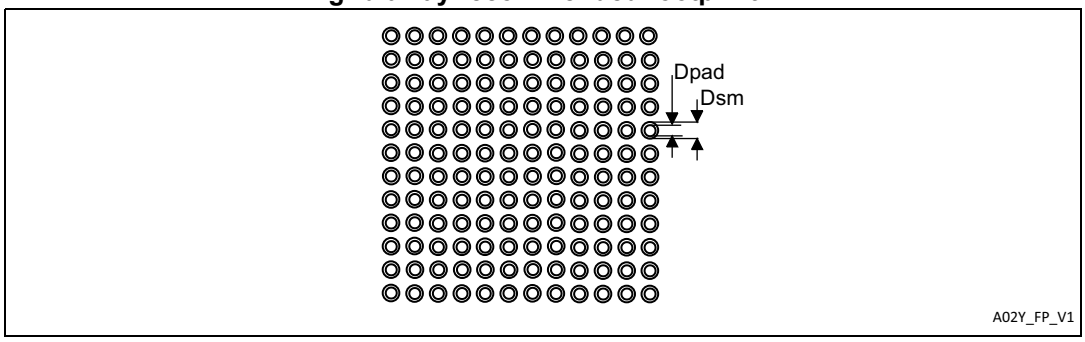


Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

Stencil opening is 0.400 mm.

Stencil thickness is between 0.100 mm and 0.125 mm.

Pad trace width is 0.120 mm.