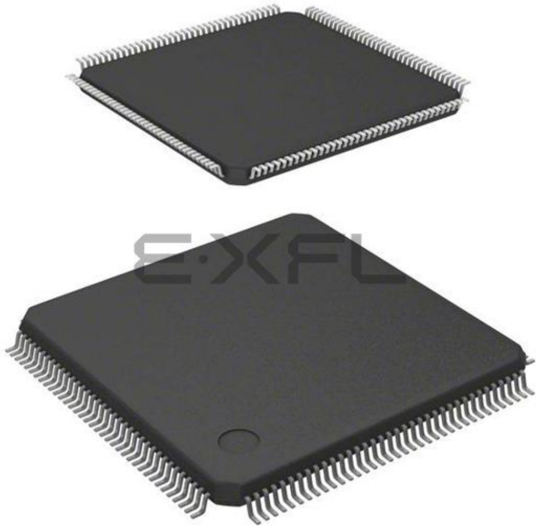

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SDIO, QSPI, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 1.5MB (1.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 320K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f413zht6 |

## 3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$ and $I^2CFMP$
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- DAC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter
- SAI.

## 3.10 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

### LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the $I^2S$ master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

## 3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

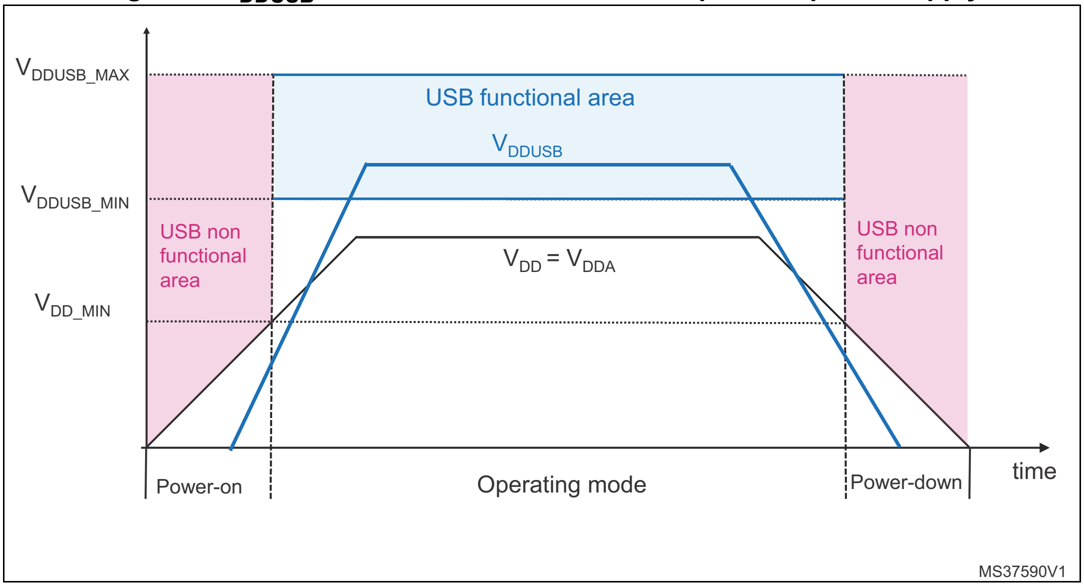
The boot loader is located in system memory. It is used to reprogram the Flash memory by using one of the interface listed in the *Table 3* or the USB OTG FS in device mode through DFU (device firmware upgrade).

**Table 3. Embedded bootloader interfaces**

| Package | USART1 PA9/ PA10 | USART2 PD6/ PD5 | USART3 PB11/ PB10 | I2C1 PB6/ PB7 | I2C2 PF0/ PF1 | I2C3 PA8/ PB4 | I2C FMP1 PB14/ PB15 | SPI1 PA4/ PA5/ PA6/ PA7 | SPI3 PA15/ PC10/ PC11/ PC12 | SPI4 PE11/ PE12/ PE13/ PE14 | CAN2 PB5/ PB13 | USB PA11 /P12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | Y | - | - | Y | - | Y | Y | Y | - | - | Y | Y |
| LQFP64 | Y | - | - | Y | - | Y | Y | Y | Y | - | Y | Y |
| WLCSP81 | Y | - | - | Y | - | Y | Y | Y | Y | Y | Y | Y |
| LQFP100 | Y | Y | - | Y | - | Y | Y | Y | Y | Y | Y | Y |
| LQFP144 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| UFBGA100 | Y | Y | Y | Y | - | Y | Y | Y | Y | Y | Y | Y |
| UFBGA144 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

**Figure 6. $V_{DDUSB}$ connected to an external independent power supply**




## 3.17 Power supply supervisor

### 3.17.1 Internal reset ON

This feature is available for $V_{DD}$ operating voltage range 1.8 V to 3.6 V.

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Table 5. Timer feature comparison (continued)

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complemen-tary output | Max. interface clock (MHz) | Max. timer clock (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| Basic timers | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 50 | 100 |
| Low-power timer | LPTIM1 | 16-bit | Up | Between 1 and 128 | No | 2 | No | 50 | 100 |

### 3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.22.2 General-purpose timers (TIMx)

There are elven synchronizable general-purpose timers embedded in the STM32F413xG/H (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F413xG/H devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four

**Figure 17. STM32F413xG/H UFBGA144 pinout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PC13 | PE3 | PE2 | PE1 | PE0 | PB4 | PB3 | PD6 | PD7 | PA15 | PA14 | PA13 |
| B | PC14-OSC32_IN | PE4 | PE5 | PE6 | PB9 | PB5 | PG15 | PG12 | PD5 | PC11 | PC10 | PA12 |
| C | PC15-OSC32_OUT | VBAT | PF0 | PF1 | PB8 | PB6 | PG14 | PG11 | PD4 | PC12 | VDDUSB | PA11 |
| D | PH0 - OSC_IN | VSS | VDD | PF2 | BOOT0 | PB7 | PG13 | PG10 | PD3 | PD1 | PA10 | PA9 |
| E | PH1 - OSC_OUT | PF3 | PF4 | PF5 | PDR_ON | VSS | VSS | PG9 | PD2 | PD0 | PC9 | PA8 |
| F | NRST | PF7 | PF6 | VDD | VDD | VDD | VDD | VDD | VDD | VDD | PC8 | PC7 |
| G | PF10 | PF9 | PF8 | VSS | VDD | VDD | VDD | VSS | VCAP_2 | VSS | PG8 | PC6 |
| H | PC0 | PC1 | PC2 | PC3 | BYPASS_REG | VSS | VCAP_1 | PE11 | PD11 | PG7 | PG6 | PG5 |
| J | VSSA | PA0 | PA4 | PC4 | PB2 | PG1 | PE10 | PE12 | PD10 | PG4 | PG3 | PG2 |
| K | VREF- | PA1 | PA5 | PC5 | PF13 | PG0 | PE9 | PE13 | PD9 | PD13 | PD14 | PD15 |
| L | VREF+ | PA2 | PA6 | PB0 | PF12 | PF15 | PE8 | PE14 | PD8 | PD12 | PB14 | PB15 |
| M | VDDA | PA3 | PA7 | PB1 | PF11 | PF14 | PE7 | PE15 | PB10 | PB11 | PB12 | PB13 |

MSv37283V2

1. The above figure shows the package top view.

**Table 9. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input/ output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | FTf | 5 V tolerant I/O, I2C FM+ option |
| | TC | Standard 3.3 V I/O |
| | TTa | 3.3 V tolerant I/O directly connected to DAC |
| | B | Dedicated BOOT0 pin |
| | NRST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Alternate functions | Functions selected through GPIOx_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 10. STM32F413xG/H pin definition (continued)**

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | - | - | - | D4 | 12 | PF2 | I/O | FT | - | I2C2_SMBA, FSMC_A2, EVENTOUT | - |
| - | - | - | - | - | E2 | 13 | PF3 | I/O | FT | - | TIM5_CH1, FSMC_A3, EVENTOUT | - |
| - | - | - | - | - | E3 | 14 | PF4 | I/O | FT | - | TIM5_CH2, FSMC_A4, EVENTOUT | - |
| - | - | - | - | - | E4 | 15 | PF5 | I/O | FT | - | TIM5_CH3, FSMC_A5, EVENTOUT | - |
| - | - | D8 | 10 | F2 | D2 | 16 | VSS | S | - | - | - | - |
| - | - | E8 | 11 | G2 | D3 | 17 | VDD | S | - | - | - | - |
| - | - | - | - | - | F3 | 18 | PF6 | I/O | FT | - | TRACED0, TIM10_CH1, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT | - |
| - | - | - | - | - | F2 | 19 | PF7 | I/O | FT | - | TRACED1, TIM11_CH1, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT | - |
| - | - | - | - | - | G3 | 20 | PF8 | I/O | FT | - | SAI1_SCK_B, UART8_RX, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT | - |
| - | - | - | - | - | G2 | 21 | PF9 | I/O | FT | - | SAI1_FS_B, UART8_TX, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT | - |
| - | - | - | - | - | G1 | 22 | PF10 | I/O | FT | - | TIM1_ETR, TIM5_CH4, EVENTOUT | - |
| 5 | 5 | E9 | 12 | F1 | D1 | 23 | PH0 - OSC_IN | I/O | FT | (6) | EVENTOUT | OSC_IN |
| 6 | 6 | F9 | 13 | G1 | E1 | 24 | PH1 - OSC_OUT | I/O | FT | (6) | EVENTOUT | OSC_OUT |
| 7 | 7 | G9 | 14 | H2 | F1 | 25 | NRST | I/O | RST | - | - | NRST |
| - | 8 | F8 | 15 | H1 | H1 | 26 | PC0 | I/O | FT | - | LPTIM1_IN1, DFSDM2_CKIN4, SAI1_MCLK_B, EVENTOUT | ADC1_IN10, WKUP2 |

**Table 10. STM32F413xG/H pin definition (continued)**

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | 18 | H7 | 27 | - | - | 38 | VSS | S | - | - | - | - |
| - | - | F6 | - | E3 | H5 | - | BYPASS_ REG | I | FT | - | - | - |
| - | 19 | J8 | 28 | - | F4 | 39 | VDD | S | - | - | - | - |
| 14 | 20 | E5 | 29 | M3 | J3 | 40 | PA4 | I/O | TTa | - | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6/FSMC_DA6, EVENTOUT | ADC1_IN4, DAC_OUT1 |
| 15 | 21 | G6 | 30 | K4 | K3 | 41 | PA5 | I/O | TTa | - | TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7/FSMC_DA7, EVENTOUT | ADC1_IN5, DAC_OUT2 |
| 16 | 22 | F5 | 31 | L4 | L3 | 42 | PA6 | I/O | FT | - | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, DFSDM2_CKIN1, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT | ADC1_IN6 |
| 17 | 23 | J7 | 32 | M4 | M3 | 43 | PA7 | I/O | FT | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, DFSDM2_DATIN1, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT | ADC1_IN7 |
| - | 24 | H6 | 33 | K5 | J4 | 44 | PC4 | I/O | FT | - | DFSDM2_CKIN2, I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT | ADC1_IN14 |
| - | 25 | J6 | 34 | L5 | K4 | 45 | PC5 | I/O | FT | - | DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT | ADC1_IN15 |

**Table 10. STM32F413xG/H pin definition (continued)**

| Pin Number | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | NC | 62 | H10 | K12 | 86 | PD15 | I/O | FTf | (2) | TIM4_CH4, I2CFMP1_SDA, DFSDM2_DATIN0, UART9_TX, FSMC_D1/FSMC_DA1, EVENTOUT | - |
| - | - | - | - | - | J12 | 87 | PG2 | I/O | FT | - | FSMC_A12, EVENTOUT | - |
| - | - | - | - | - | J11 | 88 | PG3 | I/O | FT | - | FSMC_A13, EVENTOUT | - |
| - | - | - | - | - | J10 | 89 | PG4 | I/O | FT | - | FSMC_A14, EVENTOUT | - |
| - | - | - | - | - | H12 | 90 | PG5 | I/O | FT | - | FSMC_A15, EVENTOUT | - |
| - | - | - | - | - | H11 | 91 | PG6 | I/O | FT | - | QUADSPI_BK1_NCS, EVENTOUT | - |
| - | - | - | - | - | H10 | 92 | PG7 | I/O | FT | - | USART6_CK, EVENTOUT | - |
| - | - | - | - | - | G11 | 93 | PG8 | I/O | FT | - | USART6_RTS, EVENTOUT | - |
| - | - | - | - | - | - | 94 | VSS | S | - | - | - | - |
| - | - | - | - | - | F10 | - | VDD | S | - | - | - | - |
| - | - | F1 | - | - | C11 | 95 | VDDUSB | S | - | - | - | - |
| - | 37 | D5 | 63 | E12 | G12 | 96 | PC6 | I/O | FTf | - | TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, DFSDM2_DATIN6, USART6_TX, FSMC_D1/FSMC_DA1, SDIO_D6, EVENTOUT | - |
| - | 38 | D4 | 64 | E11 | F12 | 97 | PC7 | I/O | FTf | - | TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, DFSDM2_CKIN6, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT | - |

**Table 15. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD\_x}$ power lines (source)(1) | 180 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS\_x}$ ground lines (sink)(1) | -180 | |
| $\Sigma I_{VDDUSB}$ | Total current into $V_{DDUSB}$ power lines (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD\_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS\_x}$ ground line (sink)(1) | -100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/O and control pin | -25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | -120 | |
| $I_{INJ(PIN)}$ (3) | Injected current on FT and TC pins (4) | – 5/ + 0 | |
| | Injected current on NRST and B pins (4) | | |
| | Injected current on TTa pins(5) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(6) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DDUSB}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by VIN>VDDA in the same time a negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 16. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | |
| $T_{LEAD}$ | Maximum lead temperature during soldering (WLCSP81, LQFP64/100/144, UFQFPN48, UFBGA100/144) | see note (1) | |

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

**Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max[1] | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$= 85 °C | $T_A$= 105 °C | $T_A$= 125 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled[2] | 100 | 33.3 | 35.32[3] | 35.65 | 37.65 | 41.26[3] | mA |
| | | | 84 | 26.8 | 28.45[3] | 28.97 | 30.82 | 34.39[3] | |
| | | | 64 | 18.6 | 19.74[3] | 20.35 | 22.11 | 25.35[3] | |
| | | | 50 | 14.6 | 15.57 | 16.41 | 18.21 | 21.46 | |
| | | | 25 | 7.8 | 8.37 | 9.64 | 11.32 | 14.68 | |
| | | | 20 | 6.7 | 7.25 | 8.40 | 10.25 | 13.45 | |
| | | HSI, PLL OFF[4], all peripherals enabled[2] | 16 | 4.6 | 4.96 | 6.39 | 8.20 | 11.54 | |
| | | | 1 | 0.8 | 0.86 | 2.51 | 4.34 | 7.65 | |
| | | External clock, PLL ON, all peripherals disabled[2] | 100 | 15.7 | 16.74[3] | 17.62 | 19.50 | 23.16[3] | |
| | | | 84 | 12.7 | 13.57[3] | 14.60 | 16.38 | 19.98[3] | |
| | | | 64 | 9.0 | 9.62[3] | 10.60 | 12.37 | 15.58[3] | |
| | | | 50 | 7.1 | 7.69 | 8.79 | 10.63 | 13.79 | |
| | | | 25 | 4.0 | 4.52 | 5.68 | 7.44 | 10.68 | |
| | | | 20 | 3.4 | 4.03 | 5.23 | 6.90 | 10.27 | |
| | | HSI, PLL OFF, all peripherals disabled[2] | 16 | 2.3 | 2.44 | 4.00 | 5.81 | 9.13 | |
| | | | 1 | 0.6 | 0.70 | 2.35 | 4.18 | 7.49 | |

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

**Table 43. HSE 4-26 MHz oscillator characteristics(1)**

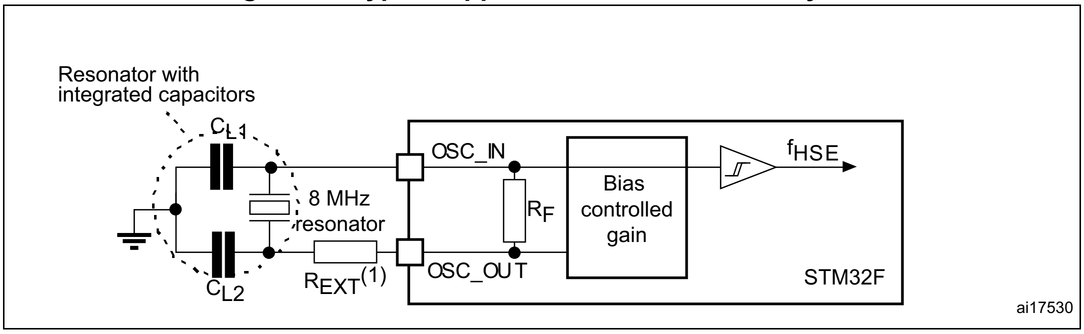
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | | 4 | - | 26 | MHz |
| $R_F$ | Feedback resistor | | - | 200 | - | kΩ |
| $I_{DD}$ | HSE current consumption | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=5 pF @25 MHz | - | 450 | - | µA |
| | | $V_{DD}$=3.3 V, ESR= 30 Ω, $C_L$=10 pF @25 MHz | - | 530 | - | |
| $ACC_{HSE}$(2) | HSE accuracy | - | -500 | - | 500 | ppm |
| $G_{m\_crit\_max}$ | Maximum critical crystal $g_m$ | Startup | - | - | 1 | mA/V |
| $t_{SU(HSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 29*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 29. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as

**Table 59. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{lkg}$ | I/O input leakage current (4) | | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | μA |
| | I/O FT/TC input leakage current (5) | | $V_{IN} = 5$ V | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(7) | All pins except for PA10 (OTG_FS_ID) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10 (OTG_FS_ID) | - | 7 | 10 | 14 | |
| $C_{IO}$(8) | I/O pin capacitance | | - | - | 5 | - | pF |

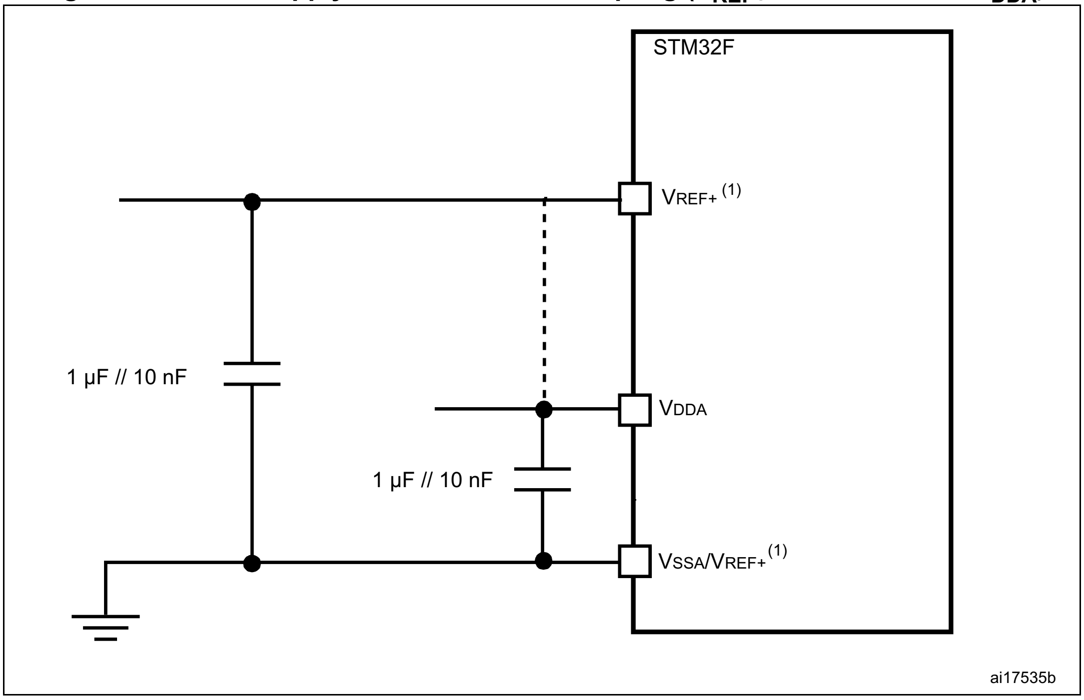
1. Guaranteed by test in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 58: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 58: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 35*.

### General PCB design guidelines

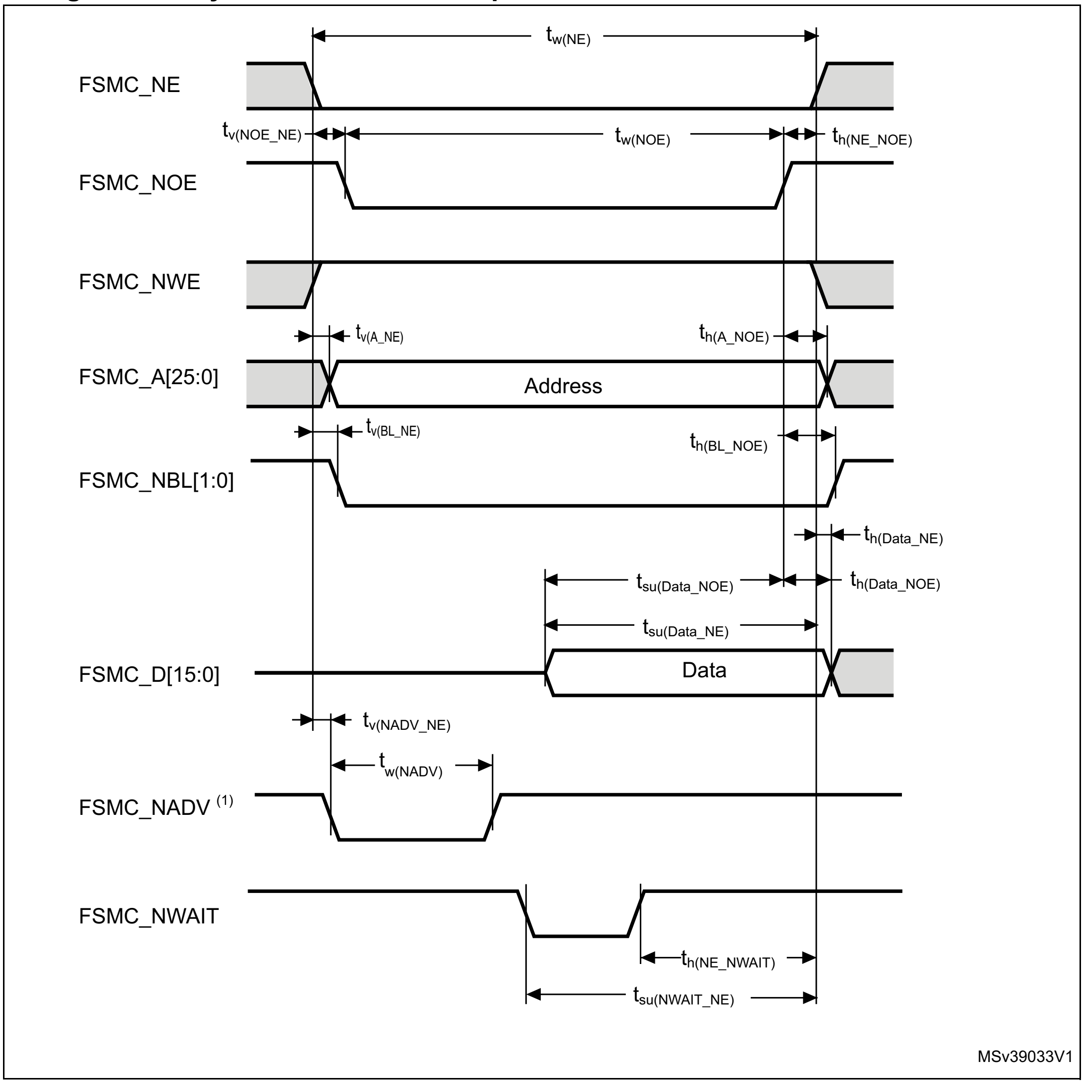
Power supply decoupling should be performed as shown in *Figure 50* or *Figure 51*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 50. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are both available on UFBGA100. $V_{REF+}$ is also available on LQFP100. When $V_{REF+}$ and $V_{REF-}$ are not available, they are internally connected to $V_{DDA}$ and $V_{SSA}$.

**Figure 53. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Figure 64. WLCSP81- 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**

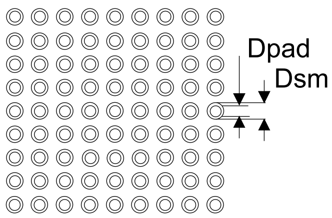



**Table 104. WLCSP81 recommended PCB design rules (0.4 mm pitch)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

## 7.2 UFQFPN48 package information

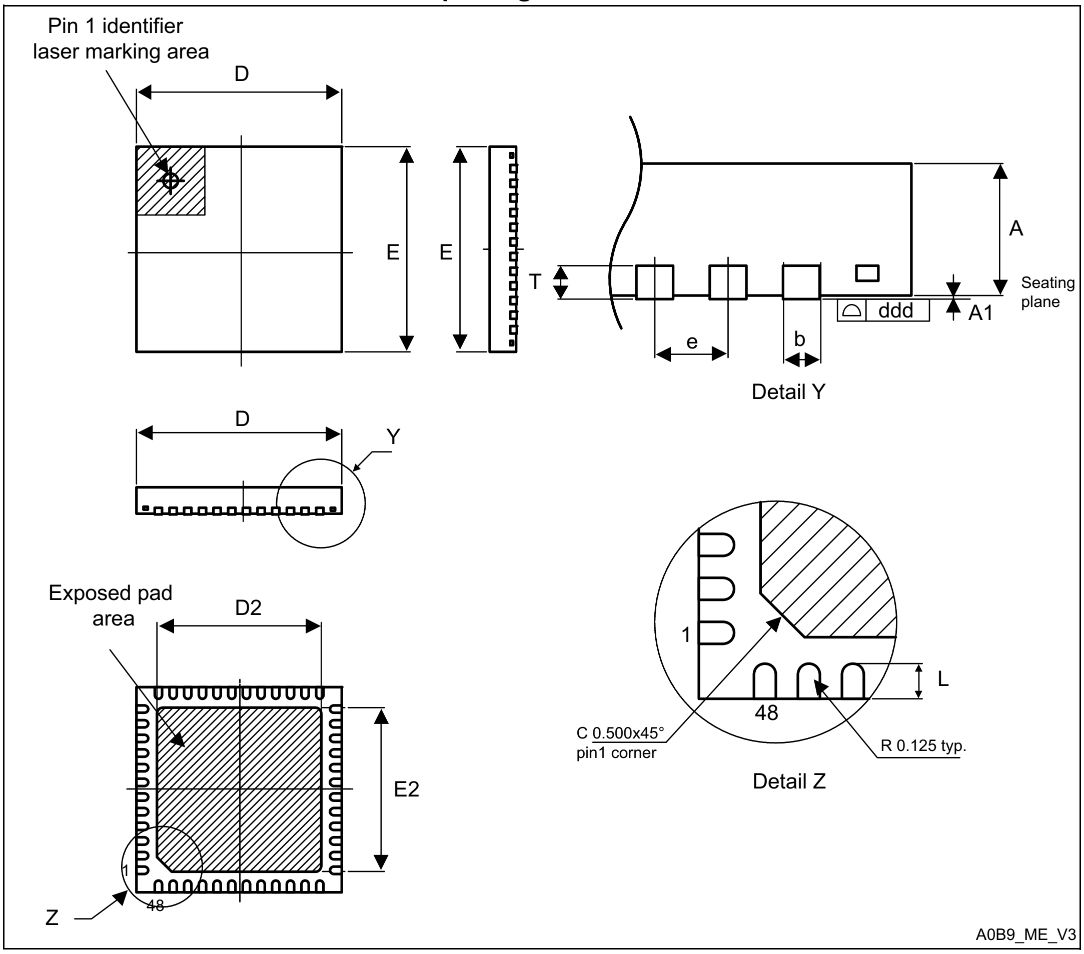
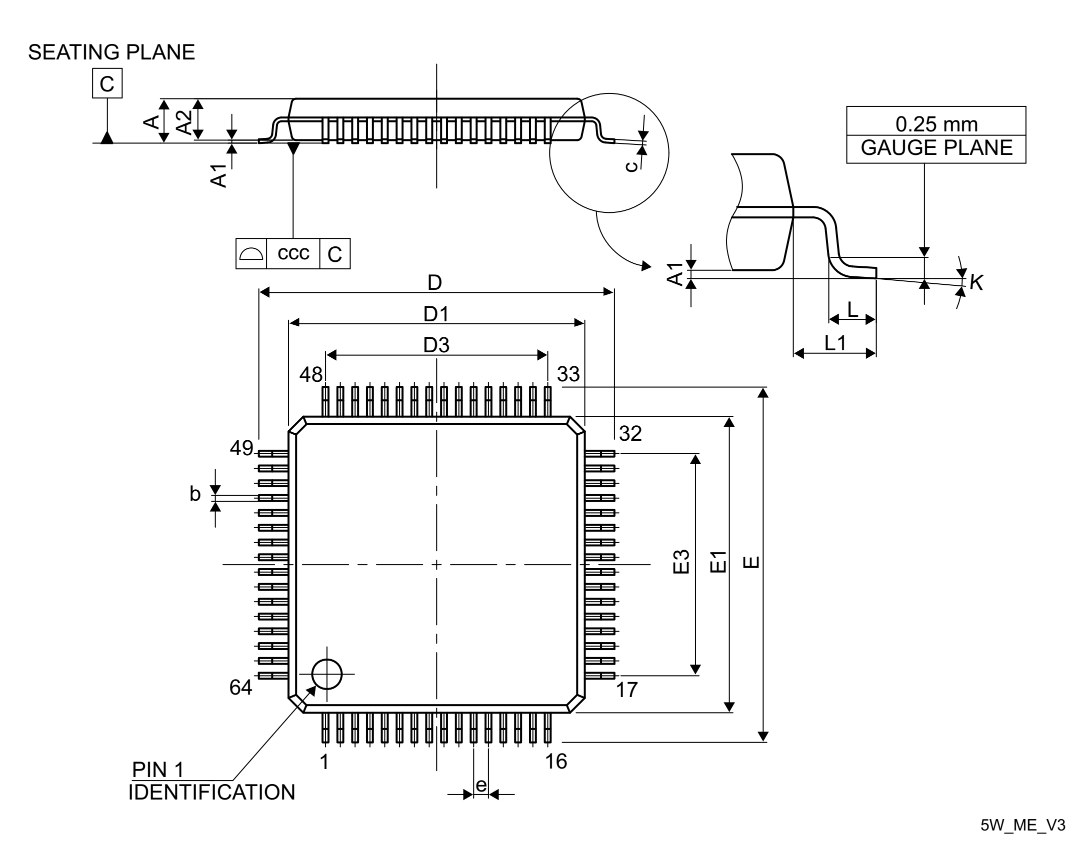



**Figure 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

## 7.3 LQFP64 package information

**Figure 69. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**



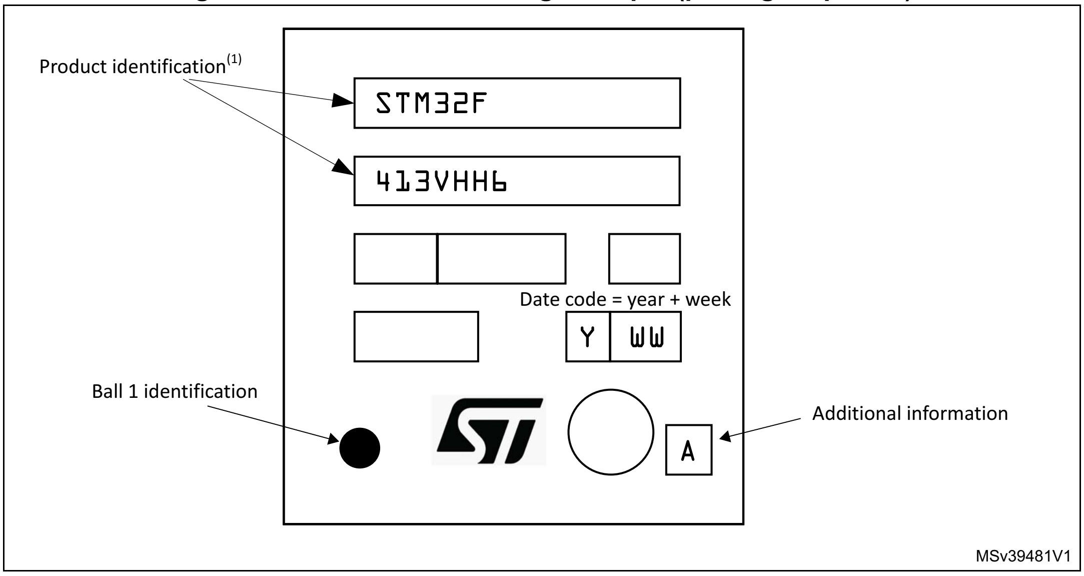

1. Drawing is not to scale.

### Device marking for UFBGA100

The following figure gives an example of topside marking and ball 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 80. UFBGA100 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| F | 0.550 | 0.600 | 0.650 | 0.0177 | 0.0197 | 0.0217 |
| ddd | - | - | 0.080 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint**

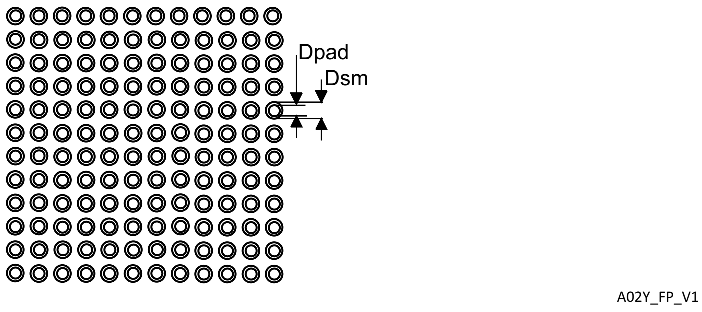



**Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.80 mm |
| Dpad | 0.400 mm |
| Dsm | 0.550 mm typ. (depends on the soldermask registration tolerance) |

*Note: Non solder mask defined (NSMD) pads are recommended.*
*4 to 6 mils solder paste screen printing process.*
*Stencil opening is 0.400 mm.*
*Stencil thickness is between 0.100 mm and 0.125 mm.*
*Pad trace width is 0.120 mm.*