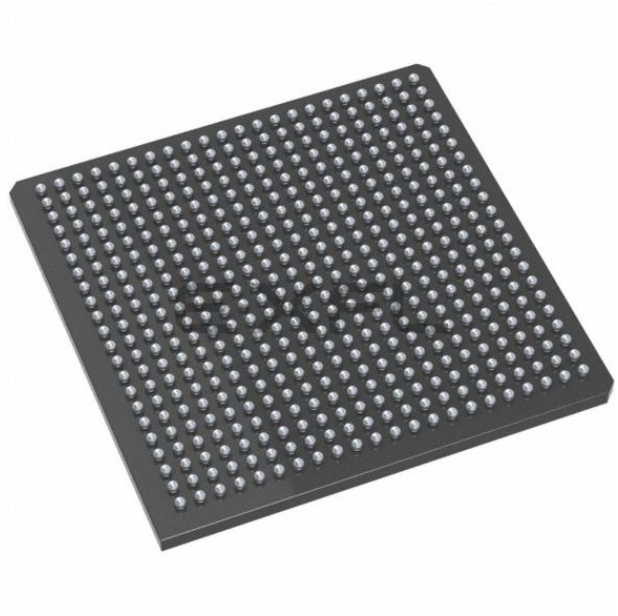
Microchip Technology - MPF100T-FCVG484E Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100t-fcvg484e

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3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

Table 13 • DC Output Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{OL} Min (V)	V_{OL} Max (V)	V_{OH} Min (V)	V_{OH} Max (V)	I_{OL}[2,6] mA	I_{OH}[2,6] mA
PCI[1]	3.15	3.3	3.45		0.1 × V_{DDI}	0.9 × V_{DDI}		1.5	0.5
LVTTL	3.15	3.3	3.45		0.4	2.4			
LVCMOS33	3.15	3.3	3.45		0.4	V_{DDI} – 0.4			
LVCMOS25	2.375	2.5	2.625		0.4	V_{DDI} – 0.4			
LVCMOS18	1.71	1.8	1.89		0.45	V_{DDI} – 0.45			
LVCMOS15	1.425	1.5	1.575		0.25 × V_{DDI}	0.75 × V_{DDI}			
LVCMOS12	1.14	1.2	1.26		0.25 × V_{DDI}	0.75 × V_{DDI}			
SSTL25I[3]	2.375	2.5	2.625		V_{TT} – 0.608	V_{TT} + 0.608		8.1	8.1
SSTL25II[3]	2.375	2.5	2.625		V_{TT} – 0.810	V_{TT} + 0.810		16.2	16.2
SSTL18I[3]	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603		6.7	6.7
SSTL18II[3]	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603		13.4	13.4
SSTL15I[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
SSTL15II[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH}) /34
SSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
SSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH}) /34
HSTL15I	1.425	1.5	1.575		0.4	V_{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V_{DDI} – 0.4		16	16

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18[5]	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18[5]	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18[5]	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSUL18I	HSUL 1.8 V Class I	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	V_{REF} – .22	V_{REF} + .22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
SLVS33	Scalable low-voltage signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
SLVS25	SLVS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
BLVDSE25[6]	Bus LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MLVDSE25[6]	Multipoint LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
LVPECLE33[6]	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
FMAX	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
FMAX	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
FMAX	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
FMAX	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
FMAX	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
FMAX	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
FMAX 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks)[2]	F_{MAXINJ}		120	1000	ps
PLL VCO frequency	F_{VCO}	800		5000	MHz
Loop bandwidth (Int)[3]	F_{BW}	F_{PHDET}/55	F_{PHDET}/44	F_{PHDET}/30	MHz
Loop bandwidth (FRAC)[3]	F_{BW}	F_{PHDET}/91	F_{PHDET}/77	F_{PHDET}/56	MHz
Static phase offset of the PLL outputs[4]	T_{SPO}			Max (±60 ps, ±0.5 degrees)	ps
	$T_{OUTJITTER}$				ps
PLL output duty cycle precision	$T_{OUTDUTY}$	48		54	%
PLL lock time[5]	T_{LOCK}			Max (6.0 µs, 625 PFD cycles)	µs
PLL unlock time[6]	T_{UNLOCK}	2		8	PFD cycles
PLL output frequency	F_{OUT}	0.050		1250	MHz
Minimum reset pulse width	T_{MRPW}				µs
Maximum delay in the feedback path[7]	F_{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread[8]	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency[9]	Mod_Freq	F_{PHDETF}/(128x63)	32	F_{PHDETF}/(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3 DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter[1]	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F_{INF}	133		800	MHz
Input feedback clock frequency	F_{INFDBF}	133		800	MHz
Primary output clock frequency	F_{OUTPF}	133		800	MHz

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2, 3]	$F_{XCVRREFCLKMAX\ CASCADE}$	20		156	20		156	MHz
Reference clock rate at the PFD[4]	$F_{TXREFCLKPFD}$	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4]	$F_{TXREFCLKPFD10G}$	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5]	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 10 KHz	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 100 KHz	$F_{TXREFPN}$			–115			–115	dBc /Hz
Phase noise at 1 MHz	$F_{TXREFPN}$			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	$T_{REFRISE}$		200	500		200	500	ps
Reference clock input fall time (90%–10%)	$T_{REFFALL}$		200	500		200	500	ps
Reference clock duty cycle	$T_{REFDUTY}$	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, se e table Differential DC Input and Output Levels.
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVCMOS25	For DC input levels, see table DC Input and Output Levels.

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115[1]		Ω
Power-up termination			>50K		Ω

1. Measured at VCM= 1.2 V and VID= 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps(–STD) / 12.7 Gbps (–1)[1]		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	Mhz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}		85		Ω	
	V_{OTERM}		100		Ω	
	V_{OTERM}		150		Ω	
Common mode voltage[1]	V_{OCM}	0.44 × V_{DDA}	0.525 × V_{DDA}	0.59 × V_{DDA}	V	DC coupled 50% setting
	V_{OCM}	0.52 × V_{DDA}	0.6 × V_{DDA}	0.66 × V_{DDA}	V	DC coupled 60% setting
	V_{OCM}	0.61 × V_{DDA}	0.7 × V_{DDA}	0.75 × V_{DDA}	V	DC coupled 70% setting
	V_{OCM}	0.63 × V_{DDA}	0.8 × V_{DDA}	0.83 × V_{DDA}	V	DC coupled 80% setting
Rise time[2]	T_{TxRF}	41		70	ps	20% to 80%
Fall time[2]		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew[3]	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew[4]	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time[7]	TTxEITrEntry				ns	
Electrical idle transition exit time[7]	TTxEITrExit				ns	
Electrical idle amplitude	VTxEIpp				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time[8]	$T_{DPLLLock}$				REFCLK UIs	
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}				UI UI	Data rate ≥8.5 Gbps to 12.7 Gbps[9] (Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥3.2 Gbps to 8.5 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥1.6 Gbps to 3.2 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.13 0.02	UI UI	Data rate ≥ 800 Mbps to 1.6 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.06 0.01	UI UI	Data rate = 250 Mbps to 800 Mbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

Table 60 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4 1GbE (1000BASE-T)

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5 SGMII and QSGMII

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6 SDI

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

		Retention Since Programmed (N = Number Digests During that Time)[1]								
Digest T_J	Storage and Operating T_J	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T_J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

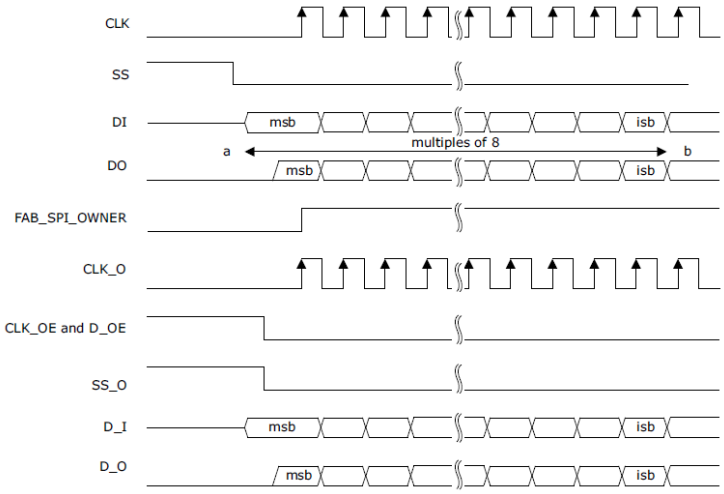
7.6.5 Digest Time

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		µs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	35	µs
	MPF300T, TL, TS, TLS	33.2	35	µs
	MPF500T, TL, TS, TLS			µs
sNVM digest run time[1]	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	46.6	48.8	µs
	MPF300T, TL, TS, TLS	46.6	48.8	µs
	MPF500T, TL, TS, TLS			µs
User key digest run time[2]	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	525.4	543.3	µs
	MPF300T, TL, TS, TLS	525.4	543.3	µs
	MPF500T, TL, TS, TLS			µs

Figure 4 • USPI Switching Characteristics



7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ[1]	Max
T_{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 µs		470 µs
T_{CONVN}	Time between subsequent channel conversions.		480 µs	
T_{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs.	0 ns		
T_{VALID}[2]	Width of the valid pulse.	1.625 µs		2 µs
T_{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 µs	Rate × 32 µs	8128 µs

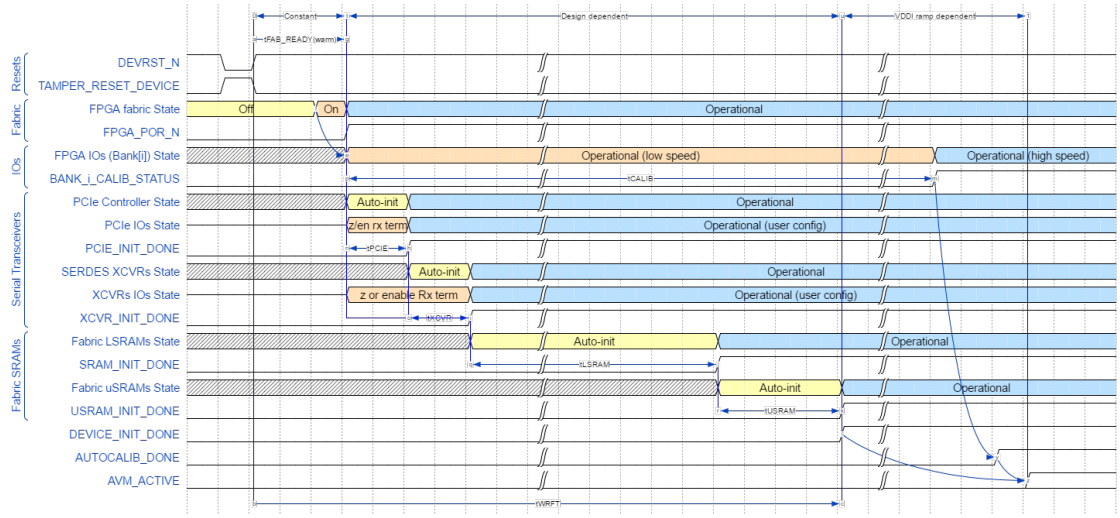
1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	–40		125	°C	
Temperature sensing accuracy	–10		10	°C	

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256[1], 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384[1], 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256[1] (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1[1]	512	2386	1579
	64K	77576	990
SHA-256[1]	512	2516	884
	64K	84752	938
SHA-384[1]	1024	4154	884
	64K	100222	938
SHA-512[1]	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384[1]	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155