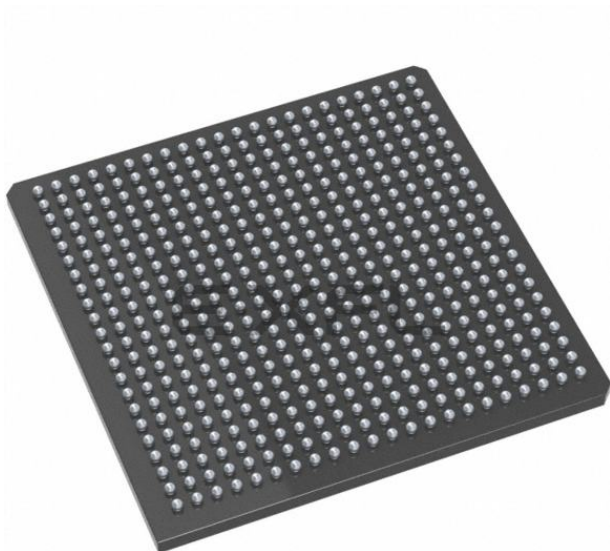




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100t-fcvg484i

Contents

1	Revision History	1
1.1	Revision 1.3	1
1.2	Revision 1.2	1
1.3	Revision 1.1	1
1.4	Revision 1.0	1
2	Overview	2
3	References	3
4	Device Offering	4
5	Silicon Status	5
6	DC Characteristics	6
6.1	Absolute Maximum Rating	6
6.2	Recommended Operating Conditions	6
6.2.1	DC Characteristics over Recommended Operating Conditions	8
6.2.2	Maximum Allowed Overshoot and Undershoot	8
6.3	Input and Output	12
6.3.1	DC Input and Output Levels	12
6.3.2	Differential DC Input and Output Levels	15
6.3.3	Complementary Differential DC Input and Output Levels	18
6.3.4	HSIO On-Die Termination	19
6.3.5	GPIO On-Die Termination	20
7	AC Switching Characteristics	22
7.1	I/O Standards Specifications	22
7.1.1	Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP	22
7.1.2	Output Delay Measurement Methodology	25
7.1.3	Input Buffer Speed	27
7.1.4	Output Buffer Speed	29
7.1.5	Maximum PHY Rate for Memory Interface IP	31
7.1.6	User I/O Switching Characteristics	32
7.2	Clocking Specifications	35
7.2.1	Clocking	35
7.2.2	PLL	36
7.2.3	DLL	37
7.2.4	RC Oscillators	38
7.3	Fabric Specifications	40
7.3.1	Math Blocks	40

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V _{IN}) Overshoot Duration as % at T _J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V _{IN}) Undershoot Duration as % at T _J = 100 °C	Condition (V)
100	-0.5
100	-0.55
100	-0.6
100	-0.65
100	-0.7
100	-0.75
100	-0.8
100	-0.85
100	-0.9
100	-0.95
100	-1
100	-1.05
100	-1.1
100	-1.15
100	-1.2
69	-1.25
45	-1.3

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM1,3} Min (V)	V _{ICM1,3} Typ (V)	V _{ICM1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18 ⁵	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18 ⁵	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18 ⁵	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

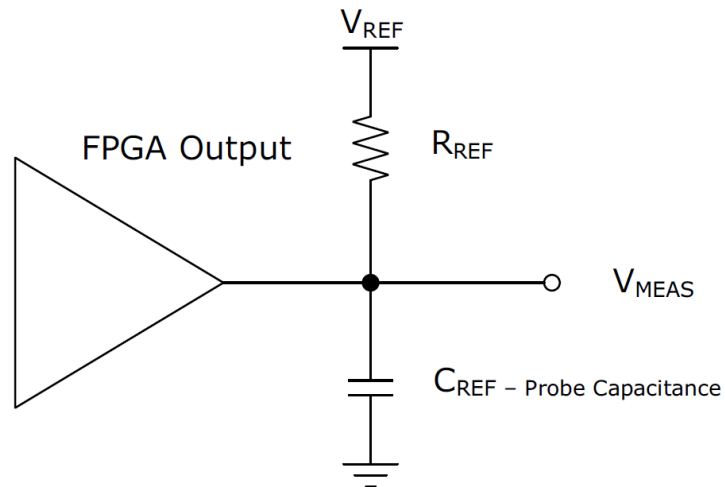
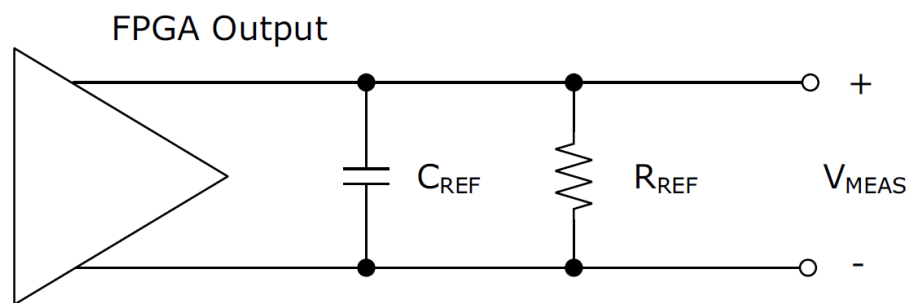
I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
HCSL25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18 ⁵	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V _{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V _{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} – 0.4 V;
 - b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
 - c. V_{ICM} – V_{ID}/2 must be >V_{SS} – 0.3 V;
 - d. Any differential input with V_{ICM} ≤ 0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. V_{DDI} = 1.8 V, V_{DDAUX} = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15 ³	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25 ³	GPIO		1.25		0.24	0.262	0.272

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
SLVS25	SLVS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
BLVDSE25 ⁶	Bus LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
MLVDSE25 ⁶	Multipoint LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
LVPECL33 ⁶	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.675	0		V

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

Figure 2 • Output Delay Measurement—Differential Test Setup


7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	-1	Unit
LVDS18	1250	1250	Mbps
RDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
F _{MAX}	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
F _{MAX}	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
F _{MAX}	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
F _{MAX}	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
F _{MAX}	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
F _{MAX}	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
F _{MAX} 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Clock-to-Data Condition
F _{MAX} 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance ¹	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Global clock F _{MAX}	F _{MAXG}	500	500	500	500	MHz	
Regional clock F _{MAX}	F _{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F _{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T _{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	μA
Operating current (V_{DD})	RC_{SCVDD}			60.7	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, see table Differential DC Input and Output Levels .
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVC MOS25	For DC input levels, see table DC Input and Output Levels .

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115 ¹		Ω
Power-up termination			>50K		Ω

1. Measured at V_{CM} = 1.2 V and V_{ID} = 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver TX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver RX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see [UG0677: PolarFire FPGA Transceiver User Guide](#).

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps ¹			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps ¹			UI

- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	34.9	μs
	MPF300T, TL, TS, TLS	33.2	34.9	μs
	MPF500T, TL, TS, TLS			μs
Factory digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	493.6	510.1	μs
	MPF300T, TL, TS, TLS	493.6	510.1	μs
	MPF500T, TL, TS, TLS			μs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

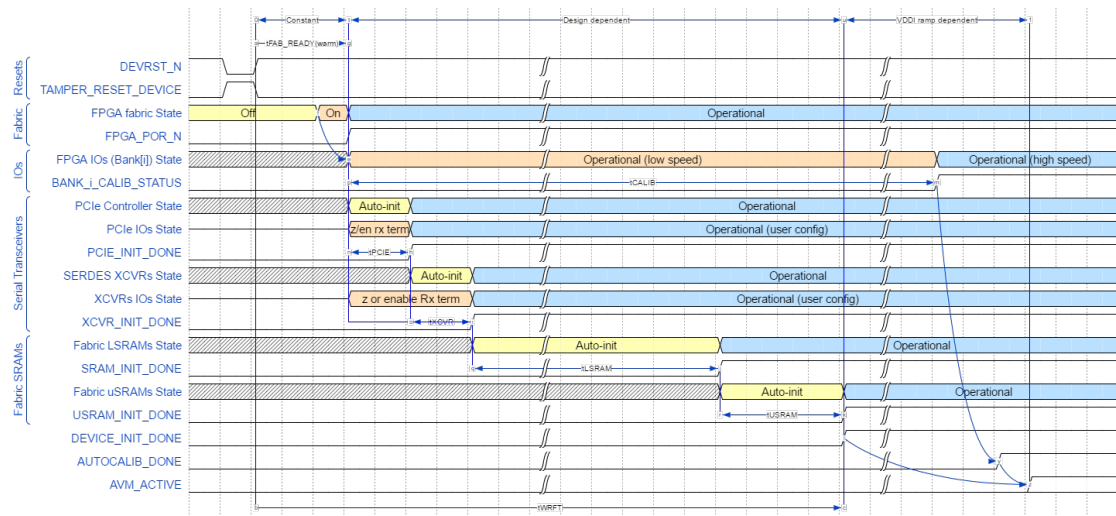
Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1, 3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1, 4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1, 2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1, 3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ^{1, 4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F _{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T _{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T _{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR _{RAMP}		10		μs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR _{ASSERT}	1			μs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	DR _{DEASSERT}	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF _{RAMP}		10		μs	
Minimum FF_EXIT_N assert time	FF _{ASSERT}	1			μs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	FF _{DEASSERT}	170			μs	The minimum time FF_EXIT_N needs to be de-asserted before assertion