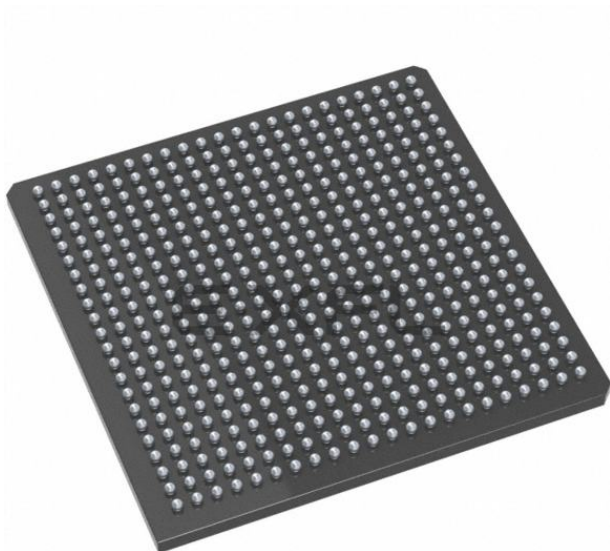




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100tls-fcg484i

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5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Preliminary
MPF200T, TL, TS, TLS	Preliminary
MPF300T, TL, TS, TLS	Preliminary
MPF500T, TL, TS, TLS	Preliminary

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	−0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	−0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	−0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	−0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	−0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	−0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	−0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	−0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	−0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	−0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	−0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	−0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	−0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	−0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	−0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	−65	150	°C
Junction temperature ¹	T _J	−55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V _{IN}) Overshoot Duration as % at T _J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V _{IN}) Undershoot Duration as % at T _J = 100 °C	Condition (V)
100	-0.5
100	-0.55
100	-0.6
100	-0.65
100	-0.7
100	-0.75
100	-0.8
100	-0.85
100	-0.9
100	-0.95
100	-1
100	-1.05
100	-1.1
100	-1.15
100	-1.2
69	-1.25
45	-1.3

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18 ⁵	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18 ⁵	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18 ⁵	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
MLVDSSE25 ³	GPIO		1.25		0.396	0.442	0.453
LVPECL33 ³	GPIO		1.65		0.664	0.722	0.755
MIPIE25 ³	GPIO		0.25		0.1	0.22	0.3

1. V_{OCM} is the output common mode voltage.
2. V_{OD} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} - 0.4V;
 - b. V_{ICM} + V_{ID}/2 must be < V_{DDI} + 0.4 V;
 - c. V_{ICM} - V_{ID}/2 must be > V_{SS} - 0.3 V.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance ¹	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Global clock F _{MAX}	F _{MAXG}	500	500	500	500	MHz	
Regional clock F _{MAX}	F _{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F _{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T _{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter ¹	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency ²	F _{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F _{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	T _{OUTJITTERP}			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T _{SKEW}			±200	ps
DLL lock time	T _{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T _{MRPW}	3			ns
Minimum input pulse width ³	T _{MIPW}	20			ns
Minimum input clock pulse width high	T _{MPWH}	400			ps
Minimum input clock pulse width low	T _{MPWL}	400			ps
Delay step size	T _{DEL}	12.7	30	35	ps
Maximum delay block delay ⁴	T _{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input) ⁵	T _{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode) ⁵	T _{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4

RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{2FREQ}		2		MHz
Accuracy	RC _{2FACC}	−4		4	%
Duty cycle	RC _{2DC}	46		54	%
Peak-to-peak output period jitter	RC _{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC _{2CJIT}		5	10	ns
Operating current (V _{DD25})	RC _{2IVPPA}			60	μA
Operating current (V _{DD})	RC _{2IVDD}			2.6	μA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{SCFREQ}		160		MHz
Accuracy	RC _{SCFACC}	−4		4	%
Duty cycle	RC _{SCDC}	47		52	%
Peak-to-peak output period jitter	RC _{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC _{SCCJIT}			172	ps
Operating current (V _{DD25})	RC _{SCVPPA}			599	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate ^{1, 2, 3}	F _{XCVRREFCLKMAX} CASCADE	20		156	20		156	MHz
Reference clock rate at the PFD ⁴	F _{TXREFCLKPFD}	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above ⁴	F _{TXREFCLKPFD10G}	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input) ⁵	F _{TXREFPN}			–110			–110	dBc /Hz
Phase noise at 10 KHz	F _{TXREFPN}			–110			–110	dBc /Hz
Phase noise at 100 KHz	F _{TXREFPN}			–115			–115	dBc /Hz
Phase noise at 1 MHz	F _{TXREFPN}			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	T _{REFRISE}		200	500		200	500	ps
Reference clock input fall time (90%–10%)	T _{REFFALL}		200	500		200	500	ps
Reference clock duty cycle	T _{REFDUTY}	40		60	40		60	%
Spread spectrum modulation spread ⁶	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency ⁷	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual F_{TxRefClkPFD} value by $20 \times \log_{10} (\text{TxRefClkPFD} / 156 \text{ MHz})$. It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps ⁵
		0.41			UI	>1.6 to 3.2 Gbps ⁵
		0.41			UI	>0.8 to 1.6 Gbps ⁵
		0.41			UI	250 to 800 Mbps ⁵
Total jitter tolerance with stressed eye	T _{TJOLSE}	0.65			UI	3.125 Gbps ⁵
		0.65			UI	6.25 Gbps ⁶
		0.7			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
Sinusoidal jitter tolerance with stressed eye	T _{SJTOLSE}	0.1			UI	3.125 Gbps ⁵
		0.05			UI	6.25 Gbps ⁶
		0.05			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

- Valid at 3.2 Gbps and below.
- Data vs. Rx reference clock frequency.
- Achieves compliance with PCIe electrical idle detection.
- Achieves compliance with SATA OOB specification.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

Table 60 • 10GbE (RXAU)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4**1GbE (1000BASE-T)**

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5**SGMII and QSGMII**

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6**SDI**

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

Retention Since Programmed (N = Number Digests During that Time) ¹										
Digest T _i	Storage and Operating T _j	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T _{SNVM_Rd}	18H				Note 1
Digital signature service raw	T _{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T _{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	T _{Challenge}	20H	1.8	2.0	ms	
Nonce service	T _{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	T _{BIT_AUTH}	22H				Note 4
IAP Image authentication	T _{IAP_AUTH}	23H				Note 4
Reserved		26H–3FH				
In application programming by index	T _{IAP_Prg_Index}	42H				Note 2
In application programming by SPI address	T _{IAP_Prg_Addr}	43H				Note 2
In application verify by index	T _{IAP_Ver_Index}	44H				Note 5
In application verify by SPI address	T _{IAP_Ver_Addr}	45H				Note 5
Auto update	T _{AutoUpdate}	46H				Note 2
Digest check	T _{digest_chk}	47H				Note 3

1. See [sNVM Read/Write Characteristics](#) (see page 58).
2. See [SPI Master Programming Time](#) (see page 52).
3. See [Digest Times](#) (see page 54).
4. See [Authentication Services Time](#) (see page 58).
5. See [Verify Services Time](#) (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

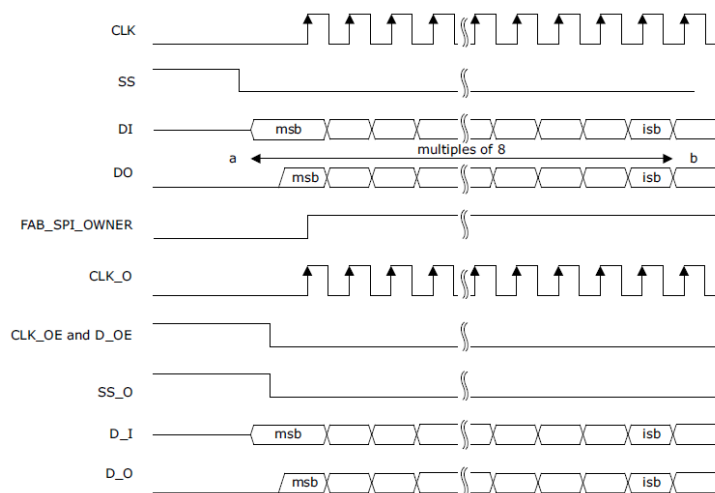
This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}			25	MHz	

Figure 4 • USPI Switching Characteristics

7.8.4

Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

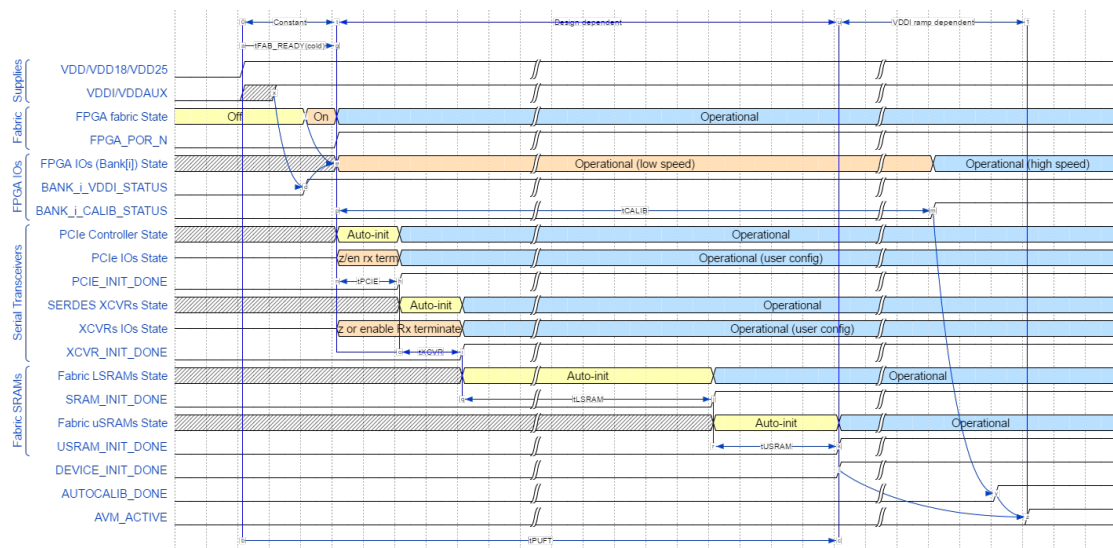
1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	

Figure 5 • Cold Reset Timing

**Notes:**

- The previous diagram shows the case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
 - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
 - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
 - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2**Warm Reset Initialization Sequence**

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 ¹ , 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384 ¹ , 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256 ¹ (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 ¹	512	2386	1579
	64K	77576	990
SHA-256 ¹	512	2516	884
	64K	84752	938
SHA-384 ¹	1024	4154	884
	64K	100222	938
SHA-512 ¹	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384 ¹	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155