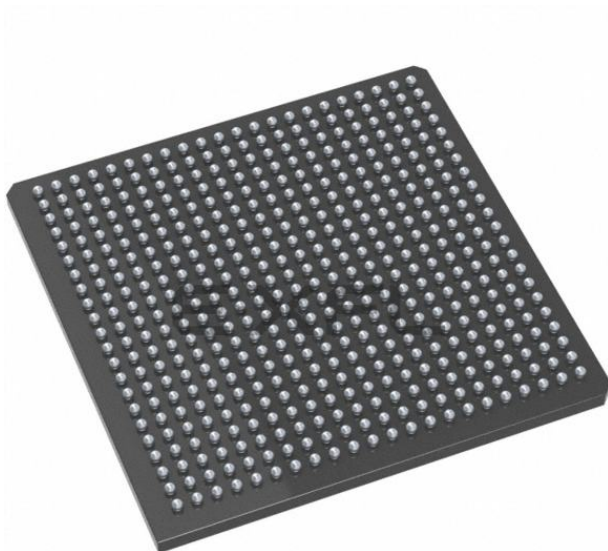




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Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100tls-fcvg484i

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2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance ¹	C _{IN} (dedicated GPIO)		5.6	pf	
	C _{IN} (GPIO)		5.6	pf	
	C _{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I _L (GPIO)		10	μA	I/O disabled, high – Z
	I _L (HSIO)		10	μA	I/O disabled, high – Z
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}	T _{RISE}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}	T _{FALL}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Pad pull-up when V _{IN} = 0 ⁵	I _{PU}	137	220	μA	V _{DDIX} = 3.3 V
Pad pull-up when V _{IN} = 0 ⁵		102	166	μA	V _{DDIX} = 2.5 V
Pad pull-up when V _{IN} = 0		68	115	μA	V _{DDIX} = 1.8 V
Pad pull-up when V _{IN} = 0		51	88	μA	V _{DDIX} = 1.5 V
Pad pull-up when V _{IN} = 0 ⁶		29	73	μA	V _{DDIX} = 1.35 V
Pad pull-up when V _{IN} = 0	I _{PD}	16	46	μA	V _{DDIX} = 1.2 V
Pad pull-down when V _{IN} = 3.3 V ⁵		65	187	μA	V _{DDIX} = 3.3 V
Pad pull-down when V _{IN} = 2.5 V ⁵		63	160	μA	V _{DDIX} = 2.5 V
Pad pull-down when V _{IN} = 1.8 V		60	117	μA	V _{DDIX} = 1.8 V
Pad pull-down when V _{IN} = 1.5 V		57	95	μA	V _{DDIX} = 1.5 V
Pad pull-down when V _{IN} = 1.35 V		52	86	μA	V _{DDIX} = 1.35 V
Pad pull-down when V _{IN} = 1.2 V		47	79	μA	V _{DDIX} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section [Recommended Operating Conditions](#) (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V _{DD}	0.2	50	ms
Transceiver core supply	V _{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V _{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V _{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V _{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	V _{DDI} [0,1,6,7]	0.2	50	ms
GPIO bank I/O power supplies	V _{DDI} [2,4,5]	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V _{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	V _{DDAUX} [2,4,5]	0.2	50	ms
Transceiver reference clock supply	V _{DD_XCVR_CLK}	0.2	50	ms
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended) ^{1, 2}	XCVR _{RX_HS}			±4	mA	V _{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended) ³	XCVR _{TX_HS}			±10	mA	V _{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended) ⁴	XCVR _{REF_HS}			±1	mA	V _{DD_XCVR_CLK} = 0 V
Current per GPIO pin (P or N single-ended) ⁵	I _{GPIO_HS}			±1	mA	V _{DDI_X} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

- Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
- Each P and N transceiver input has less than the specified maximum input current.
- Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
- V_{DD_XCVR_CLK} is powered down and the device is driven to –0.3 V < V_{IN} < V_{DD_XCVR_CLK}.
- V_{DDI_X} is powered down and the device is driven to –0.3 V < V_{IN} < GPIO V_{DDI_{max}}.

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to $V_{SS}^{4,5}$	Internal	-20	120	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$
	parallel termination to V_{SS}	-20	240	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} .
3. For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.
4. Measured at 50% of V_{DDI} .
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSTL135II	Differential HSTL 1.35 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H . All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in [Output Delay Measurement—Single-Ended Test Setup](#) (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCI 3.3 V	25	10	1.65	
LVTTTL33	LVTTTL 3.3 V	1M	0	1.65	
LVC MOS33	LVC MOS 3.3 V	1M	0	1.65	
LVC MOS25	LVC MOS 2.5 V	1M	0	1.25	
LVC MOS18	LVC MOS 1.8 V	1M	0	0.90	
LVC MOS15	LVC MOS 1.5 V	1M	0	0.75	
LVC MOS12	LVC MOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T _{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F _{MAX}	F _{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew ¹	F _{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F _{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F _{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F _{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion ²	T _{DCB}	90	90	90	90	ps	HSIO without bridging
	T _{DCB}	115	115	115	115	ps	HSIO with bridging
	T _{DCB}	90	90	90	90	ps	GPIO without bridging
	T _{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2

PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F _{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F _{INF}	10		1250	MHz
Minimum reference or feedback pulse width ¹	F _{INPULSE}	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F _{PHDET1}	1		312	MHz
Frequency at the PFD (fractional mode)	F _{PHDET2}	10	50	125	MHz
Allowable input duty cycle	F _{INDUTY}	25		75	%

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, see table Differential DC Input and Output Levels .
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVC MOS25	For DC input levels, see table DC Input and Output Levels .

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115 ¹		Ω
Power-up termination			>50K		Ω

1. Measured at V_{CM} = 1.2 V and V_{ID} = 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver TX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps ⁵
		0.41			UI	>1.6 to 3.2 Gbps ⁵
		0.41			UI	>0.8 to 1.6 Gbps ⁵
		0.41			UI	250 to 800 Mbps ⁵
Total jitter tolerance with stressed eye	T _{TJOLSE}	0.65			UI	3.125 Gbps ⁵
		0.65			UI	6.25 Gbps ⁶
		0.7			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
Sinusoidal jitter tolerance with stressed eye	T _{SJTOLSE}	0.1			UI	3.125 Gbps ⁵
		0.05			UI	6.25 Gbps ⁶
		0.05			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

- Valid at 3.2 Gbps and below.
- Data vs. Rx reference clock frequency.
- Achieves compliance with PCIe electrical idle detection.
- Achieves compliance with SATA OOB specification.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps ¹			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps ¹			UI

- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	34.9	μs
	MPF300T, TL, TS, TLS	33.2	34.9	μs
	MPF500T, TL, TS, TLS			μs
Factory digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	493.6	510.1	μs
	MPF300T, TL, TS, TLS	493.6	510.1	μs
	MPF500T, TL, TS, TLS			μs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1, 3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1, 4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1, 2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1, 3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ^{1, 4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	μs	
Authenticated and decrypted text read		159.59	160.53	166.5	μs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	μs	
User code	T_{User}	01H	0.8	1.05	μs	
Design information	T_{Design}	02H	2.4	2.7	μs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	μs	
Query security locks	T_{sec_Query}	05H	15	17	μs	
Read debug information	T_{Rd_debug}	06H	34	38	μs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM_Wr_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM_Wr_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM_Wr_Cipher}$	12H				Note 1
Reserved		13H–17H				

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T _{SNVM_Rd}	18H				Note 1
Digital signature service raw	T _{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T _{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	T _{Challenge}	20H	1.8	2.0	ms	
Nonce service	T _{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	T _{BIT_AUTH}	22H				Note 4
IAP Image authentication	T _{IAP_AUTH}	23H				Note 4
Reserved		26H–3FH				
In application programming by index	T _{IAP_Prg_Index}	42H				Note 2
In application programming by SPI address	T _{IAP_Prg_Addr}	43H				Note 2
In application verify by index	T _{IAP_Ver_Index}	44H				Note 5
In application verify by SPI address	T _{IAP_Ver_Addr}	45H				Note 5
Auto update	T _{AutoUpdate}	46H				Note 2
Digest check	T _{digest_chk}	47H				Note 3

1. See [sNVM Read/Write Characteristics](#) (see page 58).
2. See [SPI Master Programming Time](#) (see page 52).
3. See [Digest Times](#) (see page 54).
4. See [Authentication Services Time](#) (see page 58).
5. See [Verify Services Time](#) (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

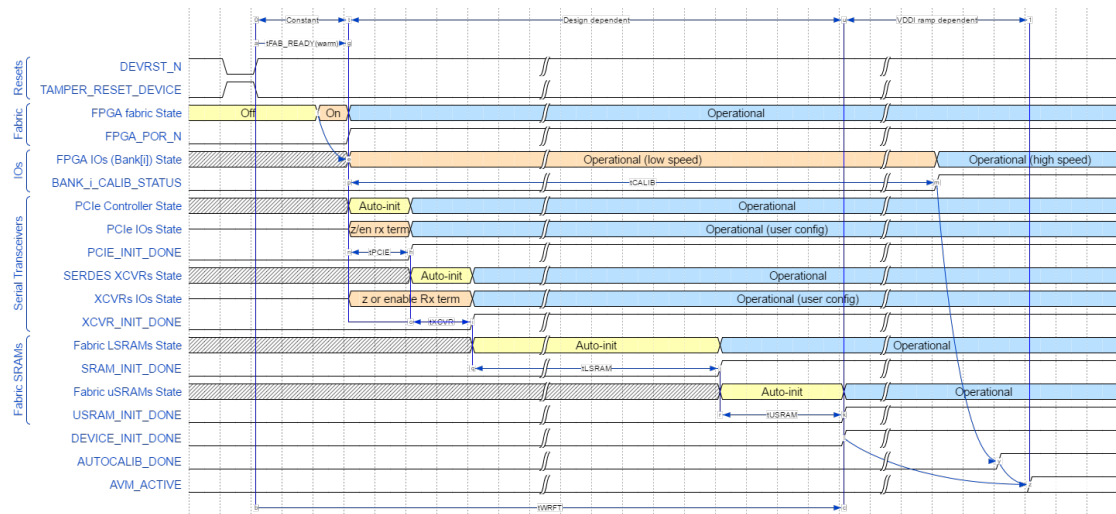
7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}			25	MHz	

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F _{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T _{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T _{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR _{RAMP}		10		μs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR _{ASSERT}	1			μs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	DR _{DEASSERT}	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF _{RAMP}		10		μs	
Minimum FF_EXIT_N assert time	FF _{ASSERT}	1			μs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	FF _{DEASSERT}	170			μs	The minimum time FF_EXIT_N needs to be de-asserted before assertion