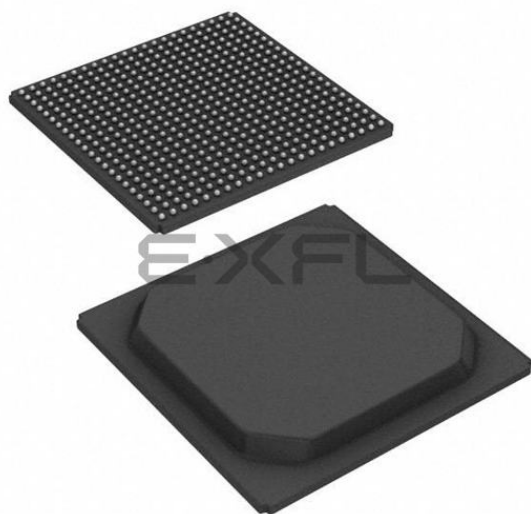




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100ts-1fcvg484i

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see [System Services \(see page 59\)](#).
- The Non-Volatile Characteristics section was updated. For more information, see [Non-Volatile Characteristics \(see page 51\)](#).
- The Fabric Macros section was updated. For more information, see [Fabric Macros \(see page 60\)](#).
- The Transceiver Switching Characteristics section was updated. For more information, see [Transceiver Switching Characteristics \(see page 42\)](#).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see [HSIO Maximum Input Buffer Speed](#) and [HSIO Maximum Output Buffer Speed](#).
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see [I/O Standards Specifications](#).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see [Non-Volatile Characteristics](#).
- A note was added defining power down conditions for programming recovery conditions. For more information, see [Power-Supply Ramp Times](#).

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	−0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	−0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	−0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	−0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	−0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	−0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	−0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	−0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	−0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	−0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	−0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	−0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	−0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	−0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	−0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	−65	150	°C
Junction temperature ¹	T _J	−55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	−0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTL	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	−0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

Min (%)	Typ	Max (%)	Unit	Condition
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} . For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
-20	34	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	40	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	48	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	80	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 80% of V_{DDI} .

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
-20	120	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 50% of V_{DDI} .

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination ¹	Internal differential termination	-20	100	20	Ω	$V_{ICM} < 0.8\text{ V}$
		-20	100	40	Ω	$0.6\text{ V} < V_{ICM} < 1.65\text{ V}$
		-20	100	80	Ω	$1.4\text{ V} < V_{ICM}$
Single-ended thevenin termination ^{2, 3}	Internal parallel thevenin termination	-40	50	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
		-40	75	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-40	150	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-20	20	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	30	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	40	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	60	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	120	20	Ω	$V_{DDI} = 1.5\text{ V}$

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
PCI	PCIE 3.3 V	0	VDDI			VDDI/2		V
LVTTTL33	LVTTTL 3.3 V	0	VDDI			VDDI/2		V
LVCNOS33	LVCNOS 3.3 V	0	VDDI			VDDI/2		V
LVCNOS25	LVCNOS 2.5 V	0	VDDI			VDDI/2		V
LVCNOS18	LVCNOS 1.8 V	0	VDDI			VDDI/2		V
LVCNOS15	LVCNOS 1.5 V	0	VDDI			VDDI/2		V
LVCNOS12	LVCNOS 1.2 V	0	VDDI			VDDI/2		V
SSTL25I	SSTL 2.5 V Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	1.25	V
SSTL25II	SSTL 2.5 V Class II	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	1.25	V
SSTL18I	SSTL 1.8 V Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	0.90	V
SSTL18II	SSTL 1.8 V Class II	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	0.90	V
SSTL15I	SSTL 1.5 V Class I	$V_{REF} - .175$	$V_{REF} + .175$			V_{REF}	0.75	V
SSTL15II	SSTL 1.5 V Class II	$V_{REF} - .175$	$V_{REF} + .175$			V_{REF}	0.75	V
SSTL135I	SSTL 1.35 V Class I	$V_{REF} - .16$	$V_{REF} + .16$			V_{REF}	0.675	V
SSTL135II	SSTL 1.35 V Class II	$V_{REF} - .16$	$V_{REF} + .16$			V_{REF}	0.675	V
HSTL15I	HSTL 1.5 V Class I	$V_{REF} - .5$	$V_{REF} + .5$			V_{REF}	0.75	V
HSTL15II	HSTL 1.5 V Class II	$V_{REF} - .5$	$V_{REF} + .5$			V_{REF}	0.75	V
HSTL135I	HSTL 1.35 V Class I	$V_{REF} - 0.45$	$V_{REF} + .45$			V_{REF}	0.675	V
HSTL135II	HSTL 1.35 V Class II	$V_{REF} - .45$	$V_{REF} + .45$			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	$V_{REF} - .4$	$V_{REF} + .4$			V_{REF}	0.60	V

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSUL18I	HSUL 1.8 V Class I	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	$V_{REF} -$.22	$V_{REF} +$.22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
SLVS33	Scalable low- voltage signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMD525/LCMD533	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T _{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F _{MAX}	F _{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew ¹	F _{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F _{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F _{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F _{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion ²	T _{DCB}	90	90	90	90	ps	HSIO without bridging
	T _{DCB}	115	115	115	115	ps	HSIO with bridging
	T _{DCB}	90	90	90	90	ps	GPIO without bridging
	T _{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2

PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F _{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F _{INF}	10		1250	MHz
Minimum reference or feedback pulse width ¹	F _{INPULSE}	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F _{PHDET1}	1		312	MHz
Frequency at the PFD (fractional mode)	F _{PHDET2}	10	50	125	MHz
Allowable input duty cycle	F _{INDUTY}	25		75	%

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	μA
Operating current (V_{DD})	RC_{SCVDD}			60.7	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

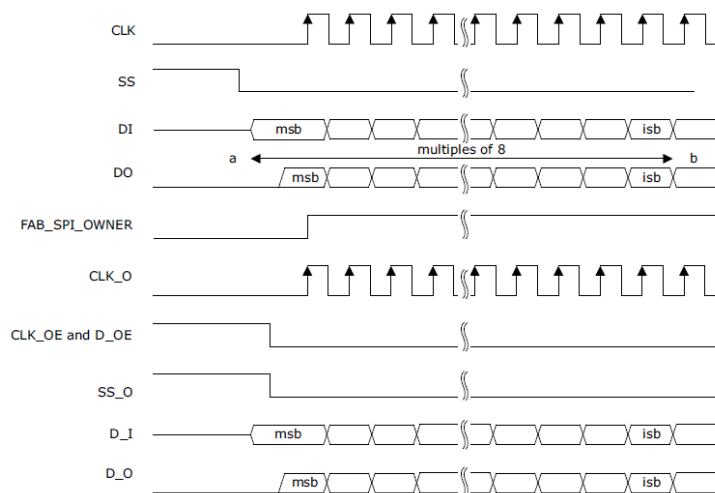
5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
FTxRefClk = 75 MHz with typical settings.
For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		$V_{DDA} + 0.3$	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC}^1	$0.7 \times V_{DDA}$		$0.9 \times V_{DDA}$	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance ²	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high) ⁹	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low) ⁹	$V_{DETLLOW}$	65		175	mV	Setting = PCIe ^{3,7}
	$V_{DETLLOW}$	95		190	mV	Setting = SATA ^{4,8}
	$V_{DETLLOW}$	75		170	mV	Setting = 1
	$V_{DETLLOW}$	95		185	mV	Setting = 2
	$V_{DETLLOW}$	100		190	mV	Setting = 3
	$V_{DETLLOW}$	140		210	mV	Setting = 4
	$V_{DETLLOW}$	155		240	mV	Setting = 5
	$V_{DETLLOW}$	165		245	mV	Setting = 6
	$V_{DETLLOW}$	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJITOL}				UI	>8.5 Gbps – 12.7 Gbps ^{5, 10}

Figure 4 • USPI Switching Characteristics

7.8.4

Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	-1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

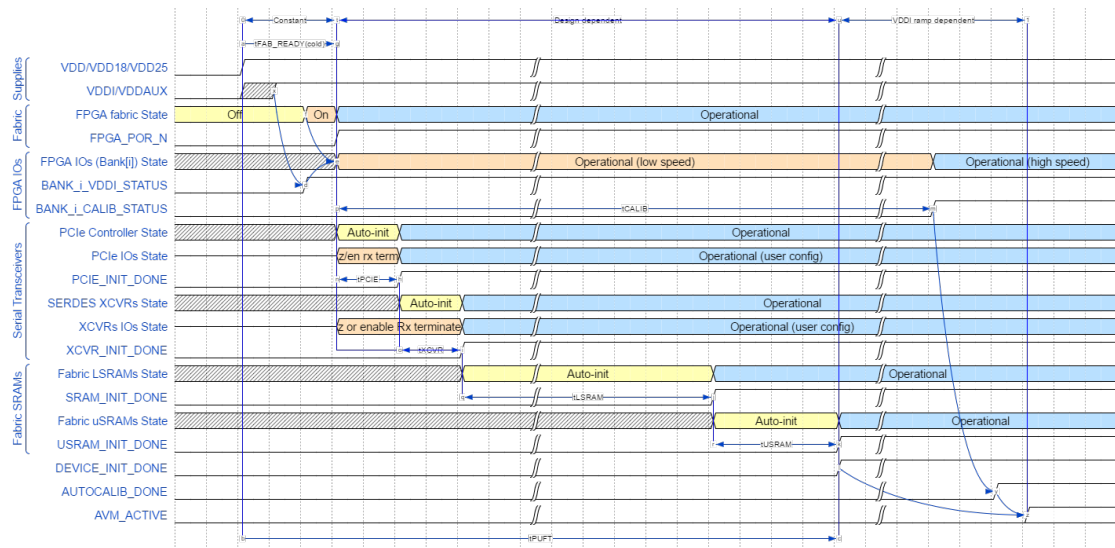
Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T _{JTAG_ACTIVE} ^{1, 2}	45	52	ns
	T _{MESH_ERR} ²	1.8	2.2	μs
	T _{CLK_GLITCH} ^{1, 2}			ns
	T _{CLK_FREQ} ^{1, 2}			μs
	T _{LOW_1P05} ²	70	108	μs
	T _{HIGH_1P8} ²	85	120	μs
	T _{HIGH_2P5} ²	130	520	μs
	T _{GLITCH_1P05} ²			μs
	T _{SECDEC} ^{1, 2}			μs
	T _{DRI_ERR} ²	14	18	μs
	T _{WDOG} ^{1, 2}			μs
	T _{LOCK_ERR} ²			μs
Time from system controller instruction execution to flag generation	T _{INST_BUF_ACCESS} ^{2, 3}	4	5	μs
	T _{INST_DEBUG} ^{2, 3}	3.3	4	μs
	T _{INST_CHK_DIGEST} ^{2, 3}	1.8	3	μs
	T _{INST_EC_SETUP} ^{2, 3}	1.8	2	μs
	T _{INST_FACT_PRIV} ^{2, 3}	3.8	5	μs
	T _{INST_KEY_VAL} ^{2, 3}	2.5	3.1	μs
	T _{INST_MISC} ^{2, 3}	1.5	2	μs
	T _{INST_PASSCODE_MATCH} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_SETUP} ^{2, 3}	4.2	5	μs
	T _{INST_PROG} ^{2, 3}	3.8	4.1	μs
	T _{INST_PUB_INFO} ^{2, 3}	4	4.5	μs
	T _{INST_ZERO_RECO} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_FAIL} ^{2, 3}	170	180	μs
	T _{INST_KEY_VAL_FAIL} ^{2, 3}	92	110	μs
	T _{INST_UNUSED} ^{2, 3}	4	5	μs
Time from sending the CLEAR to deassertion on FLAG	T _{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	T _{IO_DISABLE}	40	50	ns

Figure 5 • Cold Reset Timing

**Notes:**

- The previous diagram shows the case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
 - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
 - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
 - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2**Warm Reset Initialization Sequence**

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T _{FAB_READY} to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T _{FAB_READY} to auto-update start			T _{PUF_OVHD} ¹	T _{PUF_OVHD} ¹	ms	
The time from T _{FAB_READY} to programming recovery start			T _{PUF_OVHD} ¹	T _{PUF_OVHD} ¹	ms	
The time from T _{FAB_READY} to the tamper flags being available	T _{TAMPER_READY}	0	0	0	ms	
The time from T _{FAB_READY} to the Athena Crypto co-processor being available (for S devices only)	T _{CRYPTO_READY}	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to T_{PUF_OVHD} at section [Secure NVM Performance](#) (see page 58).

7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in [I/O-Related Supplies](#) (see page 66).

Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

Note: In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash*Freeze Mode and to exit Flash*Freeze mode.

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F _{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T _{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T _{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR _{RAMP}		10		μs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR _{ASSERT}	1			μs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	DR _{DEASSERT}	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF _{RAMP}		10		μs	
Minimum FF_EXIT_N assert time	FF _{ASSERT}	1			μs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	FF _{DEASSERT}	170			μs	The minimum time FF_EXIT_N needs to be de-asserted before assertion