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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	109000
Total RAM Bits	7782400
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-LFBGA, FCBGA
Supplier Device Package	325-FCBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf100ts-fcsg325i

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V_{DD}	–0.5	1.13	V
Transceiver Tx and Rx lanes supply	V_{DDA}	–0.5	1.13	V
Programming and HSIO receiver supply	V_{DD18}	–0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	–0.5	2.7	V
Transceiver PLL high-voltage supply	V_{DDA25}	–0.5	2.7	V
Transceiver reference clock supply	$V_{DD\_XCVR\_CLK}$	–0.5	3.6	V
Global V_{REF} for transceiver reference clocks	$XCVR_{VREF}$	–0.5	3.6	V
HSIO DC I/O supply[2]	V_{DDIx}	–0.5	2.0	V
GPIO DC I/O supply[2]	V_{DDIx}	–0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V_{DDI3}	–0.5	3.6	V
GPIO auxiliary power supply for I/O bank x[2]	V_{DDAUXx}	–0.5	3.6	V
Maximum DC input voltage on GPIO	V_{IN}	–0.5	3.8	V
Maximum DC input voltage on HSIO	V_{IN}	–0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V_{IN}	–0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V_{IN}	–0.5	3.6	V
Storage temperature (ambient)[1]	T_{STG}	–65	150	°C
Junction temperature[1]	T_J	–55	135	°C
Maximum soldering temperature RoHS	$T_{SOLROHS}$		260	°C
Maximum soldering temperature leaded	T_{SOLPB}		220	°C

1. See FPGA Programming Cycles vs Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode[1]	V_{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode[1]	V_{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less)[1]	V_{DDA}	0.97	1.00	1.03	V

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V_{IN}) Undershoot Duration as % at T_J = 100 °C	Condition (V)
100	–0.5
100	–0.55
100	–0.6
100	–0.65
100	–0.7
100	–0.75
100	–0.8
100	–0.85
100	–0.9
100	–0.95
100	–1
100	–1.05
100	–1.1
100	–1.15
100	–1.2
69	–1.25
45	–1.3

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
HCSL25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18[5]	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V_{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V_{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} – 0.4 V;
   b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
   c. V_{ICM} – V_{ID}/2 must be >VSS – 0.3 V;
   d. Any differential input with V_{ICM} ≤0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15[3]	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25[3]	GPIO		1.25		0.24	0.262	0.272

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSUL18I	HSUL 1.8 V Class I	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	V_{REF} – .22	V_{REF} + .22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
SLVS33	Scalable low-voltage signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
SLVS25	SLVS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
BLVDSE25[6]	Bus LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MLVDSE25[6]	Multipoint LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
LVPECLE33[6]	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3,4]	V_{REF}[1,5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

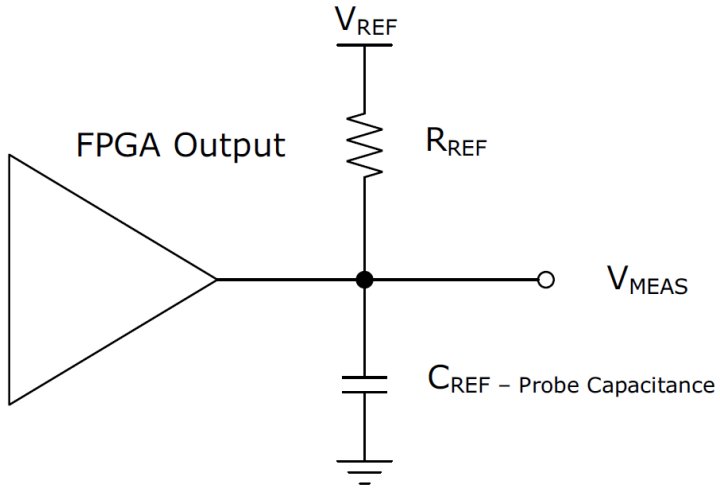
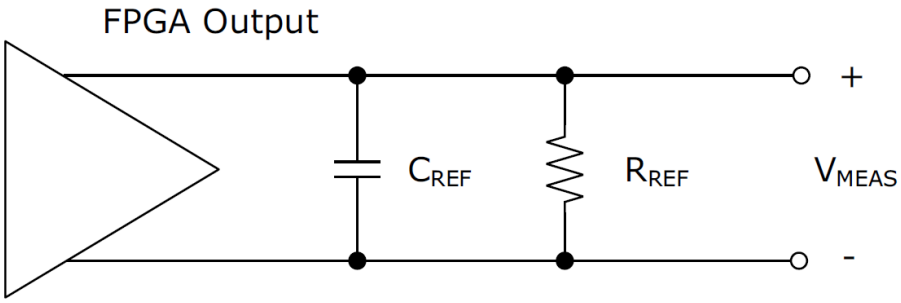


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter[1]	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency[2]	F_{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F_{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	$T_{OUTJITTERP}$			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T_{SKEW}			±200	ps
DLL lock time	T_{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T_{MRPW}	3			ns
Minimum input pulse width[3]	T_{MIPW}	20			ns
Minimum input clock pulse width high	T_{MPWH}	400			ps
Minimum input clock pulse width low	T_{MPWL}	400			ps
Delay step size	T_{DEL}	12.7	30	35	ps
Maximum delay block delay[4]	T_{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input)[5]	T_{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode)[5]	T_{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{2FREQ}		2		MHz
Accuracy	RC_{2FACC}	–4		4	%
Duty cycle	RC_{2DC}	46		54	%
Peak-to-peak output period jitter	RC_{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC_{2CJIT}		5	10	ns
Operating current (V_{DD25})	RC_{2IVPPA}			60	µA
Operating current (V_{DD})	RC_{2IVDD}			2.6	µA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{SCFREQ}		160		MHz
Accuracy	RC_{SCFACC}	–4		4	%
Duty cycle	RC_{SCDC}	47		52	%
Peak-to-peak output period jitter	RC_{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{SCCJIT}			172	ps
Operating current (V_{DD25})	RC_{SCVPPA}			599	µA

Table 44 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 45 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1,2]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled[2]	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[3]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode[2]	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode[2]	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, se e table Differential DC Input and Output Levels.
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVCMOS25	For DC input levels, see table DC Input and Output Levels.

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115[1]		Ω
Power-up termination			>50K		Ω

1. Measured at VCM= 1.2 V and VID= 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps(–STD) / 12.7 Gbps (–1)[1]		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

		Retention Since Programmed (N = Number Digests During that Time)[1]								
Digest T_J	Storage and Operating T_J	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	$T_{IAP\_Ver\_Index}$	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	$T_{IAP\_Ver\_Addr}$	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T_{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T_{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			

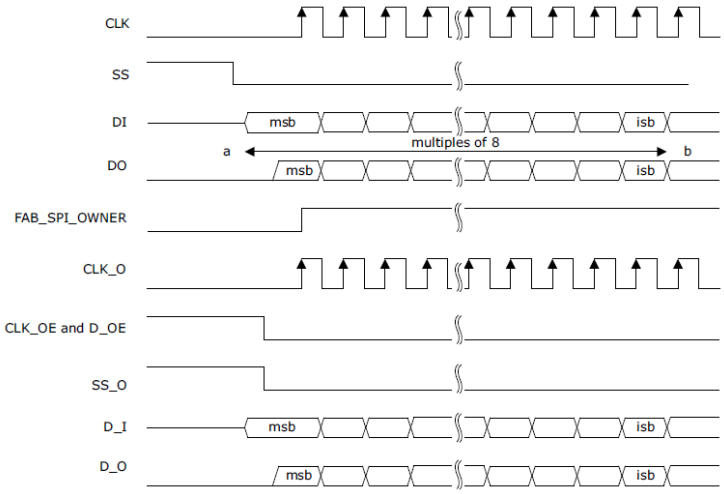
7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T_{PUF_OVHD}		100	111	ms	From T_{FAB_READY}
Plain text read		7.67	7.79	8.2	µs	

Figure 4 • USPI Switching Characteristics



7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ[1]	Max
T_{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 µs		470 µs
T_{CONVN}	Time between subsequent channel conversions.		480 µs	
T_{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs.	0 ns		
T_{VALID}[2]	Width of the valid pulse.	1.625 µs		2 µs
T_{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 µs	Rate × 32 µs	8128 µs

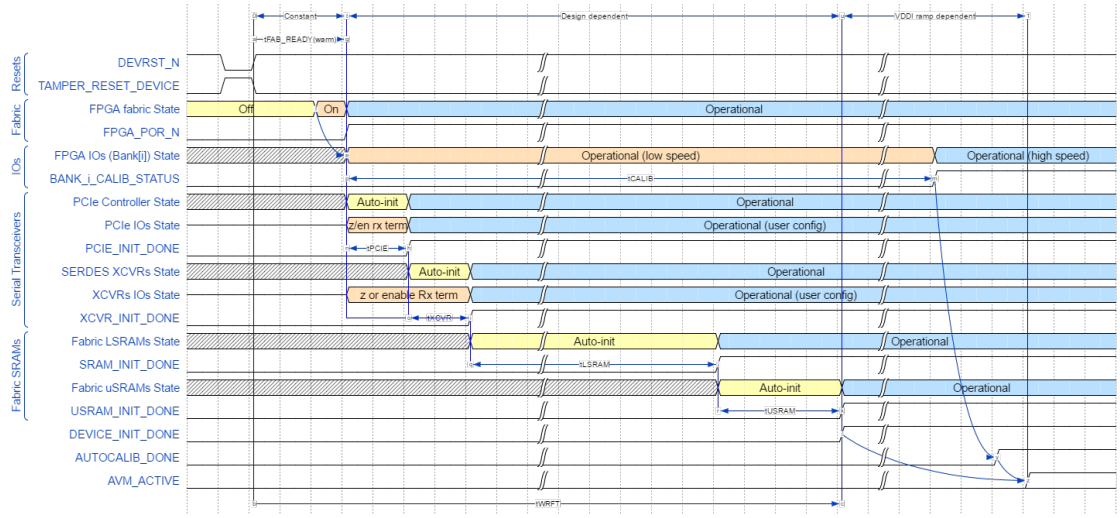
1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	–40		125	°C	
Temperature sensing accuracy	–10		10	°C	

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T_{FAB_READY} to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T_{FAB_READY} to auto-update start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to programming recovery start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to the tamper flags being available	T_{TAMPER_READY}	0	0	0	ms	
The time from T_{FAB_READY} to the Athena Crypto co-processor being available (for S devices only)	T_{CRYPTO_READY}	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to T_{PUF_OVHD} at section Secure NVM Performance (see page 58).

7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in I/O-Related Supplies (see page 66).

Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

Note: In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash*Freeze Mode and to exit Flash*Freeze mode.

7.11 User Crypto

The following section describes user crypto.

7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 112 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V – 1	VDD = 1.05 V STD	VDD = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	189		189		MHz	–40 °C to 100 °C

7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Throughput cycle count collected with Athena TeraFire Core and RISCV running at 100 MHz.

Table 113 • AES

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-ECB-128 encrypt[1]	128	515	1095
	64K	50157	933
AES-ECB-128 decrypt[1]	128	557	1760
	64K	48385	1524
AES-ECB-256 encrypt[1]	128	531	1203
	64K	58349	1203
AES-ECB-256 decrypt[1]	128	589	1676
	64K	56673	1671
AES-CBC-256 encrypt[1]	128	576	1169
	64K	52547	1169
AES-CBC-256 decrypt[1]	128	585	1744
	64K	48565	1652
AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1925	2740
	64K	60070	2158
AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1973	2268
	64K	60102	2151

1. With DPA counter measures.

Table 114 • GMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-GCM-256[1], 128-bit tag, (message is only authenticated)	128	1863	2211
	64K	49707	2128

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