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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-1fcg484e

2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance ¹	C _{IN} (dedicated GPIO)		5.6	pf	
	C _{IN} (GPIO)		5.6	pf	
	C _{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I _L (GPIO)		10	μA	I/O disabled, high – Z
	I _L (HSIO)		10	μA	I/O disabled, high – Z
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}	T _{RISE}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}	T _{FALL}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Pad pull-up when V _{IN} = 0 ⁵	I _{PU}	137	220	μA	V _{DDIX} = 3.3 V
Pad pull-up when V _{IN} = 0 ⁵		102	166	μA	V _{DDIX} = 2.5 V
Pad pull-up when V _{IN} = 0		68	115	μA	V _{DDIX} = 1.8 V
Pad pull-up when V _{IN} = 0		51	88	μA	V _{DDIX} = 1.5 V
Pad pull-up when V _{IN} = 0 ⁶		29	73	μA	V _{DDIX} = 1.35 V
Pad pull-up when V _{IN} = 0	I _{PD}	16	46	μA	V _{DDIX} = 1.2 V
Pad pull-down when V _{IN} = 3.3 V ⁵		65	187	μA	V _{DDIX} = 3.3 V
Pad pull-down when V _{IN} = 2.5 V ⁵		63	160	μA	V _{DDIX} = 2.5 V
Pad pull-down when V _{IN} = 1.8 V		60	117	μA	V _{DDIX} = 1.8 V
Pad pull-down when V _{IN} = 1.5 V		57	95	μA	V _{DDIX} = 1.5 V
Pad pull-down when V _{IN} = 1.35 V		52	86	μA	V _{DDIX} = 1.35 V
Pad pull-down when V _{IN} = 1.2 V		47	79	μA	V _{DDIX} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	−0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTL	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	−0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

Min (%)	Typ	Max (%)	Unit	Condition
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} . For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
-20	34	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	40	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	48	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	60	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	80	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 80% of V_{DDI} .

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
-20	120	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
-20	120	20	Ω	$V_{DDI} = 1.2\text{ V}$
-20	240	20	Ω	$V_{DDI} = 1.2\text{ V}$

Note: Measured at 50% of V_{DDI} .

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination ¹	Internal differential termination	-20	100	20	Ω	$V_{ICM} < 0.8\text{ V}$
		-20	100	40	Ω	$0.6\text{ V} < V_{ICM} < 1.65\text{ V}$
		-20	100	80	Ω	$1.4\text{ V} < V_{ICM}$
Single-ended thevenin termination ^{2, 3}	Internal parallel thevenin termination	-40	50	20	Ω	$V_{DDI} = 1.8\text{ V}/1.5\text{ V}$
		-40	75	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-40	150	20	Ω	$V_{DDI} = 1.8\text{ V}$
		-20	20	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	30	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	40	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	60	20	Ω	$V_{DDI} = 1.5\text{ V}$
		-20	120	20	Ω	$V_{DDI} = 1.5\text{ V}$

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMD525/LCMD533	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

Standard	STD	–1	Unit
LVC MOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDS25	500	500	Mbps
MLVDS25	500	500	Mbps
LVPECL33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVC MOS33 (20 mA)	500	500	Mbps
LVC MOS25 (16 mA)	500	500	Mbps
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps
LVC MOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
F _{MAX}	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
F _{MAX}	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
F _{MAX}	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
F _{MAX}	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
F _{MAX}	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
F _{MAX}	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
F _{MAX} 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Clock-to-Data Condition
F _{MAX} 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 44 • μ SRAM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	T_{ac}		2		2	ns	Read-port

Table 45 • μ PROM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit
Read access time	T_{ac}	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Tx data rate ^{1,2}	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled ²	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency ³	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode ²	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode ²	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Reference clock input rate ^{1,2}	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}		85		Ω	
	V_{OTERM}		100		Ω	
	V_{OTERM}		150		Ω	
Common mode voltage ¹	V_{OCM}	$0.44 \times V_{DDA}$	$0.525 \times V_{DDA}$	$0.59 \times V_{DDA}$	V	DC coupled 50% setting
	V_{OCM}	$0.52 \times V_{DDA}$	$0.6 \times V_{DDA}$	$0.66 \times V_{DDA}$	V	DC coupled 60% setting
	V_{OCM}	$0.61 \times V_{DDA}$	$0.7 \times V_{DDA}$	$0.75 \times V_{DDA}$	V	DC coupled 70% setting
	V_{OCM}	$0.63 \times V_{DDA}$	$0.8 \times V_{DDA}$	$0.83 \times V_{DDA}$	V	DC coupled 80% setting
Rise time ²	T_{TXRF}	41		70	ps	20% to 80%
Fall time ²		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew ³	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew ⁴	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time ⁷	$T_{TxElTrEntry}$				ns	
Electrical idle transition exit time ⁷	$T_{TxElTrExit}$				ns	
Electrical idle amplitude	V_{TxElpp}				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time ⁸	$T_{DPLLlock}$				REFCLK UIs	
Total jitter ^{5,6}	T_J				UI	Data rate ≥ 8.5 Gbps to 12.7 Gbps ⁹
Deterministic jitter ^{5,6}	T_{DJ}				UI	(Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter ^{5,6}	T_J			0.28	UI	Data rate ≥ 3.2 Gbps to 8.5 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_J			0.28	UI	Data rate ≥ 1.6 Gbps to 3.2 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_J			0.13	UI	Data rate ≥ 800 Mbps to 1.6 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.02	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_J			0.06	UI	Data rate = 250 Mbps to 800 Mbps
Deterministic jitter ^{5,6}	T_{DJ}			0.01	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8**Authentication Time**

The following tables describe authentication system service time.

Table 84 • Authentication Services

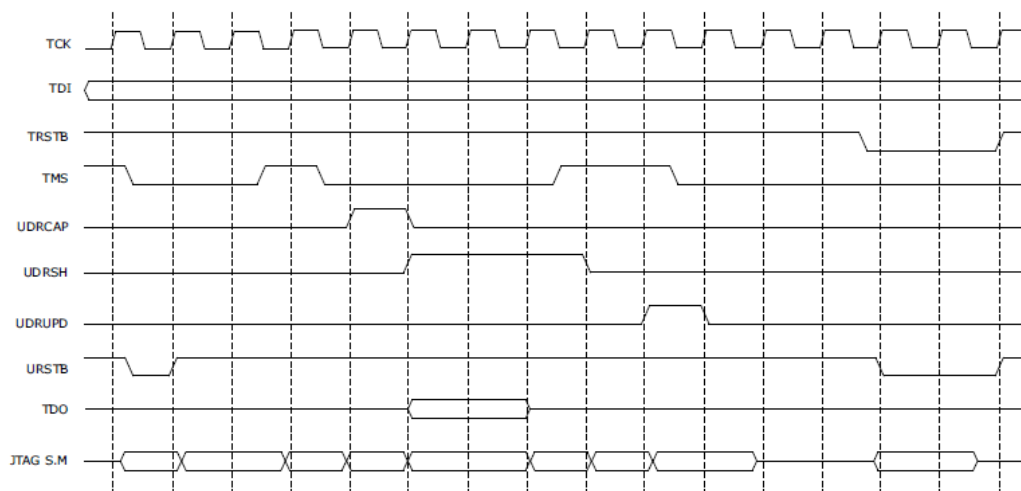
Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9**Secure NVM Performance**

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

Figure 3 • UJTAG Timing Diagram

7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 89 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}				MHz	

7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

Table 90 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V _{DDI} = 3.3 V Max	V _{DDI} = 2.5 V Max	V _{DDI} = 1.8 V Max	V _{DDI} = 1.5 V Max	V _{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins ¹	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

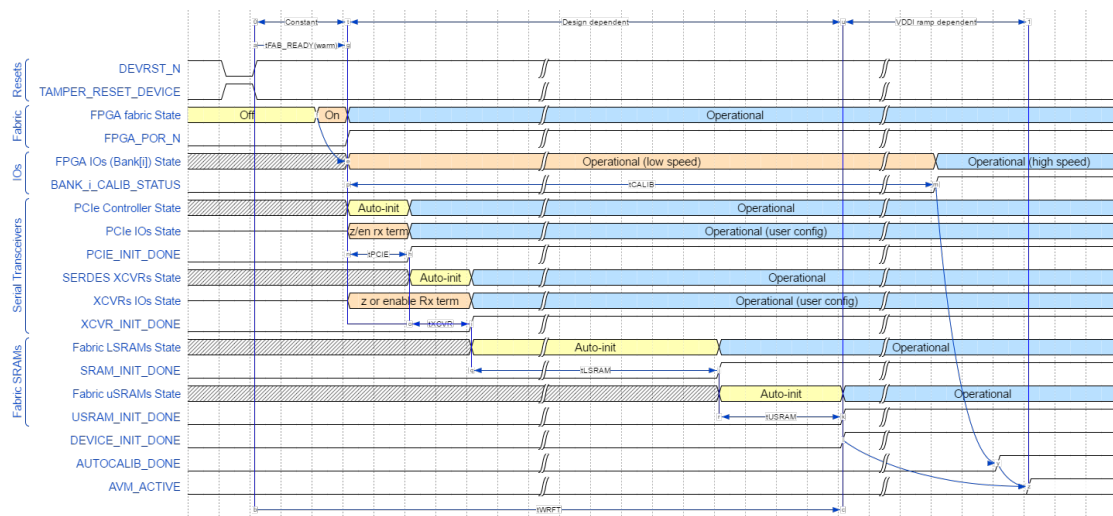
Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T _{JTAG_ACTIVE} ^{1, 2}	45	52	ns
	T _{MESH_ERR} ²	1.8	2.2	μs
	T _{CLK_GLITCH} ^{1, 2}			ns
	T _{CLK_FREQ} ^{1, 2}			μs
	T _{LOW_1P05} ²	70	108	μs
	T _{HIGH_1P8} ²	85	120	μs
	T _{HIGH_2P5} ²	130	520	μs
	T _{GLITCH_1P05} ²			μs
	T _{SECDEC} ^{1, 2}			μs
	T _{DRI_ERR} ²	14	18	μs
	T _{WDOG} ^{1, 2}			μs
	T _{LOCK_ERR} ²			μs
Time from system controller instruction execution to flag generation	T _{INST_BUF_ACCESS} ^{2, 3}	4	5	μs
	T _{INST_DEBUG} ^{2, 3}	3.3	4	μs
	T _{INST_CHK_DIGEST} ^{2, 3}	1.8	3	μs
	T _{INST_EC_SETUP} ^{2, 3}	1.8	2	μs
	T _{INST_FACT_PRIV} ^{2, 3}	3.8	5	μs
	T _{INST_KEY_VAL} ^{2, 3}	2.5	3.1	μs
	T _{INST_MISC} ^{2, 3}	1.5	2	μs
	T _{INST_PASSCODE_MATCH} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_SETUP} ^{2, 3}	4.2	5	μs
	T _{INST_PROG} ^{2, 3}	3.8	4.1	μs
	T _{INST_PUB_INFO} ^{2, 3}	4	4.5	μs
	T _{INST_ZERO_RECO} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_FAIL} ^{2, 3}	170	180	μs
	T _{INST_KEY_VAL_FAIL} ^{2, 3}	92	110	μs
	T _{INST_UNUSED} ^{2, 3}	4	5	μs
Time from sending the CLEAR to deassertion on FLAG	T _{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	T _{IO_DISABLE}	40	50	ns

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

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