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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	364
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-1fcg784e

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# 6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

## 6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

#### Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	Vdd	-0.5	1.13	V
Transceiver Tx and Rx lanes supply	Vdda	-0.5	1.13	V
Programming and HSIO receiver supply	VDD18	-0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	VDD25	-0.5	2.7	V
Transceiver PLL high-voltage supply	VDDA25	-0.5	2.7	V
Transceiver reference clock supply	Vdd_xcvr_clk	-0.5	3.6	V
Global VREF for transceiver reference clocks	XCVRvref	-0.5	3.6	V
HSIO DC I/O supply <sup>2</sup>	VDDIx	-0.5	2.0	V
GPIO DC I/O supply <sup>2</sup>	VDDIx	-0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	Vddi3	-0.5	3.6	V
GPIO auxiliary power supply for I/O bank x <sup>2</sup>	Vddauxx	-0.5	3.6	V
Maximum DC input voltage on GPIO	Vin	-0.5	3.8	V
Maximum DC input voltage on HSIO	Vin	-0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver VIN	-0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK VIN	-0.5	3.6	V
Storage temperature (ambient) <sup>1</sup>	Tstg	-65	150	°C
Junction temperature <sup>1</sup>	T	-55	135	°C
Maximum soldering temperature RoHS	Tsolrohs		260	°C
Maximum soldering temperature leaded	TSOLPB		220	°C

- 1. See FPGA Programming Cycles vs Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
- 2. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

## 6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

#### **Table 4 • Recommended Operating Conditions**

Parameter	Symbol	Min	Тур	Max	Unit
FPGA core supply at 1.0 V mode <sup>1</sup>	Vdd	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode <sup>1</sup>	Vdd	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) <sup>1</sup>	Vdda	0.97	1.00	1.03	V



AC (Vin) Overshoot Duration as % at Ti = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

### Table 8 • Maximum Overshoot During Transitions for GPIO

Note: Overshoot level is for VDDI at 3.3 V.

The following table shows the maximum AC input voltage ( $V_{IN}$ ) undershoot duration for GPIO.

AC (VIN) Undershoot Duration as % at TJ = 100 °C	Condition (V)
100	-0.5
100	-0.55
100	-0.6
100	-0.65
100	-0.7
100	-0.75
100	-0.8
100	-0.85
100	-0.9
100	-0.95
100	-1
100	-1.05
100	-1.1
100	-1.15
100	-1.2
69	-1.25
45	-1.3

## Table 9 • Maximum Undershoot During Transitions for GPIO



**Note**: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST\_N, and FF\_EXIT\_N. Weak pull-up (as specified in GPIO) is always enabled.

## 6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

## 6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

#### Table 12 • DC Input Levels

I/O Standard	Vooi Min (V)	Vool Typ (V)	V <sub>DDI</sub> Max (V)	V⊩ Min (V)	V⊫ Max (V)	V⊪ Min (V)	Vін <sup>1</sup> Max (V)
PCI	3.15	3.3	3.45	-0.3	0.3	0.5	3.45
					×	×	
					VDDI	Vddi	
LVTTL	3.15	3.3	3.45	-0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	-0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	-0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	-0.3	0.35	0.65	1.89
					×	×	
					Vddi	Vddi	
LVCMOS15	1.425	1.5	1.575	-0.3	0.35	0.65	1.575
					×	×	
					Vddi	VDDI	
LVCMOS12	1.14	1.2	1.26	-0.3	0.35	0.65	1.26
					x	×	
					Vddi	VDDI	
SSTL25I <sup>2</sup>	2.375	2.5	2.625	-0.3	VREF	VREF	2.625
					-	+	
					0.15	0.15	
SSTL25II <sup>2</sup>	2.375	2.5	2.625	-0.3	VREF	Vref	2.625
					-	+	
					0.15	0.15	
SSTL18I <sup>2</sup>	1.71	1.8	1.89	-0.3	VREF	Vref	1.89
					-	+	
					0.125	0.125	
SSTL18II <sup>2</sup>	1.71	1.8	1.89	-0.3	VREF	Vref	1.89
					-	+	
					0.125	0.125	
SSTL15I	1.425	1.5	1.575	-0.3	VREF	VREF	1.575
					-	+	
					0.1	0.1	
SSTL15II	1.425	1.5	1.575	-0.3	VREF	VREF	1.575
					-	+	
					0.1	0.1	

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Standard	Description	٧L1	VH1	VID <sup>2</sup>	VICM <sup>2</sup>	Vmeas <sup>3, 4</sup>	VREF <sup>1, 5</sup>	Un
HSUL18I	HSUL 1.8 V Class I	V <sub>REF</sub> – 0.54	V <sub>REF</sub> + 0.54			VREF	0.90	V
HSUL18II	HSUL 1.8 V Class II	V <sub>REF</sub> –	V <sub>REF</sub> +			Vref	0.90	V
HSUL12	HSUL 1.2 V	V <sub>REF</sub> –	V <sub>REF</sub> +			Vref	0.60	V
		.22	.22					
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	Vref – .15	V <sub>REF</sub> + .15			Vref	0.84	V
POD12II	POD 1.2 V Class II	V <sub>REF</sub> – .15	V <sub>REF</sub> + .15			Vref	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	0.800	0		V
SLVS33	Scalable low- voltage signaling	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.200	0		V

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Standard	Description	VL1	VH1	Vid2	VICM <sup>2</sup>	Vmeas <sup>3, 4</sup>	Vref <sup>1, 5</sup>	Unit
SLVS25	SLVS 2.5 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	Vісм – .125	V <sub>ICM</sub> + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.350	0		V
BLVDSE25 <sup>6</sup>	Bus LVDS 2.5 V	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
MLVDSE256	Multipoint LVDS 2.5 V	Vісм – .125	Vісм + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	1.650	0		V
LVPECLE336	Low-voltage positive emitter coupled logic	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	Vісм — .125	Vісм + .125	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V <sub>ICM</sub> — .125	VICM + .125	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	V <sub>ICM</sub> — .125	V <sub>ICM</sub> + .125	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	V <sub>ICM</sub> – .125	V <sub>ICM</sub> + .125	0.250	0.675	0		V

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Standard	Description	Rref (Ω)	Cref (pF)	Vmeas (V)	Vref (V)
SSTL18I	SSTL 1.8 V Class I	50	0	VREF	0.9
SSTL18II	SSTL 1.8 V Class II	50	0	VREF	0.9
SSTL15I	SSTL 1.5 V Class I	50	0	VREF	0.75
SSTL15II	SSTL 1.5 V Class II	50	0	VREF	0.75
SSTL135I	SSTL 1.35 V Class I	50	0	Vref	0.675
SSTL135II	SSTL 1.35 V Class II	50	0	VREF	0.675
HSTL15I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	Vref	0.75
HSTL15II	HSTL 1.5 V Class II	50	0	VREF	0.75
HSTL135I	HSTL 1.35 V Class I	50	0	VREF	0.675
HSTL135II	HSTL 1.35 V Class II	50	0	VREF	0.675
HSTL12	HSTL 1.2 V	50	0	VREF	0.6
HSUL18I	High-speed unterminated logic 1.8 V Class I	50	0	Vref	0.9
HSUL18II	HSUL 1.8 V Class II	50	0	VREF	0.9
HSUL12	HSUL 1.2 V	50	0	VREF	0.6
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	Vref	0.84
POD12II	POD 1.2 V Class II	50	0	VREF	0.84
LVDS33	LVDS 3.3 V	100	0	01	0
LVDS25	LVDS 2.5 V	100	0	01	0
LVDS18	LVDS 1.8 V	100	0	01	0
RSDS33	Reduced swing differential signaling 3.3 V	100	0	01	0
RSDS25	RSDS 2.5 V	100	0	01	0
RSDS18	RSDS 1.8 V	100	0	01	0
MINILVDS33	Mini-LVDS 3.3 V	100	0	01	0
MINILVDS25	Mini-LVDS 2.5 V	100	0	01	0
SUBLVDS33	Sub-LVDS 3.3 V	100	0	01	0
SUBLVDS25	Sub-LVDS 2.5 V	100	0	01	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	01	0
PPDS25	PPDS 2.5 V	100	0	01	0
BUSLVDSE25	Bus LVDS	100	0	01	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	01	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	01	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	01	0

1. The value given is the differential output voltage.



Standard	STD	-1	Unit
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver. 2. Performance is achieved with  $V_{\rm ID} \ge 200$  mV.

#### 7.1.4 **Output Buffer Speed**

## Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	-1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps



## 7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Memory Standard	Gearing Ratio	Vddaux	Vddi	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3 <sup>1</sup>	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3 <sup>1</sup>	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3 <sup>1</sup>	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2 <sup>1</sup>	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2 <sup>1</sup>	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2 <sup>1</sup>	2:1	1.8 V	1.8 V	333	400	167	200

### Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

### Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	Vddaux	Vddi	STD (Mbps)	−1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2 <sup>1</sup>	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2 <sup>1</sup>	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.



## 7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

## 7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

#### Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	—1 Тур	-1 Max	Unit	Clock-to-Data Condition
Fмах	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
Fмах	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
Fмах	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
Fмах	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

#### Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	—1 Тур	-1 Max	Unit	Clock-to- Data Condition
Fмах	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
Fмах	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
Fмах	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
Fмах	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
Fmax 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned



Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	—1 Тур	-1 Max	Unit	Clock-to- Data Condition
Fmax 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

### Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	—1 Тур	-1 Max	Unit	Forwarded Clock-to-Data Skew
Output F <sub>MAX</sub>	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned <sup>1</sup>
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered <sup>1</sup>

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	—1 Тур	-1 Max	Unit	Forwarded Clock-to- Data Skew
Output Fmax	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output Fmax 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output Fmax 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

### Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics



Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	—1 Тур	-1 Max	Unit	Forwarded Clock-to- Data Skew
Output F <sub>MAX</sub> 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F <sub>MAX</sub> 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F <sub>MAX</sub> 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

### Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance <sup>1</sup>	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data. **Note:** See the LVDS output buffer specifications for transmit characteristics.

## 7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

## 7.2.1 Clocking

The following table provides clocking specifications.

## Table 35 • Global and Regional Clock Characteristics (-40 °C to 100 °C)

Parameter	Symbol	V <sub>DD</sub> = 1.0 V STD	V <sub>DD</sub> = 1.0 V -1	V <sub>DD</sub> = 1.05 V STD	V <sub>DD</sub> = 1.05 V –1	Unit	Condition
Global clock F <sub>MAX</sub>	Fmaxg	500	500	500	500	MHz	
Regional clock Fmax	Fmaxr	375	375	375	375	MHz	Transceiver interfaces only
-	Fmaxr	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	Tdcdg	190	190	190	190	ps	At 500 MHz



Parameter	Symbol	Min	Тур	Max	Unit
Maximum input period clock jitter (reference and feedback clocks) <sup>2</sup>	Fmaxinj		120	1000	ps
PLL VCO frequency	Fvco	800		5000	MHz
Loop bandwidth (Int) <sup>3</sup>	Fвw	Fphdet/55	FPHDET/44	Fphdet/30	MHz
Loop bandwidth (FRAC) <sup>3</sup>	Fвw	<b>Б</b> рндет <b>/91</b>	FPHDET/77	Fphdet/56	MHz
Static phase offset of the PLL outputs⁴	Тѕро			Max (±60 ps, ±0.5 degrees)	ps
	TOUTJITTER				ps
PLL output duty cycle precision	Τουτρυτγ	48		54	%
PLL lock time <sup>5</sup>	Тьоск			Max (6.0 μs, 625 PFD cycles)	μs
PLL unlock time <sup>6</sup>	Tunlock	2		8	PFD cycles
PLL output frequency	Fout	0.050		1250	MHz
Minimum reset pulse width	TMRPW				μs
Maximum delay in the feedback path <sup>7</sup>	Fmaxdfb			1.5	PFD cycles
Spread spectrum modulation spread <sup>8</sup>	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency <sup>9</sup>	Mod_Freq	Fphdetf/(128x63)	32	Fphdetf/(128)	KHz

1. Minimum time for high or low pulse width.

- 2. Maximum jitter the PLL can tolerate without losing lock.
- 3. Default bandwidth setting of BW\_PROP\_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW\_PROP\_CTRL = "00" and can be increased if BW\_PROP\_CTRL = "10" and will be at the highest value if BW\_PROP\_CTRL = "11".
- 4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
- 5. Input clock cycle is REFDIV/FREF. For example, FREF = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
- 6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
- 7. Maximum propagation delay of external feedback path in deskew mode.
- 8. Programmable capability for depth of down spread or center spread modulation.
- 9. Programmable modulation rate based on the modulation divider setting (1 to 63).

**Note**: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 \* VCO Frequency) - 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

## 7.2.3 DLL

The following table provides information about DLL.

### **Table 38 • DLL Electrical Characteristics**

Parameter <sup>1</sup>	Symbol	Min	Тур	Max	Unit
Input reference clock frequency	FINF	133		800	MHz
Input feedback clock frequency	Finfdbf	133		800	MHz
Primary output clock frequency	FOUTPF	133		800	MHz



Parameter <sup>1</sup>	Symbol	Min	Тур	Max	Unit
Secondary output clock frequency <sup>2</sup>	Foutsf	33.3		800	MHz
Input clock cycle-to-cycle jitter	Finj			200	ps
Output clock period cycle-to-cycle	Toutjitterp			300	ps
jitter (w/clean input)					
Output clock-to-clock skew between	Тѕкеш			±200	ps
two outputs with the same phase settings					
DLL lock time	Тьоск	16		16K	Reference clock cycles
Minimum reset pulse width	Tmrpw	3			ns
Minimum input pulse width <sup>3</sup>	TMIPW	20			ns
Minimum input clock pulse width high	Тмрин	400			ps
Minimum input clock pulse width low	TMPWL	400			ps
Delay step size	Tdel	12.7	30	35	ps
Maximum delay block delay <sup>4</sup>	TDELMAX	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input) $^{5}$	TDUTY	40		60	%
Output clock duty cycle (in phase reference mode) <sup>5</sup>	TDUTY50	45		55	%

- 1. For all DLL modes.
- 2. Secondary output clock divided by four option.
- 3. On load, direction, move, hold, and update input signals.
- 4. 128 delay taps in one delay block.
- 5. Without duty cycle correction enabled.

## 7.2.4 RC Oscillators

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The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

#### Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit
Operating frequency	RC <sub>2FREQ</sub>		2		MHz
Accuracy	RC2FACC	-4		4	%
Duty cycle	RC <sub>2DC</sub>	46		54	%
Peak-to-peak output period jitter	RC <sub>2PJIT</sub>		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC <sub>2CJIT</sub>		5	10	ns
Operating current (VDD25)	RC2IVPPA			60	μA
Operating current (VDD)	RC <sub>2IVDD</sub>			2.6	μA

#### Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit
Operating frequency	RCSCFREQ		160		MHz
Accuracy	RCSCFACC	-4		4	%
Duty cycle	RCscdc	47		52	%
Peak-to-peak output period jitter	RCscpjit			600	ps
Peak-to-peak output cycle-to-cycle jitter	<b>RC</b> SCCJIT			172	ps
Operating current (V <sub>DD25</sub> )	RCscvppa			599	μΑ



Parameter	Symbol	Min	Тур	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps⁵
		0.41			UI	>1.6 to 3.2 Gbps <sup>5</sup>
		0.41			UI	>0.8 to 1.6 Gbps <sup>5</sup>
		0.41			UI	250 to 800 Mpbs <sup>5</sup>
Total jitter tolerance with	TIJTOLSE	0.65			UI	3.125 Gbps⁵
stressed eye		0.65			UI	6.25 Gbps <sup>6</sup>
		0.7			UI	10.3125 Gbps <sup>6</sup>
					UI	12.7 Gbps <sup>6, 10</sup>
Sinusoidal jitter tolerance with	TSJTOLSE	0.1			UI	3.125 Gbps⁵
stressed eye		0.05			UI	6.25 Gbps <sup>6</sup>
		0.05			UI	10.3125 Gbps <sup>6</sup>
					UI	12.7 Gbps <sup>6, 10</sup>
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

1. Valid at 3.2 Gbps and below.

- 2. Data vs. Rx reference clock frequency.
- 3. Achieves compliance with PCIe electrical idle detection.
- 4. Achieves compliance with SATA OOB specification.
- 5. Rx jitter values based on bit error ratio (BER) of 10−12, AC coupled input with 400 mV V<sub>ID</sub>, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- 6. Rx jitter values based on bit error ratio (BER) of 10−12, AC coupled input with 400 mV V<sub>ID</sub>, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- 7. For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- 8. For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- 9. Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- 10. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

## 7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

### 7.5.1 PCI Express

The following tables describe the PCI express.

#### Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.



Parameter	Symbol	Тур	Max	Unit
Time from negation of RESPONSE to all I/Os re-enabled	$T_{CLR\_IO\_DISABLE}$	28	38	μs
Time from triggering the response to security locked	TLOCKDOWN			ns
Time from negation of RESPONSE to earlier security unlock condition	Tclr_lockdown			ns
Time from triggering the response to device enters RESET	Ttr_RESET	11.7	14	μs
Time from triggering the response to start of zeroization	Ttr_ZEROLISE	7.4	8.2	ms

## 7.8.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

#### Table 95 • System Controller Suspend Entry and Exit Characteristics

Parameter	Symbol	Definition	Тур	Max	Unit
Time from TRSTb falling edge to SUSPEND_EN signal assertion	Tsuspend_Tr <sup>1, 2</sup>	Suspend entry time from TRST_N assertion	42	44	ns
Time from TRSTb rising edge to ACTIVE signal assertion	Tsuspend_exit	Suspend exit time from TRST_N negation	361	372	ns

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND\_EN.

2. ACTIVE signal must never be asserted with SUSPEND\_EN is asserted.

## 7.8.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

#### **Table 96 • Dynamic Reconfiguration Interface Timing Characteristics**

Parameter	Symbol	Max	Unit
PCLK frequency	FPD_PCLK	200	MHz

## 7.9 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST\_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

## 7.9.1 Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.



### Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Тур	Max	Unit	Condition
The time from T <sub>FAB_READY</sub> to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T <sub>FAB_READY</sub> to auto-update start			Tpuf_ovhd <sup>1</sup>	$T_{PUF\_OVHD^1}$	ms	
The time from TFAB_READY to programming recovery start			$T_{PUF\_OVHD^1}$	$T_{\text{PUF}\_\text{OVHD}^1}$	ms	
The time from T <sub>FAB_READY</sub> to the tamper flags being available	TTAMPER_READY	0	0	0	ms	
The time from T <sub>FAB_READY</sub> to the Athena Crypto co-processor being available (for S devices only)	Tcrypto_ready	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to TPUF\_OVHD at section Secure NVM Performance (see page 58).

## 7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

### Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

#### Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in I/O-Related Supplies (see page 66).

#### Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

**Note:** In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash\*Freeze Mode and to exit Flash\*Freeze mode.



#### Table 104 • Flash\*Freeze

Parameter	Symbol	Min	Тур	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	Tff_entry		59		μs	
The time from Flash*Freeze exit pin assertion to fabric operational state	Tff_fabric_up		133		μs	
The time from Flash*Freeze exit pin assertion to I/Os operational	TFF_IO_ACTIVE		143		μs	

## 7.10 Dedicated Pins

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The following section describes the dedicated pins.

## 7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

## Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Тур	Max	Unit	Condition
Tdisu	TDI input setup time	0.0			ns	
TDIHD	TDI input hold time	2.0			ns	
TTMSSU	TMS input setup time	1.5			ns	
Ттмянd	TMS input hold time	1.5			ns	
Fтск	TCK frequency			25	MHz	
Ттскос	TCK duty cycle	40		60	%	
Ττροςα	TDO clock to Q out			8.4	ns	C <sub>LOAD</sub> = 40 pf
TRSTBCQ	TRSTB clock to Q out			23.5	ns	C <sub>LOAD</sub> = 40 pf
TRSTBPW	TRSTB min pulse width	50			ns	
TRSTBREM	TRSTB removal time	0.0			ns	
TRSTBREC	TRSTB recovery time	12.0			ns	
CINTDI	TDI input pin capacitance			5.3	pf	
CINTMS	TMS input pin capacitance			5.3	pf	
СІМтск	TCK input pin capacitance			5.3	pf	
CINTRSTB	TRSTB input pin capacitance			5.3	pf	

## 7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

#### Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Тур	Max	Unit	Condition
SCK frequency	Fмsck			20	MHz	



1. With DPA counter measures.

#### Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 <sup>1</sup> ,	512	7477	2361
256-bit key	64K	88367	2099
HMAC-SHA-384 <sup>1</sup> ,	1024	13049	2257
384-bit key	64K	106103	2153

1. With DPA counter measures.

#### Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock- Cycles	CAL Delay In CPU Clock- Cycles
AES-CMAC-2561	128	446	9058
(message is only authenticated)	64К	45494	111053

1. With DPA counter measures.

### Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce +		102457	2751
8-bit optype			
256-bit nonce +		103218	2089
8-bit optype			

#### Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 <sup>1</sup>	512	2386	1579
	64K	77576	990
SHA-2561	512	2516	884
	64K	84752	938
SHA-3841	1024	4154	884
	64K	100222	938
SHA-512 <sup>1</sup>	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

#### Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock- Cycles	CAL Delay In CPU Clock- Cycles
ECDSA SigGen,	1024	12528912	6944
P-384/SHA-384 <sup>1</sup>	8К	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155



ECDSA SigVer,	1024	6421841	5759	
P-384/SHA-384	8K	6273510	5759	
Key Agreement (KAS), P- 384		5039125	6514	
Point Multiply, P-256 <sup>1</sup>		5176923	4482	
Point Multiply, P-384 <sup>1</sup>		12043199	5319	
Point Multiply, P-521 <sup>1</sup>		26887187	6698	
Point Addition, P-384		3018067	5779	
KeyGen (PKG), P-384		12055368	6908	
Point Verification, P-384		5091	3049	

#### 1. With DPA counter measures.

### Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock- Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048 <sup>1</sup> , CRT	2048	26862392	15900
Decrypt, RSA-3072 <sup>1</sup> , CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384 <sup>1</sup> ,CRT, PKCS #1 V 1 1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V	1024	148090970	14642
1.5	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537,	1024	970991	12000
PKCS #1 V 1.5	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537,	1024	443493	8436
PKCS #1 V 1.5	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537,	1024	973269	11313
ANSI X9.31	8K	983255	11146

1. With DPA counter measures.

## Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock- Cycles
SigGen, DSA-3072/SHA-3841	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133





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