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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	325-LFBGA, FC
Supplier Device Package	325-FCBGA (11x14.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-1fcsg325e

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see System Services (see page 59).
- The Non-Volatile Characteristics section was updated. For more information, see Non-Volatile Characteristics (see page 51).
- The Fabric Macros section was updated. For more information, see Fabric Macros (see page 60).
- The Transceiver Switching Characteristics section was updated. For more information, see Transceiver Switching Characteristics (see page 42).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed and HSIO Maximum Output Buffer Speed.
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications.
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics.
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Preliminary
MPF200T, TL, TS, TLS	Preliminary
MPF300T, TL, TS, TLS	Preliminary
MPF500T, TL, TS, TLS	Preliminary

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps)[1]	V_{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V_{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V_{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	$V_{DD\_XCVR\_CLK}$	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	$V_{DD\_XCVR\_CLK}$	2.375	2.5	2.625	V
Global V_{REF} for transceiver reference clocks[3]	$XCVR_{VREF}$	Ground		$V_{DD\_XCVR\_CLK}$	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V[4]	V_{DDIx}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V[2,4]	V_{DDIx}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V_{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 3.3 V nominal[2,4]	V_{DDAUXx}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 2.5 V nominal or lower[2,4]	V_{DDAUXx}	2.375	2.5	2.625	V
Extended commercial temperature range	T_J	0		100	°C
Industrial temperature range	T_J	–40		100	°C
Extended commercial programming temperature range	T_{PRG}	0		100	°C
Industrial programming temperature range	T_{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDIx} is 2.5 V nominal or 3.3 V nominal, V_{DDAUXx} must be connected to the V_{DDIx} supply for that bank. If V_{DDIx} for a given GPIO bank is <2.5 V nominal, V_{DDAUXx} per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}$/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
PCI	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45
LVTTL	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89
LVCMOS15	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575
LVCMOS12	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26
SSTL25I[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL25II[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL18I[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL18II[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18[5]	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18[5]	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18[5]	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

Min (%)	Typ	Max (%)	Unit	Condition
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 80% of V_{DDI}.

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	20	Ω	V_{ICM} < 0.8 V
		–20	100	40	Ω	0.6 V < V_{ICM} < 1.65 V
		–20	100	80	Ω	1.4 V < V_{ICM}
Single-ended thevenin termination[2, 3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3,4]	V_{REF}[1,5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL18I	SSTL 1.8 V Class I	50	0	V_{REF}	0.9
SSTL18II	SSTL 1.8 V Class II	50	0	V_{REF}	0.9
SSTL15I	SSTL 1.5 V Class I	50	0	V_{REF}	0.75
SSTL15II	SSTL 1.5 V Class II	50	0	V_{REF}	0.75
SSTL135I	SSTL 1.35 V Class I	50	0	V_{REF}	0.675
SSTL135II	SSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL15I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	V_{REF}	0.75
HSTL15II	HSTL 1.5 V Class II	50	0	V_{REF}	0.75
HSTL135I	HSTL 1.35 V Class I	50	0	V_{REF}	0.675
HSTL135II	HSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL12	HSTL 1.2 V	50	0	V_{REF}	0.6
HSUL18I	High-speed unterminated logic 1.8 V Class I	50	0	V_{REF}	0.9
HSUL18II	HSUL 1.8 V Class II	50	0	V_{REF}	0.9
HSUL12	HSUL 1.2 V	50	0	V_{REF}	0.6
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	V_{REF}	0.84
POD12II	POD 1.2 V Class II	50	0	V_{REF}	0.84
LVDS33	LVDS 3.3 V	100	0	0[1]	0
LVDS25	LVDS 2.5 V	100	0	0[1]	0
LVDS18	LVDS 1.8 V	100	0	0[1]	0
RSDS33	Reduced swing differential signaling 3.3 V	100	0	0[1]	0
RSDS25	RSDS 2.5 V	100	0	0[1]	0
RSDS18	RSDS 1.8 V	100	0	0[1]	0
MINILVDS33	Mini-LVDS 3.3 V	100	0	0[1]	0
MINILVDS25	Mini-LVDS 2.5 V	100	0	0[1]	0
SUBLVDS33	Sub-LVDS 3.3 V	100	0	0[1]	0
SUBLVDS25	Sub-LVDS 2.5 V	100	0	0[1]	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	0[1]	0
PPDS25	PPDS 2.5 V	100	0	0[1]	0
BUSLVDSE25	Bus LVDS	100	0	0[1]	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	0[1]	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	0[1]	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	0[1]	0

1. The value given is the differential output voltage.

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

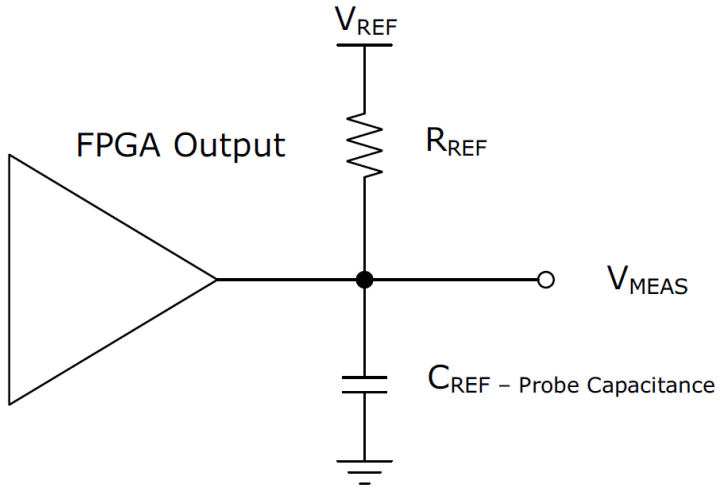
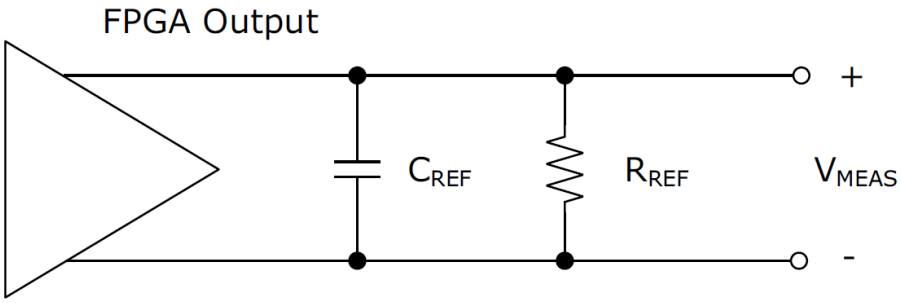


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps

1. Performance is achieved with V_{ID} ≥200 mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F_{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance[1]	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Global clock F_{MAX}	F_{MAXG}	500	500	500	500	MHz	
Regional clock F_{MAX}	F_{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F_{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T_{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter[1]	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency[2]	F_{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F_{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	$T_{OUTJITTERP}$			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T_{SKEW}			±200	ps
DLL lock time	T_{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T_{MRPW}	3			ns
Minimum input pulse width[3]	T_{MIPW}	20			ns
Minimum input clock pulse width high	T_{MPWH}	400			ps
Minimum input clock pulse width low	T_{MPWL}	400			ps
Delay step size	T_{DEL}	12.7	30	35	ps
Maximum delay block delay[4]	T_{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input)[5]	T_{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode)[5]	T_{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

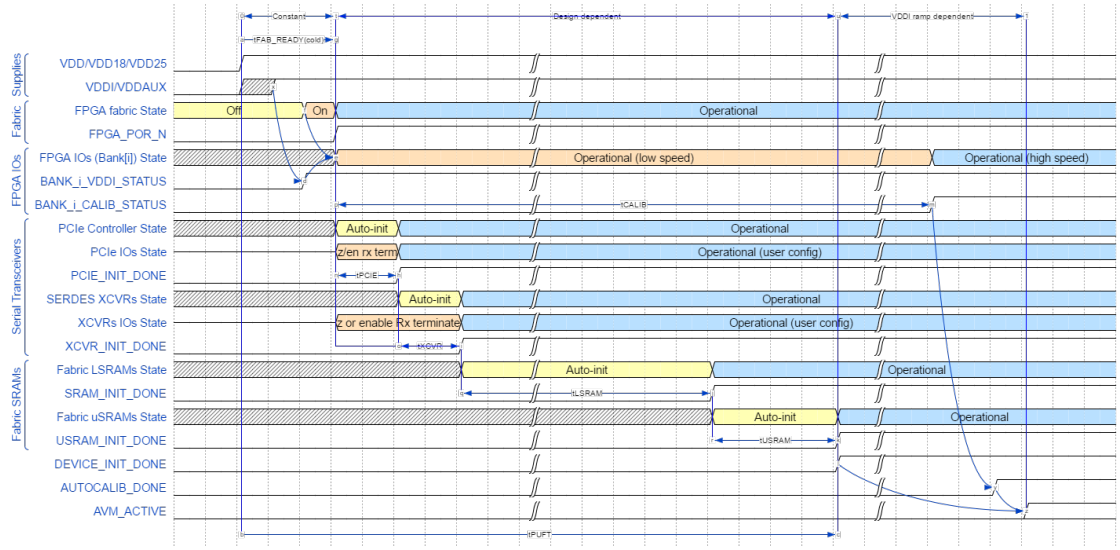
Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{2FREQ}		2		MHz
Accuracy	RC_{2FACC}	–4		4	%
Duty cycle	RC_{2DC}	46		54	%
Peak-to-peak output period jitter	RC_{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC_{2CJIT}		5	10	ns
Operating current (V_{DD25})	RC_{2IVPPA}			60	µA
Operating current (V_{DD})	RC_{2IVDD}			2.6	µA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{SCFREQ}		160		MHz
Accuracy	RC_{SCFACC}	–4		4	%
Duty cycle	RC_{SCDC}	47		52	%
Peak-to-peak output period jitter	RC_{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{SCCJIT}			172	ps
Operating current (V_{DD25})	RC_{SCVPPA}			599	µA

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	µA
Operating current (V_{DD})	RC_{SCVDD}			60.7	µA

Figure 5 • Cold Reset Timing



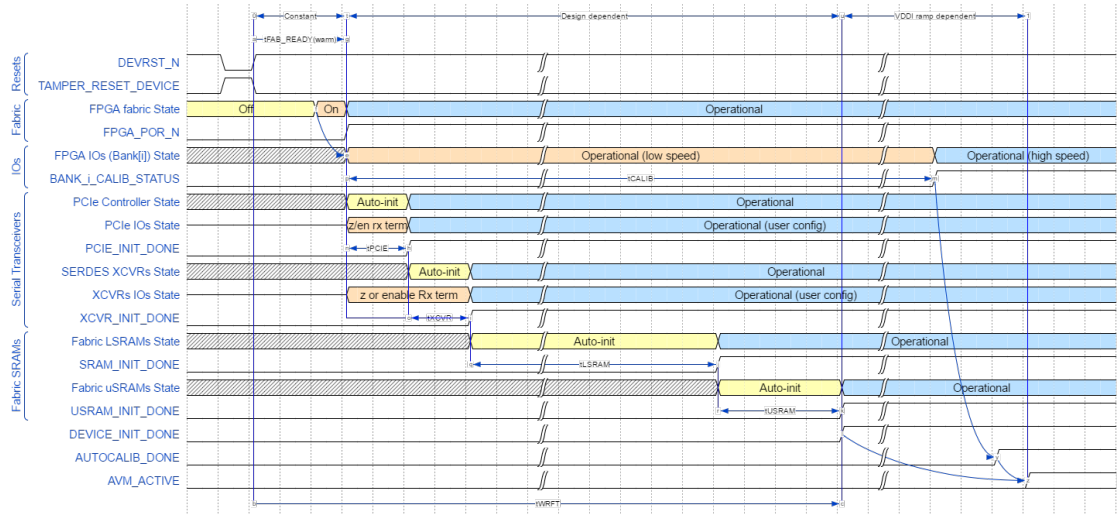
Notes:

- The previous diagram showsthe case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
  - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
  - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
  - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2 Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F_{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T_{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T_{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR_{RAMP}		10		µs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR_{ASSERT}	1			µs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	$DR_{DEASSERT}$	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF_{RAMP}		10		µs	
Minimum FF_EXIT_N assert time	FF_{ASSERT}	1			µs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	$FF_{DEASSERT}$	170			µs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

ECDSA SigVer, P-384/SHA-384	1024	6421841	5759
	8K	6273510	5759
Key Agreement (KAS), P-384		5039125	6514
Point Multiply, P-256[1]		5176923	4482
Point Multiply, P-384[1]		12043199	5319
Point Multiply, P-521[1]		26887187	6698
Point Addition, P-384		3018067	5779
KeyGen (PKG), P-384		12055368	6908
Point Verification, P-384		5091	3049

1. With DPA counter measures.

Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048[1], CRT	2048	26862392	15900
Decrypt, RSA-3072[1], CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384[1] ,CRT, PKCS #1 V 1 1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	148090970	14642
	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	970991	12000
	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	443493	8436
	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	973269	11313
	8K	983255	11146

1. With DPA counter measures.

Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SigGen, DSA-3072/SHA-384[1]	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133

SigVer, DSA-2048/SHA-256	1024	9810527	10884
	8K	9597000	10719
Key Agreement (KAS), DH-3072 (p=3072, security=256)		4920705	9338
Key Agreement (KAS), DH-3072 (p=3072, security=256)[1]		78914533	9083

1. With DPA counter measures.

Table 122 • NRBG

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string		18221	2841
Reseed: no additional input, s=256		13585	1180
Reseed: 384-bit additional input, s=256		15922	1342
Generate: (no additional input), prediction resistance enabled, s= 256	128	15262	1755
	8K	27169	8223
Generate: (no additional input), prediction resistance disabled, s= 256	128	2138	1167
	8K	14045	8223
Generate: (384-bit additional input), prediction resistance enabled, s= 256	128	21299	1944
	8K	33206	8949
Generate: (384-bit additional input), prediction resistance disabled, s= 256	128	11657	1894
	8K	23564	8950
Un-instantiate		761	666

1. With DPA counter measures.

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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