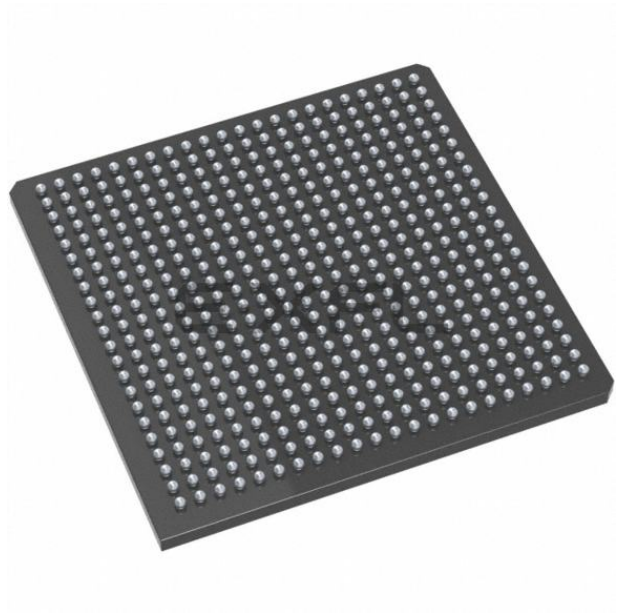

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-1fcvg484e

2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

Note: Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot Duration as % at T_J = 100 °C	Condition (V)
100	–0.05
100	–0.1
100	–0.15
100	–0.2
100	–0.25
100	–0.3
100	–0.35
100	–0.4
44	–0.45
14	–0.5
4.8	–0.55
1.6	–0.6

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

Min (%)	Typ	Max (%)	Unit	Condition
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 80% of V_{DDI}.

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	20	Ω	V_{ICM} < 0.8 V
		–20	100	40	Ω	0.6 V < V_{ICM} < 1.65 V
		–20	100	80	Ω	1.4 V < V_{ICM}
Single-ended thevenin termination[2, 3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3,4]	V_{REF}[1,5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL18I	SSTL 1.8 V Class I	50	0	V_{REF}	0.9
SSTL18II	SSTL 1.8 V Class II	50	0	V_{REF}	0.9
SSTL15I	SSTL 1.5 V Class I	50	0	V_{REF}	0.75
SSTL15II	SSTL 1.5 V Class II	50	0	V_{REF}	0.75
SSTL135I	SSTL 1.35 V Class I	50	0	V_{REF}	0.675
SSTL135II	SSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL15I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	V_{REF}	0.75
HSTL15II	HSTL 1.5 V Class II	50	0	V_{REF}	0.75
HSTL135I	HSTL 1.35 V Class I	50	0	V_{REF}	0.675
HSTL135II	HSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL12	HSTL 1.2 V	50	0	V_{REF}	0.6
HSUL18I	High-speed unterminated logic 1.8 V Class I	50	0	V_{REF}	0.9
HSUL18II	HSUL 1.8 V Class II	50	0	V_{REF}	0.9
HSUL12	HSUL 1.2 V	50	0	V_{REF}	0.6
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	V_{REF}	0.84
POD12II	POD 1.2 V Class II	50	0	V_{REF}	0.84
LVDS33	LVDS 3.3 V	100	0	0[1]	0
LVDS25	LVDS 2.5 V	100	0	0[1]	0
LVDS18	LVDS 1.8 V	100	0	0[1]	0
RSDS33	Reduced swing differential signaling 3.3 V	100	0	0[1]	0
RSDS25	RSDS 2.5 V	100	0	0[1]	0
RSDS18	RSDS 1.8 V	100	0	0[1]	0
MINILVDS33	Mini-LVDS 3.3 V	100	0	0[1]	0
MINILVDS25	Mini-LVDS 2.5 V	100	0	0[1]	0
SUBLVDS33	Sub-LVDS 3.3 V	100	0	0[1]	0
SUBLVDS25	Sub-LVDS 2.5 V	100	0	0[1]	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	0[1]	0
PPDS25	PPDS 2.5 V	100	0	0[1]	0
BUSLVDSE25	Bus LVDS	100	0	0[1]	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	0[1]	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	0[1]	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	0[1]	0

1. The value given is the differential output voltage.

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3[1]	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3[1]	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3[1]	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2[1]	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2[1]	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2[1]	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2[1]	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2[1]	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned[1]
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered[1]

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output FMAX 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks)[2]	F_{MAXINJ}		120	1000	ps
PLL VCO frequency	F_{VCO}	800		5000	MHz
Loop bandwidth (Int)[3]	F_{BW}	F_{PHDET}/55	F_{PHDET}/44	F_{PHDET}/30	MHz
Loop bandwidth (FRAC)[3]	F_{BW}	F_{PHDET}/91	F_{PHDET}/77	F_{PHDET}/56	MHz
Static phase offset of the PLL outputs[4]	T_{SPO}			Max (±60 ps, ±0.5 degrees)	ps
	$T_{OUTJITTER}$				ps
PLL output duty cycle precision	$T_{OUTDUTY}$	48		54	%
PLL lock time[5]	T_{LOCK}			Max (6.0 µs, 625 PFD cycles)	µs
PLL unlock time[6]	T_{UNLOCK}	2		8	PFD cycles
PLL output frequency	F_{OUT}	0.050		1250	MHz
Minimum reset pulse width	T_{MRPW}				µs
Maximum delay in the feedback path[7]	F_{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread[8]	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency[9]	Mod_Freq	F_{PHDETF}/(128x63)	32	F_{PHDETF}/(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3 DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter[1]	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F_{INF}	133		800	MHz
Input feedback clock frequency	F_{INFDBF}	133		800	MHz
Primary output clock frequency	F_{OUTPF}	133		800	MHz

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	µA
Operating current (V_{DD})	RC_{SCVDD}			60.7	µA

Table 44 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 45 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1,2]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled[2]	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[3]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode[2]	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode[2]	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps[1]			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps[1]			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

Table 60 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4 1GbE (1000BASE-T)

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5 SGMII and QSGMII

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6 SDI

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	34.9	µs
	MPF300T, TL, TS, TLS	33.2	34.9	µs
	MPF500T, TL, TS, TLS			µs
Factory digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	493.6	510.1	µs
	MPF300T, TL, TS, TLS	493.6	510.1	µs
	MPF500T, TL, TS, TLS			µs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53[1]	s
	MPF300T, TL, TS, TLS	90[1]	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37[2]	s
	MPF300T, TL, TS, TLS	55[2]	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

Notes:

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T_{SNVM_Rd}	18H				Note 1
Digital signature service raw	T_{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T_{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	$T_{Challenge}$	20H	1.8	2.0	ms	
Nonce service	T_{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	TBIT_AUTH	22H				Note 4
IAP Image authentication	TIAP_AUTH	23H				Note 4
Reserved		26H–3FH				
In application programming by index	$T_{IAP\_Prg\_Index}$	42H				Note 2
In application programming by SPI address	$T_{IAP\_Prg\_Addr}$	43H				Note 2
In application verify by index	TIAP_Ver_Index	44H				Note 5
In application verify by SPI address	TIAP_Ver_Addr	45H				Note 5
Auto update	$T_{AutoUpdate}$	46H				Note 2
Digest check	T_{digest_chk}	47H				Note 3

1. See sNVM Read/Write Characteristics (see page 58).
2. See SPI Master Programming Time (see page 52).
3. See Digest Times (see page 54).
4. See Authentication Services Time (see page 58).
5. See Verify Services Time (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F_{TCK}			25	MHz	

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T_{JTAG_ACTIVE}[1, 2]	45	52	ns
	T_{MESH_ERR}[2]	1.8	2.2	µs
	T_{CLK_GLITCH}[1, 2]			ns
	T_{CLK_FREQ}[1, 2]			µs
	T_{LOW_1P05}[2]	70	108	µs
	T_{HIGH_1P8}[2]	85	120	µs
	T_{HIGH_2P5}[2]	130	520	µs
	T_{GLITCH_1P05}[2]			µs
	T_{SECDEC}[1, 2]			µs
	T_{DRI_ERR}[2]	14	18	µs
	T_{WDOG}[1, 2]			µs
	T_{LOCK_ERR}[2]			µs
Time from system controller instruction execution to flag generation	$T_{INST\_BUF\_ACCESS}$[2, 3]	4	5	µs
	T_{INST_DEBUG}[2, 3]	3.3	4	µs
	$T_{INST\_CHK\_DIGEST}$[2, 3]	1.8	3	µs
	$T_{INST\_EC\_SETUP}$[2, 3]	1.8	2	µs
	$T_{INST\_FACT\_PRIV}$[2, 3]	3.8	5	µs
	$T_{INST\_KEY\_VAL}$[2, 3]	2.5	3.1	µs
	T_{INST_MISC}[2, 3]	1.5	2	µs
	$T_{INST\_PASSCODE\_MATCH}$[2, 3]	2.5	3	µs
	$T_{INST\_PASSCODE\_SETUP}$[2, 3]	4.2	5	µs
	T_{INST_PROG}[2, 3]	3.8	4.1	µs
	$T_{INST\_PUB\_INFO}$[2, 3]	4	4.5	µs
	$T_{INST\_ZERO\_RECO}$[2, 3]	2.5	3	µs
	$T_{INST\_PASSCODE\_FAIL}$[2, 3]	170	180	µs
	$T_{INST\_KEY\_VAL\_FAIL}$[2, 3]	92	110	µs
	T_{INST_UNUSED}[2, 3]	4	5	µs
Time from sending the CLEAR to deassertion on FLAG	T_{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	$T_{IO\_DISABLE}$	40	50	ns

7.9.4 Design Dependence of T PUFT and T WRFT

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note T_{PCIE} , T_{XCVR}, T_{LSRAM}, and T_{USRAM} can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$T_{PUFT} = T_{FAB\_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

$T_{WRFT} = T_{FAB\_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

Note: T_{PCIE}, T_{XCVR}, T_{LSRAM}, T_{USRAM}, and T_{CALIB} are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond T_{PUFT} (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

7.9.5 Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 99 • Cold Boot

Power-On (Cold) Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when weak pull-ups are enabled – $T_{PU\_PD\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when fabric is operational – $T_{FAB\_READY(cold)}$	1.20	4.54	7.87	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(cold)}$	1.22	4.56	7.89	ms

7.9.6 Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 100 • Warm Boot

Warm Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when weak pull-ups/pull-downs are enabled – $T_{PU\_PD\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when fabric is operational – $T_{FAB\_READY(warm)}$	0.94	1.79	2.65	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(warm)}$	0.96	1.81	2.67	ms

7.9.7 Miscellaneous Initialization Parameters

In the following table, T_{FAB_READY} refers to either $T_{FAB\_READY(cold)}$ or $T_{FAB\_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T_{FF_ENTRY}		59		µs	
The time from Flash*Freeze exit pin assertion to fabric operational state	$T_{FF\_FABRIC\_UP}$		133		µs	
The time from Flash*Freeze exit pin assertion to I/Os operational	$T_{FF\_IO\_ACTIVE}$		143		µs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T_{DISU}	TDI input setup time	0.0			ns	
T_{DIHD}	TDI input hold time	2.0			ns	
T_{TMSSU}	TMS input setup time	1.5			ns	
T_{TMSHD}	TMS input hold time	1.5			ns	
F_{TCK}	TCK frequency			25	MHz	
T_{TCKDC}	TCK duty cycle	40		60	%	
T_{TDOCQ}	TDO clock to Q out			8.4	ns	C_{LOAD} = 40 pf
T_{RSTBCQ}	TRSTB clock to Q out			23.5	ns	C_{LOAD} = 40 pf
T_{RSTBPW}	TRSTB min pulse width	50			ns	
$T_{RSTBREM}$	TRSTB removal time	0.0			ns	
$T_{RSTBREC}$	TRSTB recovery time	12.0			ns	
CIN_{TDI}	TDI input pin capacitance			5.3	pf	
CIN_{TMS}	TMS input pin capacitance			5.3	pf	
CIN_{TCK}	TCK input pin capacitance			5.3	pf	
CIN_{TRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			20	MHz	

7.11 User Crypto

The following section describes user crypto.

7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 112 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V – 1	VDD = 1.05 V STD	VDD = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	189		189		MHz	–40 °C to 100 °C

7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Throughput cycle count collected with Athena TeraFire Core and RISCV running at 100 MHz.

Table 113 • AES

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-ECB-128 encrypt[1]	128	515	1095
	64K	50157	933
AES-ECB-128 decrypt[1]	128	557	1760
	64K	48385	1524
AES-ECB-256 encrypt[1]	128	531	1203
	64K	58349	1203
AES-ECB-256 decrypt[1]	128	589	1676
	64K	56673	1671
AES-CBC-256 encrypt[1]	128	576	1169
	64K	52547	1169
AES-CBC-256 decrypt[1]	128	585	1744
	64K	48565	1652
AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1925	2740
	64K	60070	2158
AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1973	2268
	64K	60102	2151

1. With DPA counter measures.

Table 114 • GMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-GCM-256[1], 128-bit tag, (message is only authenticated)	128	1863	2211
	64K	49707	2128