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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	325-LFBGA, FC
Supplier Device Package	325-FCBGA (11x14.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-fcsg325e

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4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
PCI	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45
LVTTL	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89
LVCMOS15	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575
LVCMOS12	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26
SSTL25I[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL25II[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL18I[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL18II[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
PCI	PCIE 3.3 V	0	VDDI			VDDI/2		V
LVTTL33	LVTTL 3.3 V	0	VDDI			VDDI/2		V
LVCMOS33	LVCMOS 3.3 V	0	VDDI			VDDI/2		V
LVCMOS25	LVCMOS 2.5 V	0	VDDI			VDDI/2		V
LVCMOS18	LVCMOS 1.8 V	0	VDDI			VDDI/2		V
LVCMOS15	LVCMOS 1.5 V	0	VDDI			VDDI/2		V
LVCMOS12	LVCMOS 1.2 V	0	VDDI			VDDI/2		V
SSTL25I	SSTL 2.5 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL25II	SSTL 2.5 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL18I	SSTL 1.8 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL18II	SSTL 1.8 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL15I	SSTL 1.5 V Class I	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL15II	SSTL 1.5 V Class II	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL135I	SSTL 1.35 V Class I	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
SSTL135II	SSTL 1.35 V Class II	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
HSTL15I	HSTL 1.5 V Class I	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL15II	HSTL 1.5 V Class II	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL135I	HSTL 1.35 V Class I	V_{REF} – 0.45	V_{REF} + . 45			V_{REF}	0.675	V
HSTL135II	HSTL 1.35 V Class II	V_{REF} – .45	V_{REF} + .45			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	V_{REF} – .4	V_{REF} + .4			V_{REF}	0.60	V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
SLVS25	SLVS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
BLVDSE25[6]	Bus LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MLVDSE25[6]	Multipoint LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
LVPECLE33[6]	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3[1]	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3[1]	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3[1]	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2[1]	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2[1]	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2[1]	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2[1]	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2[1]	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F_{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance[1]	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Global clock F_{MAX}	F_{MAXG}	500	500	500	500	MHz	
Regional clock F_{MAX}	F_{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F_{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T_{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T_{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F_{MAX}	F_{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew[1]	F_{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F_{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F_{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F_{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion[2]	T_{DCB}	90	90	90	90	ps	HSIO without bridging
	T_{DCB}	115	115	115	115	ps	HSIO with bridging
	T_{DCB}	90	90	90	90	ps	GPIO without bridging
	T_{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2 PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F_{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F_{INF}	10		1250	MHz
Minimum reference or feedback pulse width[1]	$F_{INPULSE}$	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F_{PHDETI}	1		312	MHz
Frequency at the PFD (fractional mode)	F_{PHDETF}	10	50	125	MHz
Allowable input duty cycle	F_{INDUTY}	25		75	%

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, se e table Differential DC Input and Output Levels.
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVCMOS25	For DC input levels, see table DC Input and Output Levels.

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115[1]		Ω
Power-up termination			>50K		Ω

1. Measured at VCM= 1.2 V and VID= 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps(–STD) / 12.7 Gbps (–1)[1]		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}		85		Ω	
	V_{OTERM}		100		Ω	
	V_{OTERM}		150		Ω	
Common mode voltage[1]	V_{OCM}	0.44 × V_{DDA}	0.525 × V_{DDA}	0.59 × V_{DDA}	V	DC coupled 50% setting
	V_{OCM}	0.52 × V_{DDA}	0.6 × V_{DDA}	0.66 × V_{DDA}	V	DC coupled 60% setting
	V_{OCM}	0.61 × V_{DDA}	0.7 × V_{DDA}	0.75 × V_{DDA}	V	DC coupled 70% setting
	V_{OCM}	0.63 × V_{DDA}	0.8 × V_{DDA}	0.83 × V_{DDA}	V	DC coupled 80% setting
Rise time[2]	T_{TxRF}	41		70	ps	20% to 80%
Fall time[2]		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew[3]	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew[4]	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time[7]	TTxEITrEntry				ns	
Electrical idle transition exit time[7]	TTxEITrExit				ns	
Electrical idle amplitude	VTxEIpp				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time[8]	$T_{DPLLLock}$				REFCLK UIs	
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}				UI UI	Data rate ≥8.5 Gbps to 12.7 Gbps[9] (Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥3.2 Gbps to 8.5 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥1.6 Gbps to 3.2 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.13 0.02	UI UI	Data rate ≥ 800 Mbps to 1.6 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.06 0.01	UI UI	Data rate = 250 Mbps to 800 Mbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

Table 60 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4 1GbE (1000BASE-T)

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5 SGMII and QSGMII

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6 SDI

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

7.5.7 CPRI

The following table describes CPRI.

Table 66 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps [1]			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps [1]			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5.8 JESD204B

The following table describes JESD204B.

Table 67 • JESD204B

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps		0.35	UI
	6.25 Gbps		0.3	UI
	12.5 Gbps[1]			UI
Receive jitter tolerance	3.125 Gbps	0.56		UI
	6.25 Gbps	0.6		UI
	12.5 Gbps[1]			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T_J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

7.6.5 Digest Time

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		µs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	35	µs
	MPF300T, TL, TS, TLS	33.2	35	µs
	MPF500T, TL, TS, TLS			µs
sNVM digest run time[1]	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	46.6	48.8	µs
	MPF300T, TL, TS, TLS	46.6	48.8	µs
	MPF500T, TL, TS, TLS			µs
User key digest run time[2]	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	525.4	543.3	µs
	MPF300T, TL, TS, TLS	525.4	543.3	µs
	MPF500T, TL, TS, TLS			µs

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T_{FF_ENTRY}		59		µs	
The time from Flash*Freeze exit pin assertion to fabric operational state	$T_{FF\_FABRIC\_UP}$		133		µs	
The time from Flash*Freeze exit pin assertion to I/Os operational	$T_{FF\_IO\_ACTIVE}$		143		µs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T_{DISU}	TDI input setup time	0.0			ns	
T_{DIHD}	TDI input hold time	2.0			ns	
T_{TMSSU}	TMS input setup time	1.5			ns	
T_{TMSHD}	TMS input hold time	1.5			ns	
F_{TCK}	TCK frequency			25	MHz	
T_{TCKDC}	TCK duty cycle	40		60	%	
T_{TDOCQ}	TDO clock to Q out			8.4	ns	C_{LOAD} = 40 pf
T_{RSTBCQ}	TRSTB clock to Q out			23.5	ns	C_{LOAD} = 40 pf
T_{RSTBPW}	TRSTB min pulse width	50			ns	
$T_{RSTBREM}$	TRSTB removal time	0.0			ns	
$T_{RSTBREC}$	TRSTB recovery time	12.0			ns	
CIN_{TDI}	TDI input pin capacitance			5.3	pf	
CIN_{TMS}	TMS input pin capacitance			5.3	pf	
CIN_{TCK}	TCK input pin capacitance			5.3	pf	
CIN_{TRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			20	MHz	

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F_{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T_{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T_{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR_{RAMP}		10		µs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR_{ASSERT}	1			µs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	$DR_{DEASSERT}$	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF_{RAMP}		10		µs	
Minimum FF_EXIT_N assert time	FF_{ASSERT}	1			µs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	$FF_{DEASSERT}$	170			µs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256[1], 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384[1], 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256[1] (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1[1]	512	2386	1579
	64K	77576	990
SHA-256[1]	512	2516	884
	64K	84752	938
SHA-384[1]	1024	4154	884
	64K	100222	938
SHA-512[1]	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384[1]	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155