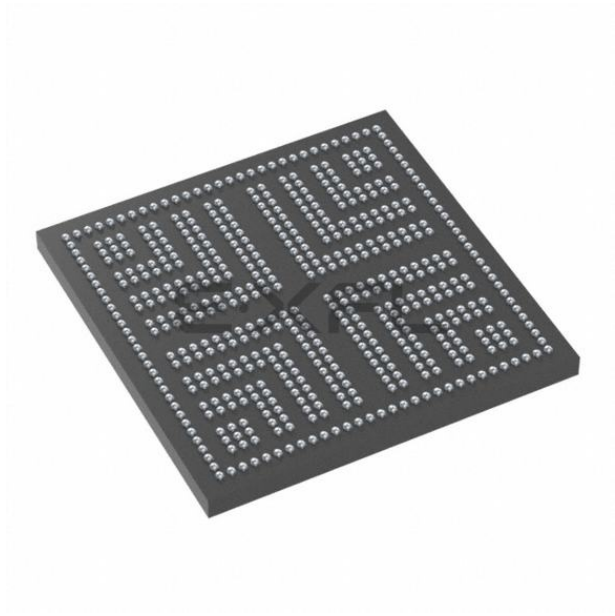

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-fcsg536e

Contents

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V_{DD}	–0.5	1.13	V
Transceiver Tx and Rx lanes supply	V_{DDA}	–0.5	1.13	V
Programming and HSIO receiver supply	V_{DD18}	–0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	–0.5	2.7	V
Transceiver PLL high-voltage supply	V_{DDA25}	–0.5	2.7	V
Transceiver reference clock supply	$V_{DD\_XCVR\_CLK}$	–0.5	3.6	V
Global V_{REF} for transceiver reference clocks	$XCVR_{VREF}$	–0.5	3.6	V
HSIO DC I/O supply[2]	V_{DDIx}	–0.5	2.0	V
GPIO DC I/O supply[2]	V_{DDIx}	–0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V_{DDI3}	–0.5	3.6	V
GPIO auxiliary power supply for I/O bank x[2]	V_{DDAUXx}	–0.5	3.6	V
Maximum DC input voltage on GPIO	V_{IN}	–0.5	3.8	V
Maximum DC input voltage on HSIO	V_{IN}	–0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V_{IN}	–0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V_{IN}	–0.5	3.6	V
Storage temperature (ambient)[1]	T_{STG}	–65	150	°C
Junction temperature[1]	T_J	–55	135	°C
Maximum soldering temperature RoHS	$T_{SOLROHS}$		260	°C
Maximum soldering temperature leaded	T_{SOLPB}		220	°C

1. See FPGA Programming Cycles vs Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode[1]	V_{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode[1]	V_{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less)[1]	V_{DDA}	0.97	1.00	1.03	V

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V_{IN}) Undershoot Duration as % at T_J = 100 °C	Condition (V)
100	–0.5
100	–0.55
100	–0.6
100	–0.65
100	–0.7
100	–0.75
100	–0.8
100	–0.85
100	–0.9
100	–0.95
100	–1
100	–1.05
100	–1.1
100	–1.15
100	–1.2
69	–1.25
45	–1.3

Min (%)	Typ	Max (%)	Unit	Condition
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 80% of V_{DDI}.

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	20	Ω	V_{ICM} < 0.8 V
		–20	100	40	Ω	0.6 V < V_{ICM} < 1.65 V
		–20	100	80	Ω	1.4 V < V_{ICM}
Single-ended thevenin termination[2, 3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

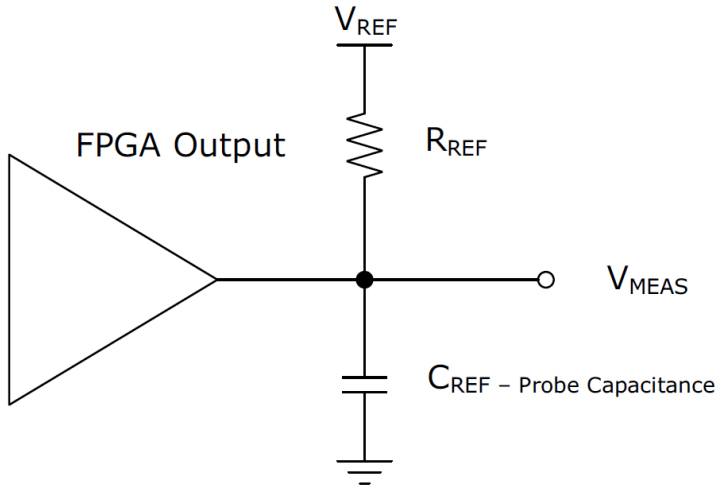
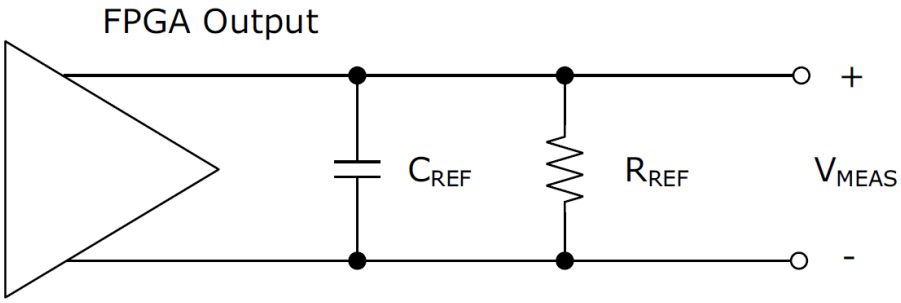


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with V_{ID} ≥200 mV.

7.1.4 Output Buffer Speed

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps

Standard	STD	–1	Unit
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

Parameter[1]	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency[2]	F_{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F_{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	$T_{OUTJITTERP}$			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T_{SKEW}			±200	ps
DLL lock time	T_{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T_{MRPW}	3			ns
Minimum input pulse width[3]	T_{MIPW}	20			ns
Minimum input clock pulse width high	T_{MPWH}	400			ps
Minimum input clock pulse width low	T_{MPWL}	400			ps
Delay step size	T_{DEL}	12.7	30	35	ps
Maximum delay block delay[4]	T_{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input)[5]	T_{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode)[5]	T_{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{2FREQ}		2		MHz
Accuracy	RC_{2FACC}	–4		4	%
Duty cycle	RC_{2DC}	46		54	%
Peak-to-peak output period jitter	RC_{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC_{2CJIT}		5	10	ns
Operating current (V_{DD25})	RC_{2IVPPA}			60	µA
Operating current (V_{DD})	RC_{2IVDD}			2.6	µA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{SCFREQ}		160		MHz
Accuracy	RC_{SCFACC}	–4		4	%
Duty cycle	RC_{SCDC}	47		52	%
Peak-to-peak output period jitter	RC_{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{SCCJIT}			172	ps
Operating current (V_{DD25})	RC_{SCVPPA}			599	µA

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	µA
Operating current (V_{DD})	RC_{SCVDD}			60.7	µA

Table 44 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 45 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1,2]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled[2]	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[3]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode[2]	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode[2]	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, se e table Differential DC Input and Output Levels.
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVCMOS25	For DC input levels, see table DC Input and Output Levels.

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115[1]		Ω
Power-up termination			>50K		Ω

1. Measured at VCM= 1.2 V and VID= 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps(–STD) / 12.7 Gbps (–1)[1]		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps[5]
		0.41			UI	>1.6 to 3.2 Gbps[5]
		0.41			UI	>0.8 to 1.6 Gbps [5]
		0.41			UI	250 to 800 Mpbs [5]
Total jitter tolerance with stressed eye	$T_{TJTOLSE}$	0.65			UI	3.125 Gbps[5]
		0.65			UI	6.25 Gbps[6]
		0.7			UI	10.3125 Gbps[6]
					UI	12.7 Gbps[6, 10]
Sinusoidal jitter tolerance with stressed eye	$T_{SJTOLSE}$	0.1			UI	3.125 Gbps[5]
		0.05			UI	6.25 Gbps[6]
		0.05			UI	10.3125 Gbps[6]
					UI	12.7 Gbps[6, 10]
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

1. Valid at 3.2 Gbps and below.
2. Data vs. Rx reference clock frequency.
3. Achieves compliance with PCIe electrical idle detection.
4. Achieves compliance with SATA OOB specification.
5. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
6. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
7. For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
8. For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
9. Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
10. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53[1]	s
	MPF300T, TL, TS, TLS	90[1]	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37[2]	s
	MPF300T, TL, TS, TLS	55[2]	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

Notes:

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T_{JTAG_ACTIVE}[1, 2]	45	52	ns
	T_{MESH_ERR}[2]	1.8	2.2	µs
	T_{CLK_GLITCH}[1, 2]			ns
	T_{CLK_FREQ}[1, 2]			µs
	T_{LOW_1P05}[2]	70	108	µs
	T_{HIGH_1P8}[2]	85	120	µs
	T_{HIGH_2P5}[2]	130	520	µs
	T_{GLITCH_1P05}[2]			µs
	T_{SECDEC}[1, 2]			µs
	T_{DRI_ERR}[2]	14	18	µs
	T_{WDOG}[1, 2]			µs
	T_{LOCK_ERR}[2]			µs
Time from system controller instruction execution to flag generation	$T_{INST\_BUF\_ACCESS}$[2, 3]	4	5	µs
	T_{INST_DEBUG}[2, 3]	3.3	4	µs
	$T_{INST\_CHK\_DIGEST}$[2, 3]	1.8	3	µs
	$T_{INST\_EC\_SETUP}$[2, 3]	1.8	2	µs
	$T_{INST\_FACT\_PRIV}$[2, 3]	3.8	5	µs
	$T_{INST\_KEY\_VAL}$[2, 3]	2.5	3.1	µs
	T_{INST_MISC}[2, 3]	1.5	2	µs
	$T_{INST\_PASSCODE\_MATCH}$[2, 3]	2.5	3	µs
	$T_{INST\_PASSCODE\_SETUP}$[2, 3]	4.2	5	µs
	T_{INST_PROG}[2, 3]	3.8	4.1	µs
	$T_{INST\_PUB\_INFO}$[2, 3]	4	4.5	µs
	$T_{INST\_ZERO\_RECO}$[2, 3]	2.5	3	µs
	$T_{INST\_PASSCODE\_FAIL}$[2, 3]	170	180	µs
	$T_{INST\_KEY\_VAL\_FAIL}$[2, 3]	92	110	µs
	T_{INST_UNUSED}[2, 3]	4	5	µs
Time from sending the CLEAR to deassertion on FLAG	T_{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	$T_{IO\_DISABLE}$	40	50	ns

7.9.4 Design Dependence of T PUFT and T WRFT

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note T_{PCIE} , T_{XCVR}, T_{LSRAM}, and T_{USRAM} can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$T_{PUFT} = T_{FAB\_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

$T_{WRFT} = T_{FAB\_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

Note: T_{PCIE}, T_{XCVR}, T_{LSRAM}, T_{USRAM}, and T_{CALIB} are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond T_{PUFT} (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

7.9.5 Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 99 • Cold Boot

Power-On (Cold) Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when weak pull-ups are enabled – $T_{PU\_PD\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when fabric is operational – $T_{FAB\_READY(cold)}$	1.20	4.54	7.87	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(cold)}$	1.22	4.56	7.89	ms

7.9.6 Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 100 • Warm Boot

Warm Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when weak pull-ups/pull-downs are enabled – $T_{PU\_PD\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when fabric is operational – $T_{FAB\_READY(warm)}$	0.94	1.79	2.65	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(warm)}$	0.96	1.81	2.67	ms

7.9.7 Miscellaneous Initialization Parameters

In the following table, T_{FAB_READY} refers to either $T_{FAB\_READY(cold)}$ or $T_{FAB\_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T_{FF_ENTRY}		59		µs	
The time from Flash*Freeze exit pin assertion to fabric operational state	$T_{FF\_FABRIC\_UP}$		133		µs	
The time from Flash*Freeze exit pin assertion to I/Os operational	$T_{FF\_IO\_ACTIVE}$		143		µs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T_{DISU}	TDI input setup time	0.0			ns	
T_{DIHD}	TDI input hold time	2.0			ns	
T_{TMSSU}	TMS input setup time	1.5			ns	
T_{TMSHD}	TMS input hold time	1.5			ns	
F_{TCK}	TCK frequency			25	MHz	
T_{TCKDC}	TCK duty cycle	40		60	%	
T_{TDOCQ}	TDO clock to Q out			8.4	ns	C_{LOAD} = 40 pf
T_{RSTBCQ}	TRSTB clock to Q out			23.5	ns	C_{LOAD} = 40 pf
T_{RSTBPW}	TRSTB min pulse width	50			ns	
$T_{RSTBREM}$	TRSTB removal time	0.0			ns	
$T_{RSTBREC}$	TRSTB recovery time	12.0			ns	
CIN_{TDI}	TDI input pin capacitance			5.3	pf	
CIN_{TMS}	TMS input pin capacitance			5.3	pf	
CIN_{TCK}	TCK input pin capacitance			5.3	pf	
CIN_{TRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			20	MHz	

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