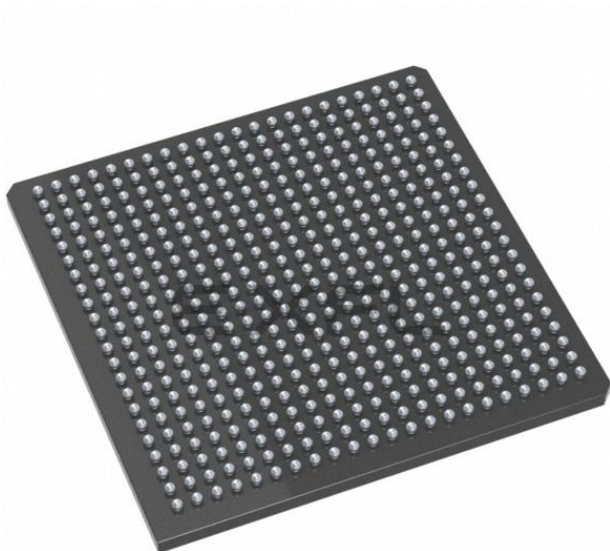




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Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (Tj)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200t-fcvg484e

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3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance ¹	C _{IN} (dedicated GPIO)		5.6	pf	
	C _{IN} (GPIO)		5.6	pf	
	C _{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I _L (GPIO)		10	μA	I/O disabled, high – Z
	I _L (HSIO)		10	μA	I/O disabled, high – Z
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}	T _{RISE}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}	T _{FALL}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Pad pull-up when V _{IN} = 0 ⁵	I _{PU}	137	220	μA	V _{DDIX} = 3.3 V
Pad pull-up when V _{IN} = 0 ⁵		102	166	μA	V _{DDIX} = 2.5 V
Pad pull-up when V _{IN} = 0		68	115	μA	V _{DDIX} = 1.8 V
Pad pull-up when V _{IN} = 0		51	88	μA	V _{DDIX} = 1.5 V
Pad pull-up when V _{IN} = 0 ⁶		29	73	μA	V _{DDIX} = 1.35 V
Pad pull-up when V _{IN} = 0	I _{PD}	16	46	μA	V _{DDIX} = 1.2 V
Pad pull-down when V _{IN} = 3.3 V ⁵		65	187	μA	V _{DDIX} = 3.3 V
Pad pull-down when V _{IN} = 2.5 V ⁵		63	160	μA	V _{DDIX} = 2.5 V
Pad pull-down when V _{IN} = 1.8 V		60	117	μA	V _{DDIX} = 1.8 V
Pad pull-down when V _{IN} = 1.5 V		57	95	μA	V _{DDIX} = 1.5 V
Pad pull-down when V _{IN} = 1.35 V		52	86	μA	V _{DDIX} = 1.35 V
Pad pull-down when V _{IN} = 1.2 V		47	79	μA	V _{DDIX} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
PCI	PCI E 3.3 V	0	VDDI			VDDI/2		V
LVTTTL33	LVTTTL 3.3 V	0	VDDI			VDDI/2		V
LVC MOS33	LVC MOS 3.3 V	0	VDDI			VDDI/2		V
LVC MOS25	LVC MOS 2.5 V	0	VDDI			VDDI/2		V
LVC MOS18	LVC MOS 1.8 V	0	VDDI			VDDI/2		V
LVC MOS15	LVC MOS 1.5 V	0	VDDI			VDDI/2		V
LVC MOS12	LVC MOS 1.2 V	0	VDDI			VDDI/2		V
SSTL25I	SSTL 2.5 V Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	1.25	V
SSTL25II	SSTL 2.5 V Class II	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	1.25	V
SSTL18I	SSTL 1.8 V Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	0.90	V
SSTL18II	SSTL 1.8 V Class II	$V_{REF} - 0.5$	$V_{REF} + 0.5$			V_{REF}	0.90	V
SSTL15I	SSTL 1.5 V Class I	$V_{REF} - .175$	$V_{REF} + .175$			V_{REF}	0.75	V
SSTL15II	SSTL 1.5 V Class II	$V_{REF} - .175$	$V_{REF} + .175$			V_{REF}	0.75	V
SSTL135I	SSTL 1.35 V Class I	$V_{REF} - .16$	$V_{REF} + .16$			V_{REF}	0.675	V
SSTL135II	SSTL 1.35 V Class II	$V_{REF} - .16$	$V_{REF} + .16$			V_{REF}	0.675	V
HSTL15I	HSTL 1.5 V Class I	$V_{REF} - .5$	$V_{REF} + .5$			V_{REF}	0.75	V
HSTL15II	HSTL 1.5 V Class II	$V_{REF} - .5$	$V_{REF} + .5$			V_{REF}	0.75	V
HSTL135I	HSTL 1.35 V Class I	$V_{REF} - 0.45$	$V_{REF} + .45$			V_{REF}	0.675	V
HSTL135II	HSTL 1.35 V Class II	$V_{REF} - .45$	$V_{REF} + .45$			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	$V_{REF} - .4$	$V_{REF} + .4$			V_{REF}	0.60	V

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSTL135II	Differential HSTL 1.35 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

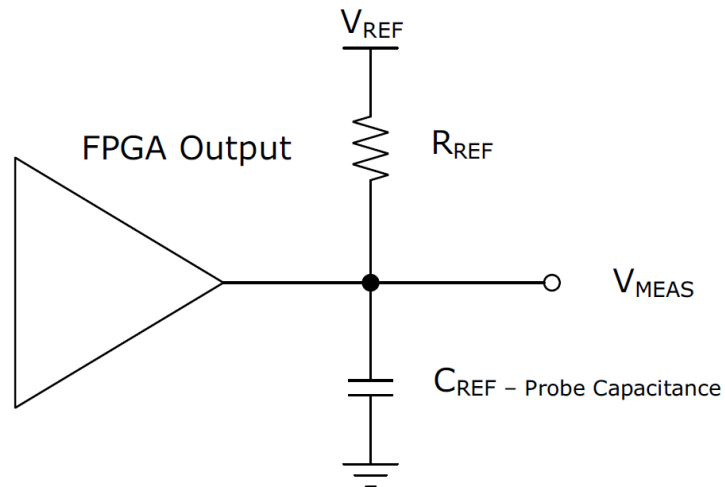
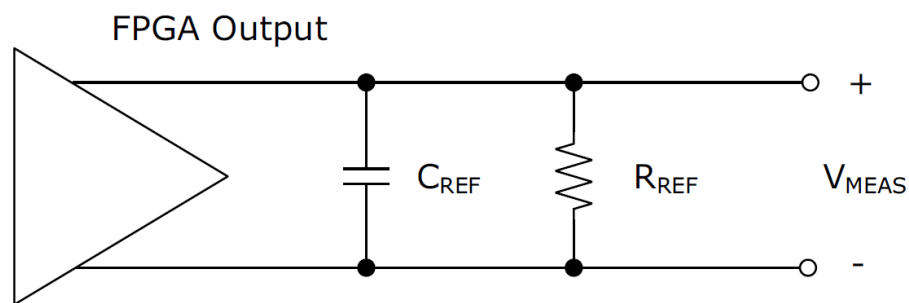
1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H . All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in [Output Delay Measurement—Single-Ended Test Setup](#) (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCI 3.3 V	25	10	1.65	
LVTTTL33	LVTTTL 3.3 V	1M	0	1.65	
LVC MOS33	LVC MOS 3.3 V	1M	0	1.65	
LVC MOS25	LVC MOS 2.5 V	1M	0	1.25	
LVC MOS18	LVC MOS 1.8 V	1M	0	0.90	
LVC MOS15	LVC MOS 1.5 V	1M	0	0.75	
LVC MOS12	LVC MOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

Figure 2 • Output Delay Measurement—Differential Test Setup


7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	-1	Unit
LVDS18	1250	1250	Mbps
RDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3 ¹	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3 ¹	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3 ¹	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2 ¹	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2 ¹	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2 ¹	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2 ¹	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2 ¹	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F _{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance ¹	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Global clock F _{MAX}	F _{MAXG}	500	500	500	500	MHz	
Regional clock F _{MAX}	F _{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F _{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T _{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks) ²	F _{MAXINJ}		120	1000	ps
PLL VCO frequency	F _{VCO}	800		5000	MHz
Loop bandwidth (Int) ³	F _{BW}	F _{PHDET} /55	F _{PHDET} /44	F _{PHDET} /30	MHz
Loop bandwidth (FRAC) ³	F _{BW}	F _{PHDET} /91	F _{PHDET} /77	F _{PHDET} /56	MHz
Static phase offset of the PLL outputs ⁴	T _{SPO}			Max (±60 ps, ±0.5 degrees)	ps
	T _{OUTJITTER}				ps
PLL output duty cycle precision	T _{OUTDUTY}	48		54	%
PLL lock time ⁵	T _{LOCK}			Max (6.0 μs, 625 PFD cycles)	μs
PLL unlock time ⁶	T _{UNLOCK}	2		8	PFD cycles
PLL output frequency	F _{OUT}	0.050		1250	MHz
Minimum reset pulse width	T _{MRPW}				μs
Maximum delay in the feedback path ⁷	F _{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread ⁸	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency ⁹	Mod_Freq	F _{PHDET} /(128x63)	32	F _{PHDET} /(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3

DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter ¹	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F _{INF}	133		800	MHz
Input feedback clock frequency	F _{INFDBF}	133		800	MHz
Primary output clock frequency	F _{OUTPF}	133		800	MHz

Table 60 • 10GbE (RXAU)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4**1GbE (1000BASE-T)**

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5**SGMII and QSGMII**

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6**SDI**

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T _J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is $20 \times LF = 20 \times .8 = 16$ years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is $10 \times LF$ or 10 years over the industrial temperature range.

7.6.5**Digest Time**

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		μs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	35	μs
	MPF300T, TL, TS, TLS	33.2	35	μs
	MPF500T, TL, TS, TLS			μs
sNVM digest run time ¹	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	46.6	48.8	μs
	MPF300T, TL, TS, TLS	46.6	48.8	μs
	MPF500T, TL, TS, TLS			μs
User key digest run time ²	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	525.4	543.3	μs
	MPF300T, TL, TS, TLS	525.4	543.3	μs
	MPF500T, TL, TS, TLS			μs

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1,4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1,2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1,3}			s	Full scrubbing
Time to scrub the fabric data PNVM data (non-recoverable) ^{1,4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 79 • Zeroization Times for MPF300T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1,2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1,4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1,2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1,3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ^{1,4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 80 • Zeroization Times for MPF500T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1,2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T _{SNVM_Rd}	18H				Note 1
Digital signature service raw	T _{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T _{SIG_DER}	1AH	174	187	ms	
Reserved		1BH– 1FH				
PUF emulation	T _{Challenge}	20H	1.8	2.0	ms	
Nonce service	T _{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	T _{BIT_AUTH}	22H				Note 4
IAP Image authentication	T _{IAP_AUTH}	23H				Note 4
Reserved		26H–3FH				
In application programming by index	T _{IAP_Prg_Index}	42H				Note 2
In application programming by SPI address	T _{IAP_Prg_Addr}	43H				Note 2
In application verify by index	T _{IAP_Ver_Index}	44H				Note 5
In application verify by SPI address	T _{IAP_Ver_Addr}	45H				Note 5
Auto update	T _{AutoUpdate}	46H				Note 2
Digest check	T _{digest_chk}	47H				Note 3

1. See [sNVM Read/Write Characteristics](#) (see page 58).
2. See [SPI Master Programming Time](#) (see page 52).
3. See [Digest Times](#) (see page 54).
4. See [Authentication Services Time](#) (see page 58).
5. See [Verify Services Time](#) (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

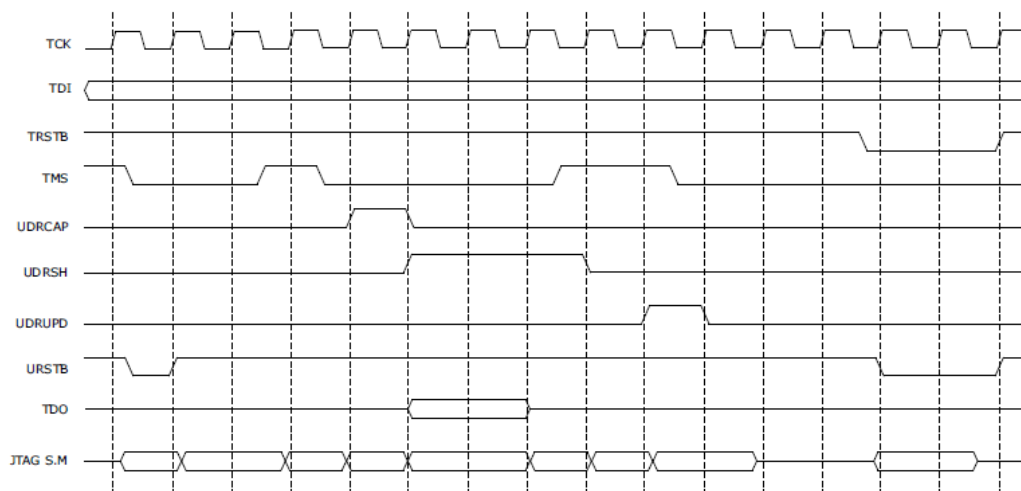
This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}			25	MHz	

Figure 3 • UJTAG Timing Diagram

7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 89 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}				MHz	

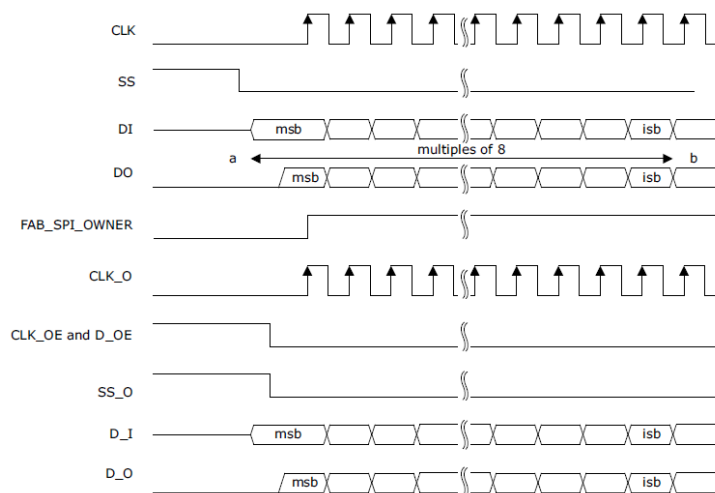
7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

Table 90 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V _{DDI} = 3.3 V Max	V _{DDI} = 2.5 V Max	V _{DDI} = 1.8 V Max	V _{DDI} = 1.5 V Max	V _{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins ¹	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Figure 4 • USPI Switching Characteristics

7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	

7.11 User Crypto

The following section describes user crypto.

7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 112 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V – 1	VDD = 1.05 V STD	VDD = 1.05 V – 1	Unit	Condition
Operating frequency	F _{MAX}	189		189		MHz	–40 °C to 100 °C

7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Throughput cycle count collected with Athena TeraFire Core and RISCv running at 100 MHz.

Table 113 • AES

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-ECB-128 encrypt ¹	128	515	1095
	64K	50157	933
AES-ECB-128 decrypt ¹	128	557	1760
	64K	48385	1524
AES-ECB-256 encrypt ¹	128	531	1203
	64K	58349	1203
AES-ECB-256 decrypt ¹	128	589	1676
	64K	56673	1671
AES-CBC-256 encrypt ¹	128	576	1169
	64K	52547	1169
AES-CBC-256 decrypt ¹	128	585	1744
	64K	48565	1652
AES-GCM-128 encrypt ¹ , 128-bit tag, (full message encrypted/authenticated)	128	1925	2740
	64K	60070	2158
AES-GCM-256 encrypt ¹ , 128-bit tag, (full message encrypted/authenticated)	128	1973	2268
	64K	60102	2151

1. With DPA counter measures.

Table 114 • GMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-GCM-256 ¹ , 128-bit tag, (message is only authenticated)	128	1863	2211
	64K	49707	2128

SigVer, DSA-2048/SHA-256	1024	9810527	10884
	8K	9597000	10719
Key Agreement (KAS), DH-3072 (p=3072, security=256)		4920705	9338
Key Agreement (KAS), DH-3072 (p=3072, security=256) ¹		78914533	9083

1. With DPA counter measures.

Table 122 • NRBG

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string		18221	2841
Reseed: no additional input, s=256		13585	1180
Reseed: 384-bit additional input, s=256		15922	1342
Generate: (no additional input), prediction resistance enabled, s= 256	128	15262	1755
	8K	27169	8223
Generate: (no additional input), prediction resistance disabled, s= 256	128	2138	1167
	8K	14045	8223
Generate: (384-bit additional input), prediction resistance enabled, s= 256	128	21299	1944
	8K	33206	8949
Generate: (384-bit additional input), prediction resistance disabled, s= 256	128	11657	1894
	8K	23564	8950
Un-instantiate		761	666

1. With DPA counter measures.