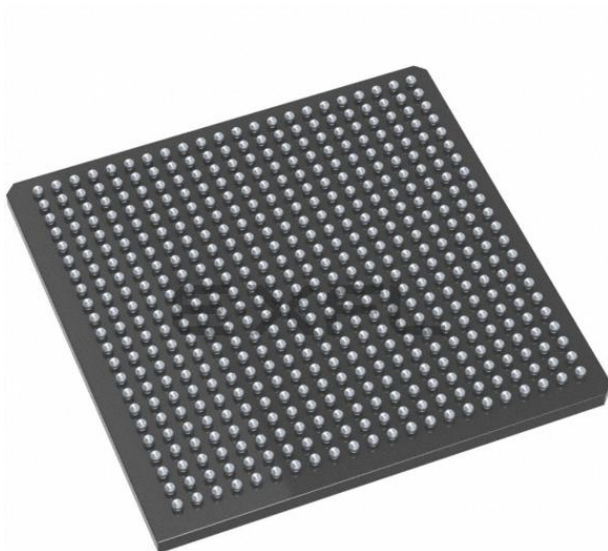




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200tl-fcg484e

2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps) ¹	V _{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V _{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V _{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	V _{DD_XCVR_CLK}	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	V _{DD_XCVR_CLK}	2.375	2.5	2.625	V
Global V _{REF} for transceiver reference clocks ³	XCVR _{VREF}	Ground		V _{DD_XCVR_CLK}	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V ⁴	V _{DDI_x}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V ^{2,4}	V _{DDI_x}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V _{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDI_x} = 3.3 V nominal ^{2,4}	V _{DDAUX_x}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDI_x} = 2.5 V nominal or lower ^{2,4}	V _{DDAUX_x}	2.375	2.5	2.625	V
Extended commercial temperature range	T _J	0		100	°C
Industrial temperature range	T _J	–40		100	°C
Extended commercial programming temperature range	T _{PRG}	0		100	°C
Industrial programming temperature range	T _{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDI_x} is 2.5 V nominal or 3.3 V nominal, V_{DDAUX_x} must be connected to the V_{DDI_x} supply for that bank. If V_{DDI_x} for a given GPIO bank is <2.5 V nominal, V_{DDAUX_x} per I/O bank must be powered at 2.5 V nominal.
3. XCVR_{VREF} globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near V_{DD_XCVR_CLK}/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDI_x and VDDAUX_x.

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

Table 13 • DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
PCI ¹	3.15	3.3	3.45		0.1 x V _{DDI}	0.9 x V _{DDI}		1.5	0.5
LVTTL	3.15	3.3	3.45		0.4	2.4			
LVC MOS33	3.15	3.3	3.45		0.4	V _{DDI} – 0.4			
LVC MOS25	2.375	2.5	2.625		0.4	V _{DDI} – 0.4			
LVC MOS18	1.71	1.8	1.89		0.45	V _{DDI} – 0.45			
LVC MOS15	1.425	1.5	1.575		0.25 x V _{DDI}	0.75 x V _{DDI}			
LVC MOS12	1.14	1.2	1.26		0.25 x V _{DDI}	0.75 x V _{DDI}			
SSTL25I ³	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608		8.1	8.1
SSTL25II ³	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810		16.2	16.2
SSTL18I ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		6.7	6.7
SSTL18II ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		16	16

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
HCSL25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18 ⁵	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V _{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V _{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} – 0.4 V;
 - b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
 - c. V_{ICM} – V_{ID}/2 must be >V_{SS} – 0.3 V;
 - d. Any differential input with V_{ICM} ≤ 0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. V_{DDI} = 1.8 V, V_{DDAUX} = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15 ³	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25 ³	GPIO		1.25		0.24	0.262	0.272

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to $V_{SS}^{4,5}$	Internal	-20	120	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$
	parallel termination to V_{SS}	-20	240	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} .
3. For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.
4. Measured at 50% of V_{DDI} .
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

Standard	Description	V_I^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSUL18I	HSUL 1.8 V Class I	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	$V_{REF} -$.22	$V_{REF} +$.22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
SLVS33	Scalable low- voltage signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

Standard	STD	–1	Unit
LVC MOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LC MDS25	1250	1250	Mbps
LVDS33/LC MDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLV DSE25	500	500	Mbps
MLV DSE25	500	500	Mbps
LVPECE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LV TTL33 (20 mA)	500	500	Mbps
LVC MOS33 (20 mA)	500	500	Mbps
LVC MOS25 (16 mA)	500	500	Mbps
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps
LVC MOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
F _{MAX}	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
F _{MAX}	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
F _{MAX}	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
F _{MAX}	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
F _{MAX}	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
F _{MAX}	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
F _{MAX} 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter ¹	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency ²	F _{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F _{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	T _{OUTJITTERP}			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T _{SKEW}			±200	ps
DLL lock time	T _{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T _{MRPW}	3			ns
Minimum input pulse width ³	T _{MIPW}	20			ns
Minimum input clock pulse width high	T _{MPWH}	400			ps
Minimum input clock pulse width low	T _{MPWL}	400			ps
Delay step size	T _{DEL}	12.7	30	35	ps
Maximum delay block delay ⁴	T _{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input) ⁵	T _{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode) ⁵	T _{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4

RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{2FREQ}		2		MHz
Accuracy	RC _{2FACC}	−4		4	%
Duty cycle	RC _{2DC}	46		54	%
Peak-to-peak output period jitter	RC _{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC _{2CIIT}		5	10	ns
Operating current (V _{DD25})	RC _{2IVPPA}			60	μA
Operating current (V _{DD})	RC _{2IVDD}			2.6	μA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{SCFREQ}		160		MHz
Accuracy	RC _{SCFACC}	−4		4	%
Duty cycle	RC _{SCDC}	47		52	%
Peak-to-peak output period jitter	RC _{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC _{SCCIIT}			172	ps
Operating current (V _{DD25})	RC _{SCVPPA}			599	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

Table 44 • μ SRAM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	T_{ac}		2		2	ns	Read-port

Table 45 • μ PROM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit
Read access time	T_{ac}	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Tx data rate ^{1,2}	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled ²	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency ³	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode ²	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode ²	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Reference clock input rate ^{1,2}	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps ¹			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps ¹			UI

- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

Retention Since Programmed (N = Number Digests During that Time) ¹										
Digest T _i	Storage and Operating T _j	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	34.9	μs
	MPF300T, TL, TS, TLS	33.2	34.9	μs
	MPF500T, TL, TS, TLS			μs
Factory digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	493.6	510.1	μs
	MPF300T, TL, TS, TLS	493.6	510.1	μs
	MPF500T, TL, TS, TLS			μs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1, 3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1, 4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1, 2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1, 3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ^{1, 4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1, 2}			ms	One iteration of scrubbing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	μs	
Authenticated and decrypted text read		159.59	160.53	166.5	μs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

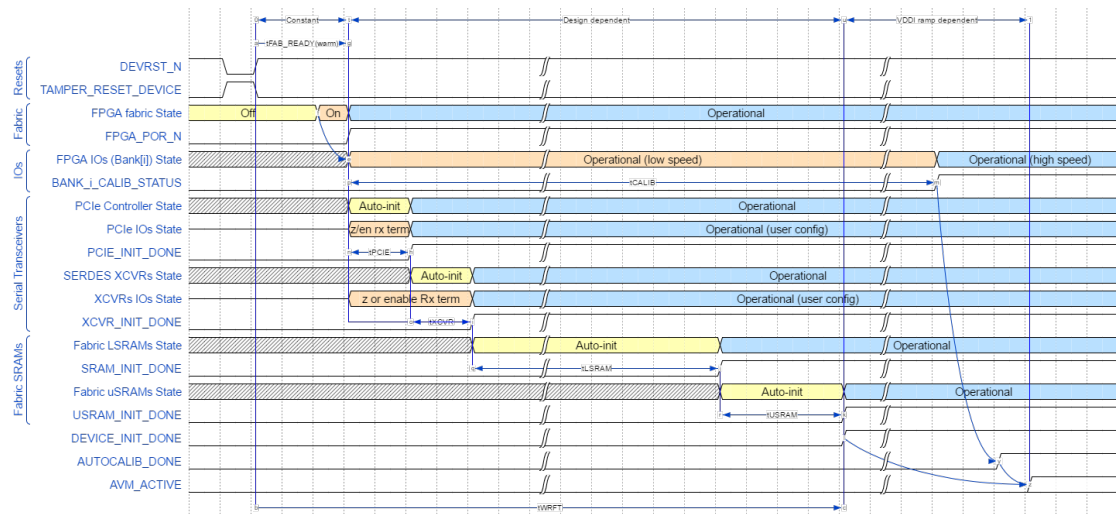
This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	μs	
User code	T_{User}	01H	0.8	1.05	μs	
Design information	T_{Design}	02H	2.4	2.7	μs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	μs	
Query security locks	T_{sec_Query}	05H	15	17	μs	
Read debug information	T_{Rd_debug}	06H	34	38	μs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM_Wr_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM_Wr_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM_Wr_Cipher}$	12H				Note 1
Reserved		13H–17H				

Figure 6 • Warm Reset Timing

7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

7.9.4 Design Dependence of T_{PUFT} and T_{WRFT}

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note T_{PCIE} , T_{XCVR} , T_{LSRAM} , and T_{USRAM} can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$$T_{PUFT} = T_{FAB_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

$$T_{WRFT} = T_{FAB_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

Note: T_{PCIE} , T_{XCVR} , T_{LSRAM} , T_{USRAM} , and T_{CALIB} are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond T_{PUFT} (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

7.9.5 Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA I/Os are functional for low-speed (sub 400 MHz) operation.

Table 99 • Cold Boot

Power-On (Cold) Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when weak pull-ups are enabled – $T_{PU_PD_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when fabric is operational – $T_{FAB_READY(cold)}$	1.20	4.54	7.87	ms
Time when output pins start driving – $T_{OUT_ACTIVE(cold)}$	1.22	4.56	7.89	ms

7.9.6 Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA I/Os are functional for low-speed (sub 400 MHz) operation.

Table 100 • Warm Boot

Warm Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when weak pull-ups/pull-downs are enabled – $T_{PU_PD_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when fabric is operational – $T_{FAB_READY(warm)}$	0.94	1.79	2.65	ms
Time when output pins start driving – $T_{OUT_ACTIVE(warm)}$	0.96	1.81	2.67	ms

7.9.7 Miscellaneous Initialization Parameters

In the following table, T_{FAB_READY} refers to either $T_{FAB_READY(cold)}$ or $T_{FAB_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 ¹ , 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384 ¹ , 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256 ¹ (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 ¹	512	2386	1579
	64K	77576	990
SHA-256 ¹	512	2516	884
	64K	84752	938
SHA-384 ¹	1024	4154	884
	64K	100222	938
SHA-512 ¹	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384 ¹	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155