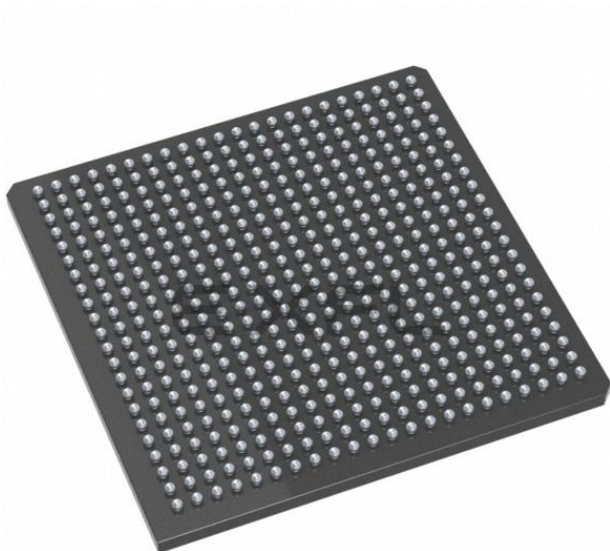




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200tl-fcg484i

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see [System Services \(see page 59\)](#).
- The Non-Volatile Characteristics section was updated. For more information, see [Non-Volatile Characteristics \(see page 51\)](#).
- The Fabric Macros section was updated. For more information, see [Fabric Macros \(see page 60\)](#).
- The Transceiver Switching Characteristics section was updated. For more information, see [Transceiver Switching Characteristics \(see page 42\)](#).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see [HSIO Maximum Input Buffer Speed](#) and [HSIO Maximum Output Buffer Speed](#).
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see [I/O Standards Specifications](#).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see [Non-Volatile Characteristics](#).
- A note was added defining power down conditions for programming recovery conditions. For more information, see [Power-Supply Ramp Times](#).

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	−0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	−0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	−0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	−0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	−0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	−0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	−0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	−0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	−0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	−0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	−0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	−0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	−0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	−0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	−0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	−65	150	°C
Junction temperature ¹	T _J	−55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at $T_J = 100\text{ }^{\circ}\text{C}$	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

Note: Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot Duration as % at $T_J = 100\text{ }^{\circ}\text{C}$	Condition (V)
100	-0.05
100	-0.1
100	-0.15
100	-0.2
100	-0.25
100	-0.3
100	-0.35
100	-0.4
44	-0.45
14	-0.5
4.8	-0.55
1.6	-0.6

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section [Recommended Operating Conditions](#) (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V _{DD}	0.2	50	ms
Transceiver core supply	V _{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V _{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V _{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V _{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	V _{DDI} [0,1,6,7]	0.2	50	ms
GPIO bank I/O power supplies	V _{DDI} [2,4,5]	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V _{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	V _{DDAUX} [2,4,5]	0.2	50	ms
Transceiver reference clock supply	V _{DD_XCVR_CLK}	0.2	50	ms
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended) ^{1, 2}	XCVR _{RX_HS}			±4	mA	V _{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended) ³	XCVR _{TX_HS}			±10	mA	V _{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended) ⁴	XCVR _{REF_HS}			±1	mA	V _{DD_XCVR_CLK} = 0 V
Current per GPIO pin (P or N single-ended) ⁵	I _{GPIO_HS}			±1	mA	V _{DDI_X} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

- Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
- Each P and N transceiver input has less than the specified maximum input current.
- Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
- V_{DD_XCVR_CLK} is powered down and the device is driven to –0.3 V < V_{IN} < V_{DD_XCVR_CLK}.
- V_{DDI_X} is powered down and the device is driven to –0.3 V < V_{IN} < GPIO V_{DDI_{max}}.

Table 13 • DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
PCI ¹	3.15	3.3	3.45		0.1 x V _{DDI}	0.9 x V _{DDI}		1.5	0.5
LVTTL	3.15	3.3	3.45		0.4	2.4			
LVC MOS33	3.15	3.3	3.45		0.4	V _{DDI} – 0.4			
LVC MOS25	2.375	2.5	2.625		0.4	V _{DDI} – 0.4			
LVC MOS18	1.71	1.8	1.89		0.45	V _{DDI} – 0.45			
LVC MOS15	1.425	1.5	1.575		0.25 x V _{DDI}	0.75 x V _{DDI}			
LVC MOS12	1.14	1.2	1.26		0.25 x V _{DDI}	0.75 x V _{DDI}			
SSTL25I ³	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608		8.1	8.1
SSTL25II ³	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810		16.2	16.2
SSTL18I ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		6.7	6.7
SSTL18II ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		16	16

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks) ²	F _{MAXINJ}		120	1000	ps
PLL VCO frequency	F _{VCO}	800		5000	MHz
Loop bandwidth (Int) ³	F _{BW}	F _{PHDET} /55	F _{PHDET} /44	F _{PHDET} /30	MHz
Loop bandwidth (FRAC) ³	F _{BW}	F _{PHDET} /91	F _{PHDET} /77	F _{PHDET} /56	MHz
Static phase offset of the PLL outputs ⁴	T _{SPO}			Max (±60 ps, ±0.5 degrees)	ps
	T _{OUTJITTER}				ps
PLL output duty cycle precision	T _{OUTDUTY}	48		54	%
PLL lock time ⁵	T _{LOCK}			Max (6.0 μs, 625 PFD cycles)	μs
PLL unlock time ⁶	T _{UNLOCK}	2		8	PFD cycles
PLL output frequency	F _{OUT}	0.050		1250	MHz
Minimum reset pulse width	T _{MRPW}				μs
Maximum delay in the feedback path ⁷	F _{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread ⁸	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency ⁹	Mod_Freq	F _{PHDET} /(128x63)	32	F _{PHDET} /(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3

DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter ¹	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F _{INF}	133		800	MHz
Input feedback clock frequency	F _{INFDBF}	133		800	MHz
Primary output clock frequency	F _{OUTPF}	133		800	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver RX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see [UG0677: PolarFire FPGA Transceiver User Guide](#).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps ⁵
		0.41			UI	>1.6 to 3.2 Gbps ⁵
		0.41			UI	>0.8 to 1.6 Gbps ⁵
		0.41			UI	250 to 800 Mbps ⁵
Total jitter tolerance with stressed eye	T _{TJOLSE}	0.65			UI	3.125 Gbps ⁵
		0.65			UI	6.25 Gbps ⁶
		0.7			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
Sinusoidal jitter tolerance with stressed eye	T _{SJTOLSE}	0.1			UI	3.125 Gbps ⁵
		0.05			UI	6.25 Gbps ⁶
		0.05			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

- Valid at 3.2 Gbps and below.
- Data vs. Rx reference clock frequency.
- Achieves compliance with PCIe electrical idle detection.
- Achieves compliance with SATA OOB specification.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

7.5.7 CPRI

The following table describes CPRI.

Table 66 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5.8 JESD204B

The following table describes JESD204B.

Table 67 • JESD204B

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps		0.35	UI
	6.25 Gbps		0.3	UI
	12.5 Gbps ¹			UI
Receive jitter tolerance	3.125 Gbps	0.56		UI
	6.25 Gbps	0.6		UI
	12.5 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

Retention Since Programmed (N = Number Digests During that Time) ¹										
Digest T _i	Storage and Operating T _i	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T _J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is $20 \times LF = 20 \times .8 = 16$ years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is $10 \times LF$ or 10 years over the industrial temperature range.

7.6.5**Digest Time**

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		μs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	35	μs
	MPF300T, TL, TS, TLS	33.2	35	μs
	MPF500T, TL, TS, TLS			μs
sNVM digest run time ¹	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	46.6	48.8	μs
	MPF300T, TL, TS, TLS	46.6	48.8	μs
	MPF500T, TL, TS, TLS			μs
User key digest run time ²	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	525.4	543.3	μs
	MPF300T, TL, TS, TLS	525.4	543.3	μs
	MPF500T, TL, TS, TLS			μs

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable) ^{1, 4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1, 2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1, 3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ¹			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53 ¹	s
	MPF300T, TL, TS, TLS	90 ¹	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37 ²	s
	MPF300T, TL, TS, TLS	55 ²	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

Notes:

- Standalone verify is limited to 2,000 total device hours over the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

