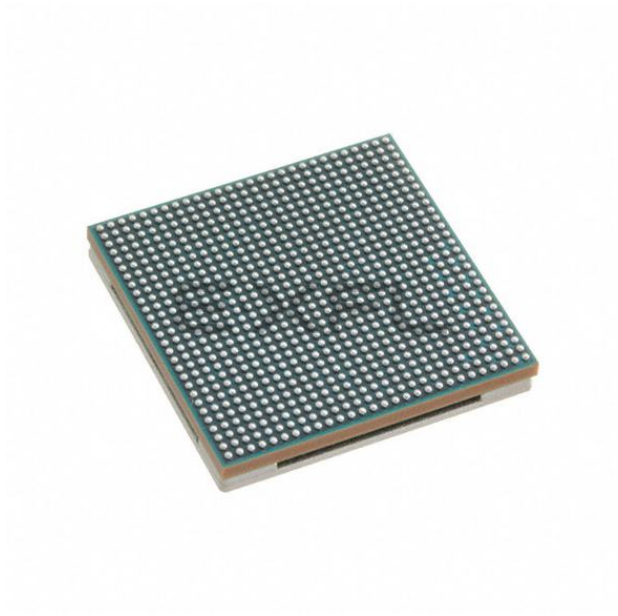

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 192000 |
| Total RAM Bits | 13619200 |
| Number of I/O | 364 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.08V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 784-BBGA, FCBGA |
| Supplier Device Package | 784-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/mpf200tl-fcg784i |

# 2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C $T_J$) and extended commercial temperature range (0 °C to 100 °C $T_J$). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply $V_{DD}$ can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply $V_{DDA}$ can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage ($V_{IN}$) overshoot duration for HSIO.

**Table 6 • Maximum Overshoot During Transitions for HSIO**

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 1.8 |
| 100 | 1.85 |
| 100 | 1.9 |
| 100 | 1.95 |
| 100 | 2 |
| 100 | 2.05 |
| 100 | 2.1 |
| 100 | 2.15 |
| 100 | 2.2 |
| 90 | 2.25 |
| 30 | 2.3 |
| 7.5 | 2.35 |
| 1.9 | 2.4 |

**Note:** Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage ($V_{IN}$) undershoot duration for HSIO.

**Table 7 • Maximum Undershoot During Transitions for HSIO**

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | –0.05 |
| 100 | –0.1 |
| 100 | –0.15 |
| 100 | –0.2 |
| 100 | –0.25 |
| 100 | –0.3 |
| 100 | –0.35 |
| 100 | –0.4 |
| 44 | –0.45 |
| 14 | –0.5 |
| 4.8 | –0.55 |
| 1.6 | –0.6 |

The following table shows the maximum AC input voltage ($V_{IN}$) overshoot duration for GPIO.

**Note**: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

## 6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

### 6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

**Table 12 • DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$[1] Max (V) |
|---|---|---|---|---|---|---|---|
| PCI | 3.15 | 3.3 | 3.45 | –0.3 | 0.3 × $V_{DDI}$ | 0.5 × $V_{DDI}$ | 3.45 |
| LVTTL | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 2.625 |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.89 |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.575 |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.26 |
| SSTL25I[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL25II[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL18I[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL18II[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| SSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| RSDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| MINILVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| SUBLVDS33 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS18[5] | HSIO | Mid (default) | 0.6 | 0.9 | 1.65 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS25 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS18[5] | HSIO | Mid (default) | 0.6 | 0.8 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| SLVS33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS18[5] | HSIO | Mid (default) | 0.6 | 1.00 | 1.65 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.3 |
| HCSL33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| HCSL25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL18[5] | HSIO | Mid (default) | 0.6 | 1.0 | 1.65 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.55 | 1.1 |
| BUSLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.1 | $V_{DDIn}$ |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.1 | $V_{DDIn}$ |
| MLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.35 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.35 | 2.4 |
| LVPECL33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| LVPECLE33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| MIPI25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.05 | 0.2 | 0.3 |

1. $V_{ICM}$ is the input common mode.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
   a. $V_{ICM}$ must be less than $V_{DDI}$ – 0.4 V;
   b. $V_{ICM}$ + $V_{ID}$/2 must be <$V_{DDI}$ + 0.4 V;
   c. $V_{ICM}$ – $V_{ID}$/2 must be >VSS – 0.3 V;
   d. Any differential input with $V_{ICM}$ ≤0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

### Table 15 • Differential DC Output Levels

| I/O Standard | Bank Type | $V_{OCM}$[1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$[2] Min (V) | $V_{OD}$[2] Typ (V) | $V_{OD}$[2] Max (V) |
|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | | 1.2 | | 0.25 | 0.35 | 0.45 |
| LVDS25 | GPIO | | 1.2 | | 0.25 | 0.35 | 0.45 |
| LCMDS33 | GPIO | | 0.6 | | 0.25 | 0.35 | 0.45 |
| LCMDS25 | GPIO | | 0.6 | | 0.25 | 0.35 | 0.45 |
| RSDS33 | GPIO | | 1.2 | | 0.17 | 0.2 | 0.23 |
| RSDS25 | GPIO | | 1.2 | | 0.17 | 0.2 | 0.23 |
| MINILVDS33 | GPIO | | 1.2 | | 0.3 | 0.4 | 0.6 |
| MINILVDS25 | GPIO | | 1.2 | | 0.3 | 0.4 | 0.6 |
| SUBLVDS33 | GPIO | | 0.9 | | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | | 0.9 | | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | | 0.8 | | 0.17 | 0.2 | 0.23 |
| PPDS25 | GPIO | | 0.8 | | 0.17 | 0.2 | 0.23 |
| SLVSE15[3] | GPIO, HSIO | | 0.2 | | 0.12 | 0.135 | 0.15 |
| BUSLVDSE25[3] | GPIO | | 1.25 | | 0.24 | 0.262 | 0.272 |

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3,4] | $V_{REF}$[1,5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSTL135II | Differential HSTL 1.35 V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.675 | 0 | | V |
| HSTL12 | Differential HSTL 1.2 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | | V |
| HSUL18I | Differential HSUL 1.8 V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| HSUL18II | Differential HSUL 1.8 V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| HSUL12 | Differential HSUL 1.2 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | | V |
| POD12I | Differential POD 1.2 V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | | V |
| POD12II | Differential POD 1.2 V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | | V |
| MIPI25 | Mobile Industry Processor Interface | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | | V |

1. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst-case of these measurements. $V_{REF}$ values listed are typical. Input waveform switches between $V_L$ and $V_H$. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV $V_{ID}$ for timing. $V_{CM}$ is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the $V_{REF}$/$V_{MEAS}$ parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

### 7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

**Table 23 • Output Delay Measurement Methodology**

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| PCI | PCIE 3.3 V | 25 | 10 | 1.65 | |
| LVTTL33 | LVTTL 3.3 V | 1M | 0 | 1.65 | |
| LVCMOS33 | LVCMOS 3.3 V | 1M | 0 | 1.65 | |
| LVCMOS25 | LVCMOS 2.5 V | 1M | 0 | 1.25 | |
| LVCMOS18 | LVCMOS 1.8 V | 1M | 0 | 0.90 | |
| LVCMOS15 | LVCMOS 1.5 V | 1M | 0 | 0.75 | |
| LVCMOS12 | LVCMOS 1.2 V | 1M | 0 | 0.60 | |
| SSTL25I | Stub-series terminated logic 2.5 V Class I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL25II | SSTL 2.5 V Class II | 50 | 0 | $V_{REF}$ | 1.25 |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|---|---|
| FMAX 4:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 8:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 2:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 4:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|---|---|
| FMAX 8:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |

**Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|---|---|
| Output FMAX | TX_SDR_G_A | Tx SDR | | | | | | | MHz | From a global clock source, aligned[1] |
| | TX_SDR_G_C | Tx SDR | | | | | | | MHz | From a global clock source, centered[1] |

1. A centered clock-to-data interface can be created with a negedge launch of the data.

**Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|---|---|
| Output FMAX | TX_DDR_G_A | Tx DDR | | | 335 | | | 335 | MHz | From a global clock source, aligned |
| | TX_DDR_G_C | Tx DDR | | | 335 | | | 335 | MHz | From a global clock source, centered |
| | TX_DDR_L_A | Tx DDR | | | 250 | | | 250 | MHz | From a lane clock source, aligned |
| | TX_DDR_L_C | Tx DDR | | | 250 | | | 250 | MHz | From a lane clock source, centered |
| Output FMAX 2:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| Output FMAX 4:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| Output FMAX 8:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Maximum input period clock jitter (reference and feedback clocks)[2] | $F_{MAXINJ}$ | | 120 | 1000 | ps |
| PLL VCO frequency | $F_{VCO}$ | 800 | | 5000 | MHz |
| Loop bandwidth (Int)[3] | $F_{BW}$ | $F_{PHDET}$/55 | $F_{PHDET}$/44 | $F_{PHDET}$/30 | MHz |
| Loop bandwidth (FRAC)[3] | $F_{BW}$ | $F_{PHDET}$/91 | $F_{PHDET}$/77 | $F_{PHDET}$/56 | MHz |
| Static phase offset of the PLL outputs[4] | $T_{SPO}$ | | | Max (±60 ps, ±0.5 degrees) | ps |
| | $T_{OUTJITTER}$ | | | | ps |
| PLL output duty cycle precision | $T_{OUTDUTY}$ | 48 | | 54 | % |
| PLL lock time[5] | $T_{LOCK}$ | | | Max (6.0 µs, 625 PFD cycles) | µs |
| PLL unlock time[6] | $T_{UNLOCK}$ | 2 | | 8 | PFD cycles |
| PLL output frequency | $F_{OUT}$ | 0.050 | | 1250 | MHz |
| Minimum reset pulse width | $T_{MRPW}$ | | | | µs |
| Maximum delay in the feedback path[7] | $F_{MAXDFB}$ | | | 1.5 | PFD cycles |
| Spread spectrum modulation spread[8] | Mod_Spread | 0.1 | | 3.1 | % |
| Spread spectrum modulation frequency[9] | Mod_Freq | $F_{PHDETF}$/(128x63) | 32 | $F_{PHDETF}$/(128) | KHz |

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/$F_{REF}$. For example, $F_{REF}$ = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

**Note**: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

### 7.2.3 DLL

The following table provides information about DLL.

**Table 38 • DLL Electrical Characteristics**

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input reference clock frequency | $F_{INF}$ | 133 | | 800 | MHz |
| Input feedback clock frequency | $F_{INFDBF}$ | 133 | | 800 | MHz |
| Primary output clock frequency | $F_{OUTPF}$ | 133 | | 800 | MHz |

| Parameter | Symbol | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Reference clock input rate[1, 2, 3] | $F_{XCVRREFCLKMAX\ CASCADE}$ | 20 | | 156 | 20 | | 156 | MHz |
| Reference clock rate at the PFD[4] | $F_{TXREFCLKPFD}$ | 20 | | 156 | 20 | | 156 | MHz |
| Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4] | $F_{TXREFCLKPFD10G}$ | 75 | | 156 | 75 | | 156 | MHz |
| Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5] | $F_{TXREFPN}$ | | | –110 | | | –110 | dBc /Hz |
| Phase noise at 10 KHz | $F_{TXREFPN}$ | | | –110 | | | –110 | dBc /Hz |
| Phase noise at 100 KHz | $F_{TXREFPN}$ | | | –115 | | | –115 | dBc /Hz |
| Phase noise at 1 MHz | $F_{TXREFPN}$ | | | –135 | | | –135 | dBc /Hz |
| Reference clock input rise time (10%–90%) | $T_{REFRISE}$ | | 200 | 500 | | 200 | 500 | ps |
| Reference clock input fall time (90%–10%) | $T_{REFFALL}$ | | 200 | 500 | | 200 | 500 | ps |
| Reference clock duty cycle | $T_{REFDUTY}$ | 40 | | 60 | 40 | | 60 | % |
| Spread spectrum modulation spread[6] | Mod_Spread | 0.1 | | 3.1 | 0.1 | | 3.1 | % |
| Spread spectrum modulation frequency[7] | Mod_Freq | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | KHz |

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

### 7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| UFS UPERM digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 33.2 | 34.9 | µs |
| | MPF300T, TL, TS, TLS | 33.2 | 34.9 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| Factory digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 493.6 | 510.1 | µs |
| | MPF300T, TL, TS, TLS | 493.6 | 510.1 | µs |
| | MPF500T, TL, TS, TLS | | | µs |

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

**Note:** These times do not include the power-up to functional timing overhead when using digest checks on power-up.

### 7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

**Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | | | ms | Zip flag set |
| Time to destroy the fabric data[1] | | | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | | | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | | | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | | | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | | | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | | | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | | | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1, 4] | | | s | Full scrubbing |
| Time to verify[5] | | | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

**Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | | | ms | Zip flag set |
| Time to destroy the fabric data[1] | | | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | | | ms | One iteration of scrubbing |

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | | | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | | | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | | | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | | | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1] | | | s | Full scrubbing |
| Time to verify[5] | | | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

## 7.6.7 Verify Time

The following tables describe verify time.

**Table 81 • Standalone Fabric Verify Times**

| Parameter | Devices | Max | Unit |
|---|---|---|---|
| Standalone verification over JTAG | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 53[1] | s |
| | MPF300T, TL, TS, TLS | 90[1] | s |
| | MPF500T, TL, TS, TLS | | s |
| Standalone verification over SPI | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 37[2] | s |
| | MPF300T, TL, TS, TLS | 55[2] | s |
| | MPF500T, TL, TS, TLS | | s |

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

**Notes:**

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

**Table 82 • Verify Time by Programming Hardware**

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF100T, TL, TS, TLS | | | | | | |
| MPF200T, TL, TS, TLS | 9 | 67 | 53 | | | s |
| MPF300T, TL, TS, TLS | 14 | 95 | 90 | | | s |

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF500T, TL, TS, TLS | | | | | | |

**Notes:**

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

**Table 83 • Verify System Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| In application verify by index | $T_{IAP\_Ver\_Index}$ | 44H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | | | s |
| In application verify by SPI address | $T_{IAP\_Ver\_Addr}$ | 45H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | | | s |

## 7.6.8 Authentication Time

The following tables describe authentication system service time.

**Table 84 • Authentication Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Bitstream Authentication | $T_{BIT\_AUTH}$ | 22H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | | | s |
| IAP Image Authentication | $T_{IAP\_AUTH}$ | 23H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | | | |

## 7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

**Table 85 • sNVM Read/Write Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Plain text programming | | 7.0 | 7.2 | 7.9 | ms | |
| Authenticated text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authenticated and encrypted text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authentication R/W 1st access from power-up overhead | $T_{PUF\_OVHD}$ | | 100 | 111 | ms | From $T_{FAB\_READY}$ |
| Plain text read | | 7.67 | 7.79 | 8.2 | µs | |

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Authenticated text read | | 113.25 | 114.02 | 118.5 | µs | |
| Authenticated and decrypted text read | | 159.59 | 160.53 | 166.5 | µs | |

**Notes:**

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- $T_{PUF\_OVHD}$ is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

### 7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

**Table 86 • sNVM Programming Cycles vs. Retention Characteristics**

| Programming Temperature | Programming Cycles per Page, Max | Programming Cycles per Block, Max | Retention Years |
|---|---|---|---|
| –40 °C to 100 °C | 10,000 | 100,000 | 20 |
| –40 °C to 85 °C | 10,000 | 100,000 | 20 |
| –40 °C to 55 °C | 10,000 | 100,000 | 20 |

**Note:** Page size = 128 bytes. Block size = 56 KBytes.

## 7.7 System Services

This section describes system switching and throughput characteristics.

### 7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

**Table 87 • System Services Throughput Characteristics**

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Serial number | $T_{Serial}$ | 00H | 65 | 67 | µs | |
| User code | $T_{User}$ | 01H | 0.8 | 1.05 | µs | |
| Design information | $T_{Design}$ | 02H | 2.4 | 2.7 | µs | |
| Device certificate | $T_{Cert}$ | 03H | 255 | 271 | ms | |
| Read digests | $T_{digest\_read}$ | 04H | 201 | 215 | µs | |
| Query security locks | $T_{sec\_Query}$ | 05H | 15 | 17 | µs | |
| Read debug information | $T_{Rd\_debug}$ | 06H | 34 | 38 | µs | |
| Reserved | | 07H–0FH | | | | |
| Secure NVM write plain text | $T_{SNVM\_Wr\_Plain}$ | 10H | | | | Note 1 |
| Secure NVM write authenticated plain text | $T_{SNVM\_Wr\_Auth}$ | 11H | | | | Note 1 |
| Secure NVM write authenticated cipher text | $T_{SNVM\_Wr\_Cipher}$ | 12H | | | | Note 1 |
| Reserved | | 13H–17H | | | | |

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Secure NVM read | $T_{SNVM\_Rd}$ | 18H | | | | Note 1 |
| Digital signature service raw | $T_{SIG\_RAW}$ | 19H | 174 | 187 | ms | |
| Digital signature service DER | $T_{SIG\_DER}$ | 1AH | 174 | 187 | ms | |
| Reserved | | 1BH–1FH | | | | |
| PUF emulation | $T_{Challenge}$ | 20H | 1.8 | 2.0 | ms | |
| Nonce service | $T_{Nonce}$ | 21H | 1.2 | 1.4 | ms | |
| Bitstream authentication | TBIT_AUTH | 22H | | | | Note 4 |
| IAP Image authentication | TIAP_AUTH | 23H | | | | Note 4 |
| Reserved | | 26H–3FH | | | | |
| In application programming by index | $T_{IAP\_Prg\_Index}$ | 42H | | | | Note 2 |
| In application programming by SPI address | $T_{IAP\_Prg\_Addr}$ | 43H | | | | Note 2 |
| In application verify by index | TIAP_Ver_Index | 44H | | | | Note 5 |
| In application verify by SPI address | TIAP_Ver_Addr | 45H | | | | Note 5 |
| Auto update | $T_{AutoUpdate}$ | 46H | | | | Note 2 |
| Digest check | $T_{digest\_chk}$ | 47H | | | | Note 3 |

1. See sNVM Read/Write Characteristics (see page 58).
2. See SPI Master Programming Time (see page 52).
3. See Digest Times (see page 54).
4. See Authentication Services Time (see page 58).
5. See Verify Services Time (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

## 7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

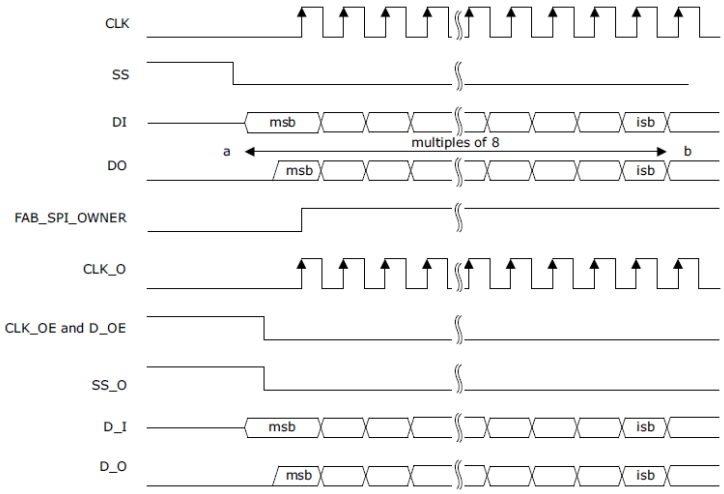
### 7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

**Table 88 • UJTAG Performance Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | | | 25 | MHz | |

**Figure 4 • USPI Switching Characteristics**




## 7.8.4 Tamper Detectors

The following section describes tamper detectors.

**Table 91 • ADC Conversion Rate**

| Parameter | Description | Min | Typ[1] | Max |
|---|---|---|---|---|
| $T_{CONV1}$ | Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0. | 420 µs | | 470 µs |
| $T_{CONVN}$ | Time between subsequent channel conversions. | | 480 µs | |
| $T_{SETUP}$ | Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs. | 0 ns | | |
| $T_{VALID}$[2] | Width of the valid pulse. | 1.625 µs | | 2 µs |
| $T_{RATE}$ | Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter. | 480 µs | Rate × 32 µs | 8128 µs |

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

**Note:** Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

**Table 92 • Temperature and Voltage Sensor Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Temperature sensing range | –40 | | 125 | °C | |
| Temperature sensing accuracy | –10 | | 10 | °C | |

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Time from negation of RESPONSE to all I/Os re-enabled | $T_{CLR\_IO\_DISABLE}$ | 28 | 38 | µs |
| Time from triggering the response to security locked | $T_{LOCKDOWN}$ | | | ns |
| Time from negation of RESPONSE to earlier security unlock condition | $T_{CLR\_LOCKDOWN}$ | | | ns |
| Time from triggering the response to device enters RESET | $T_{tr\_RESET}$ | 11.7 | 14 | µs |
| Time from triggering the response to start of zeroization | $T_{tr\_ZEROLISE}$ | 7.4 | 8.2 | ms |

### 7.8.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

**Table 95 • System Controller Suspend Entry and Exit Characteristics**

| Parameter | Symbol | Definition | Typ | Max | Unit |
|---|---|---|---|---|---|
| Time from TRSTb falling edge to SUSPEND_EN signal assertion | $T_{suspend\_Tr}$[1, 2] | Suspend entry time from TRST_N assertion | 42 | 44 | ns |
| Time from TRSTb rising edge to ACTIVE signal assertion | $T_{suspend\_exit}$ | Suspend exit time from TRST_N negation | 361 | 372 | ns |

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

### 7.8.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

**Table 96 • Dynamic Reconfiguration Interface Timing Characteristics**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| PCLK frequency | $F_{PD\_PCLK}$ | 200 | MHz |

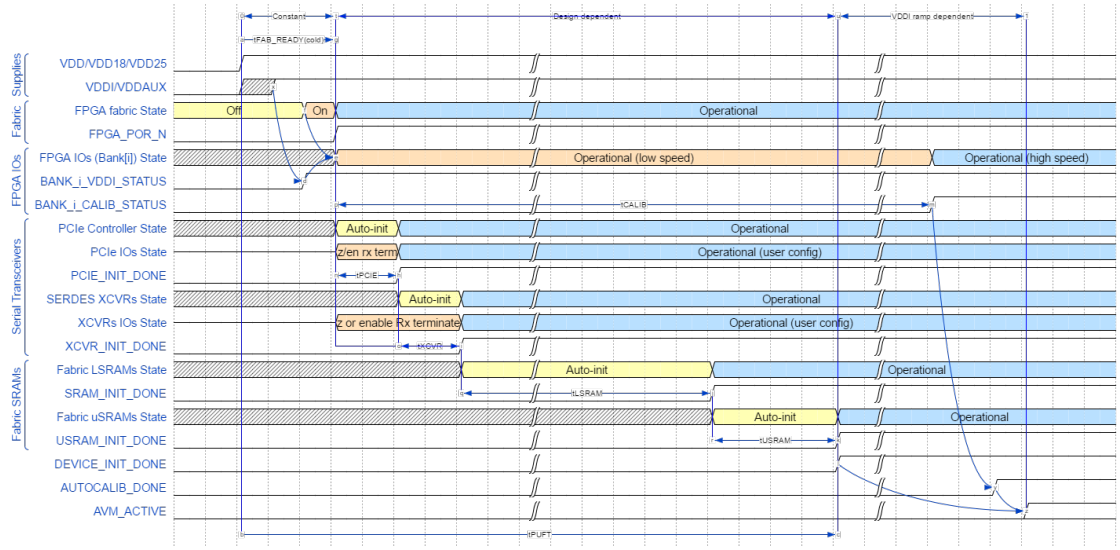
## 7.9 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

### 7.9.1 Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.

**Figure 5 • Cold Reset Timing**




**Notes:**

- The previous diagram showsthe case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
  - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
  - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
  - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

## 7.9.2 Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

## 7.11 User Crypto

The following section describes user crypto.

### 7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

**Table 112 • TeraFire F5200B Switching Characteristics**

| Parameter | Symbol | VDD = 1.0 V STD | VDD = 1.0 V – 1 | VDD = 1.05 V STD | VDD = 1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Operating frequency | $F_{MAX}$ | 189 | | 189 | | MHz | –40 °C to 100 °C |

### 7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

**Note:** Throughput cycle count collected with Athena TeraFire Core and RISCV running at 100 MHz.

**Table 113 • AES**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-ECB-128 encrypt[1] | 128 | 515 | 1095 |
| | 64K | 50157 | 933 |
| AES-ECB-128 decrypt[1] | 128 | 557 | 1760 |
| | 64K | 48385 | 1524 |
| AES-ECB-256 encrypt[1] | 128 | 531 | 1203 |
| | 64K | 58349 | 1203 |
| AES-ECB-256 decrypt[1] | 128 | 589 | 1676 |
| | 64K | 56673 | 1671 |
| AES-CBC-256 encrypt[1] | 128 | 576 | 1169 |
| | 64K | 52547 | 1169 |
| AES-CBC-256 decrypt[1] | 128 | 585 | 1744 |
| | 64K | 48565 | 1652 |
| AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1925 | 2740 |
| | 64K | 60070 | 2158 |
| AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1973 | 2268 |
| | 64K | 60102 | 2151 |

1. With DPA counter measures.

**Table 114 • GMAC**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-GCM-256[1], 128-bit tag, (message is only authenticated) | 128 | 1863 | 2211 |
| | 64K | 49707 | 2128 |

| | | | |
|---|---|---|---|
| SigVer, DSA-2048/SHA-256 | 1024 | 9810527 | 10884 |
| | 8K | 9597000 | 10719 |
| Key Agreement (KAS), DH-3072 (p=3072, security=256) | | 4920705 | 9338 |
| Key Agreement (KAS), DH-3072 (p=3072, security=256)[1] | | 78914533 | 9083 |

1. With DPA counter measures.

**Table 122 • NRBG**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string | | 18221 | 2841 |
| Reseed: no additional input, s=256 | | 13585 | 1180 |
| Reseed: 384-bit additional input, s=256 | | 15922 | 1342 |
| Generate: (no additional input), prediction resistance enabled, s= 256 | 128 | 15262 | 1755 |
| | 8K | 27169 | 8223 |
| Generate: (no additional input), prediction resistance disabled, s= 256 | 128 | 2138 | 1167 |
| | 8K | 14045 | 8223 |
| Generate: (384-bit additional input), prediction resistance enabled, s= 256 | 128 | 21299 | 1944 |
| | 8K | 33206 | 8949 |
| Generate: (384-bit additional input), prediction resistance disabled, s= 256 | 128 | 11657 | 1894 |
| | 8K | 23564 | 8950 |
| Un-instantiate | | 761 | 666 |

1. With DPA counter measures.