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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-LFBGA, FC
Supplier Device Package	325-FCBGA (11x14.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200tl-fcsg325i

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see System Services (see page 59).
- The Non-Volatile Characteristics section was updated. For more information, see Non-Volatile Characteristics (see page 51).
- The Fabric Macros section was updated. For more information, see Fabric Macros (see page 60).
- The Transceiver Switching Characteristics section was updated. For more information, see Transceiver Switching Characteristics (see page 42).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed and HSIO Maximum Output Buffer Speed.
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications.
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics.
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
PCI	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45
LVTTL	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89
LVCMOS15	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575
LVCMOS12	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26
SSTL25I[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL25II[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL18I[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL18II[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
HCSL25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18[5]	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V_{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V_{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} – 0.4 V;
   b. $V_{ICM} + V_{ID}/2$ must be $< V_{DDI} + 0.4$ V;
   c. $V_{ICM} - V_{ID}/2$ must be $>$VSS – 0.3 V;
   d. Any differential input with $V_{ICM} \leq 0.6$ V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15[3]	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25[3]	GPIO		1.25		0.24	0.262	0.272

Min (%)	Typ	Max (%)	Unit	Condition
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 80% of V_{DDI}.

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	20	Ω	V_{ICM} < 0.8 V
		–20	100	40	Ω	0.6 V < V_{ICM} < 1.65 V
		–20	100	80	Ω	1.4 V < V_{ICM}
Single-ended thevenin termination[2, 3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to V_{SS}[4, 5]	Internal parallel termination to V_{SS}	–20	120	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V
		–20	240	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of V_{DDI}.
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL18I	SSTL 1.8 V Class I	50	0	V_{REF}	0.9
SSTL18II	SSTL 1.8 V Class II	50	0	V_{REF}	0.9
SSTL15I	SSTL 1.5 V Class I	50	0	V_{REF}	0.75
SSTL15II	SSTL 1.5 V Class II	50	0	V_{REF}	0.75
SSTL135I	SSTL 1.35 V Class I	50	0	V_{REF}	0.675
SSTL135II	SSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL15I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	V_{REF}	0.75
HSTL15II	HSTL 1.5 V Class II	50	0	V_{REF}	0.75
HSTL135I	HSTL 1.35 V Class I	50	0	V_{REF}	0.675
HSTL135II	HSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL12	HSTL 1.2 V	50	0	V_{REF}	0.6
HSUL18I	High-speed unterminated logic 1.8 V Class I	50	0	V_{REF}	0.9
HSUL18II	HSUL 1.8 V Class II	50	0	V_{REF}	0.9
HSUL12	HSUL 1.2 V	50	0	V_{REF}	0.6
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	V_{REF}	0.84
POD12II	POD 1.2 V Class II	50	0	V_{REF}	0.84
LVDS33	LVDS 3.3 V	100	0	0[1]	0
LVDS25	LVDS 2.5 V	100	0	0[1]	0
LVDS18	LVDS 1.8 V	100	0	0[1]	0
RSDS33	Reduced swing differential signaling 3.3 V	100	0	0[1]	0
RSDS25	RSDS 2.5 V	100	0	0[1]	0
RSDS18	RSDS 1.8 V	100	0	0[1]	0
MINILVDS33	Mini-LVDS 3.3 V	100	0	0[1]	0
MINILVDS25	Mini-LVDS 2.5 V	100	0	0[1]	0
SUBLVDS33	Sub-LVDS 3.3 V	100	0	0[1]	0
SUBLVDS25	Sub-LVDS 2.5 V	100	0	0[1]	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	0[1]	0
PPDS25	PPDS 2.5 V	100	0	0[1]	0
BUSLVDSE25	Bus LVDS	100	0	0[1]	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	0[1]	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	0[1]	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	0[1]	0

1. The value given is the differential output voltage.

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

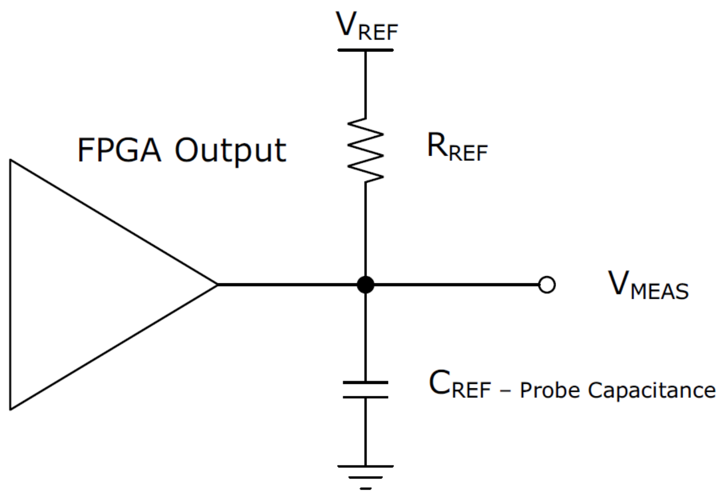
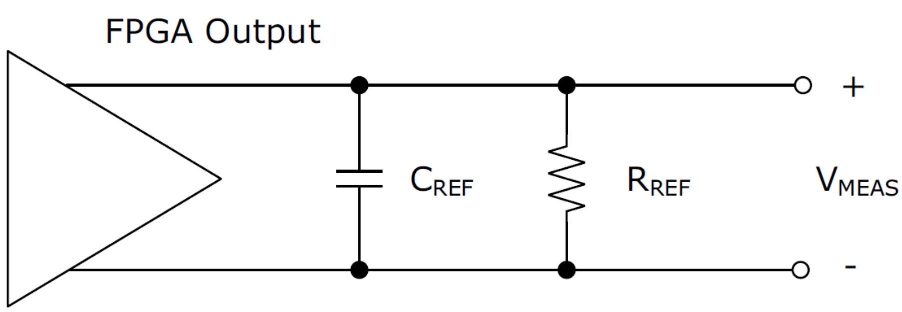


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
FMAX	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
FMAX	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
FMAX	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
FMAX	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
FMAX	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
FMAX	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
FMAX 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks)[2]	FMAXINJ		120	1000	ps
PLL VCO frequency	FVCO	800		5000	MHz
Loop bandwidth (Int)[3]	FBW	FPHDET/55	FPHDET/44	FPHDET/30	MHz
Loop bandwidth (FRAC)[3]	FBW	FPHDET/91	FPHDET/77	FPHDET/56	MHz
Static phase offset of the PLL outputs[4]	TSPO			Max (±60 ps, ±0.5 degrees)	ps
	TOUTJITTER				ps
PLL output duty cycle precision	TOUTDUTY	48		54	%
PLL lock time[5]	TLOCK			Max (6.0 µs, 625 PFD cycles)	µs
PLL unlock time[6]	TUNLOCK	2		8	PFD cycles
PLL output frequency	FOUT	0.050		1250	MHz
Minimum reset pulse width	TMRPW				µs
Maximum delay in the feedback path[7]	FMAXDFB			1.5	PFD cycles
Spread spectrum modulation spread[8]	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency[9]	Mod_Freq	FPHDETF/(128x63)	32	FPHDETF/(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/FREF. For example, FREF = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3 DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter[1]	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	FINF	133		800	MHz
Input feedback clock frequency	FINFDBF	133		800	MHz
Primary output clock frequency	FOUTPF	133		800	MHz

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2, 3]	$F_{XCVRREFCLKMAX CASCADE}$	20		156	20		156	MHz
Reference clock rate at the PFD[4]	$F_{TXREFCLKPFD}$	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4]	$F_{TXREFCLKPFD10G}$	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5]	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 10 KHz	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 100 KHz	$F_{TXREFPN}$			–115			–115	dBc /Hz
Phase noise at 1 MHz	$F_{TXREFPN}$			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	$T_{REFRISE}$		200	500		200	500	ps
Reference clock input fall time (90%–10%)	$T_{REFFALL}$		200	500		200	500	ps
Reference clock duty cycle	$T_{REFDUTY}$	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T_J	Programming Cycles, Max	Retention Years	Retention Years at T_J
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41[1]		s
		MPF300T, TL, TS, TLS	50[1]	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS[1]		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data PNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 79 • Zeroization Times for MPF300T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non- recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 80 • Zeroization Times for MPF500T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	µs	
Authenticated and decrypted text read		159.59	160.53	166.5	µs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	µs	
User code	T_{User}	01H	0.8	1.05	µs	
Design information	T_{Design}	02H	2.4	2.7	µs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	µs	
Query security locks	T_{sec_Query}	05H	15	17	µs	
Read debug information	T_{Rd_debug}	06H	34	38	µs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM\_Wr\_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM\_Wr\_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM\_Wr\_Cipher}$	12H				Note 1
Reserved		13H–17H				

7.9.4 Design Dependence of T PUFT and T WRFT

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note T_{PCIE}, T_{XCVR}, T_{LSRAM}, and T_{USRAM} can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$T_{PUFT} = T_{FAB\_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

$T_{WRFT} = T_{FAB\_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

Note: T_{PCIE}, T_{XCVR}, T_{LSRAM}, T_{USRAM}, and T_{CALIB} are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond T_{PUFT} (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

7.9.5 Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 99 • Cold Boot

Power-On (Cold) Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when weak pull-ups are enabled – $T_{PU\_PD\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when fabric is operational – $T_{FAB\_READY(cold)}$	1.20	4.54	7.87	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(cold)}$	1.22	4.56	7.89	ms

7.9.6 Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 100 • Warm Boot

Warm Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when weak pull-ups/pull-downs are enabled – $T_{PU\_PD\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when fabric is operational – $T_{FAB\_READY(warm)}$	0.94	1.79	2.65	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(warm)}$	0.96	1.81	2.67	ms

7.9.7 Miscellaneous Initialization Parameters

In the following table, T_{FAB_READY} refers to either $T_{FAB\_READY(cold)}$ or $T_{FAB\_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T_{FAB_READY} to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T_{FAB_READY} to auto-update start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to programming recovery start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to the tamper flags being available	T_{TAMPER_READY}	0	0	0	ms	
The time from T_{FAB_READY} to the Athena Crypto co-processor being available (for S devices only)	T_{CRYPTO_READY}	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to T_{PUF_OVHD} at section Secure NVM Performance (see page 58).

7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in I/O-Related Supplies (see page 66).

Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

Note: In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash*Freeze Mode and to exit Flash*Freeze mode.