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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	170
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	325-LFBGA, FC
Supplier Device Package	325-FCBGA (11x14.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200tls-fcsg325i

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Preliminary
MPF200T, TL, TS, TLS	Preliminary
MPF300T, TL, TS, TLS	Preliminary
MPF500T, TL, TS, TLS	Preliminary

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at $T_J = 100^\circ\text{C}$	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

Note: Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot Duration as % at $T_J = 100^\circ\text{C}$	Condition (V)
100	-0.05
100	-0.1
100	-0.15
100	-0.2
100	-0.25
100	-0.3
100	-0.35
100	-0.4
44	-0.45
14	-0.5
4.8	-0.55
1.6	-0.6

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

Table 13 • DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
PCI ¹	3.15	3.3	3.45		0.1 x V _{DDI}	0.9 x V _{DDI}		1.5	0.5
LVTTL	3.15	3.3	3.45		0.4	2.4			
LVC MOS33	3.15	3.3	3.45		0.4	V _{DDI} – 0.4			
LVC MOS25	2.375	2.5	2.625		0.4	V _{DDI} – 0.4			
LVC MOS18	1.71	1.8	1.89		0.45	V _{DDI} – 0.45			
LVC MOS15	1.425	1.5	1.575		0.25 x V _{DDI}	0.75 x V _{DDI}			
LVC MOS12	1.14	1.2	1.26		0.25 x V _{DDI}	0.75 x V _{DDI}			
SSTL25I ³	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608		8.1	8.1
SSTL25II ³	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810		16.2	16.2
SSTL18I ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		6.7	6.7
SSTL18II ³	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603		13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4		16	16

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
HCSL25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18 ⁵	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V _{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V _{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} – 0.4 V;
 - b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
 - c. V_{ICM} – V_{ID}/2 must be >V_{SS} – 0.3 V;
 - d. Any differential input with V_{ICM} ≤ 0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. V_{DDI} = 1.8 V, V_{DDAUX} = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15 ³	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25 ³	GPIO		1.25		0.24	0.262	0.272

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to $V_{SS}^{4,5}$	Internal	-20	120	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$
	parallel termination to V_{SS}	-20	240	20	Ω	$V_{DDI} = 2.5\text{ V}/1.8\text{ V}/1.5\text{ V}/1.2\text{ V}$

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI} .
3. For 50 Ω /75 Ω /150 Ω cases, nearest supported values of 40 Ω /60 Ω /120 Ω are used.
4. Measured at 50% of V_{DDI} .
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSUL18I	HSUL 1.8 V Class I	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	$V_{REF} -$ 0.54	$V_{REF} +$ 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	$V_{REF} -$.22	$V_{REF} +$.22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	$V_{REF} -$.15	$V_{REF} +$.15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.800	0		V
SLVS33	Scalable low- voltage signaling 3.3 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
SLVS25	SLVS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
BLVDSE25 ⁶	Bus LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
MLVDSE25 ⁶	Multipoint LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
LVPECL33 ⁶	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.675	0		V

Standard	STD	–1	Unit
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps
LVC MOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with $V_{ID} \geq 200$ mV.

7.1.4 Output Buffer Speed

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3 ¹	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3 ¹	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3 ¹	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2 ¹	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2 ¹	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2 ¹	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2 ¹	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2 ¹	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T _{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F _{MAX}	F _{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew ¹	F _{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F _{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F _{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F _{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion ²	T _{DCB}	90	90	90	90	ps	HSIO without bridging
	T _{DCB}	115	115	115	115	ps	HSIO with bridging
	T _{DCB}	90	90	90	90	ps	GPIO without bridging
	T _{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2

PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F _{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F _{INF}	10		1250	MHz
Minimum reference or feedback pulse width ¹	F _{INPULSE}	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F _{PHDET1}	1		312	MHz
Frequency at the PFD (fractional mode)	F _{PHDET2}	10	50	125	MHz
Allowable input duty cycle	F _{INDUTY}	25		75	%

Parameter ¹	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency ²	F _{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F _{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	T _{OUTJITTERP}			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T _{SKEW}			±200	ps
DLL lock time	T _{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T _{MRPW}	3			ns
Minimum input pulse width ³	T _{MIPW}	20			ns
Minimum input clock pulse width high	T _{MPWH}	400			ps
Minimum input clock pulse width low	T _{MPWL}	400			ps
Delay step size	T _{DEL}	12.7	30	35	ps
Maximum delay block delay ⁴	T _{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input) ⁵	T _{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode) ⁵	T _{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4

RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{2FREQ}		2		MHz
Accuracy	RC _{2FACC}	−4		4	%
Duty cycle	RC _{2DC}	46		54	%
Peak-to-peak output period jitter	RC _{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC _{2CIIT}		5	10	ns
Operating current (V _{DD25})	RC _{2IVPPA}			60	μA
Operating current (V _{DD})	RC _{2IVDD}			2.6	μA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{SCFREQ}		160		MHz
Accuracy	RC _{SCFACC}	−4		4	%
Duty cycle	RC _{SCDC}	47		52	%
Peak-to-peak output period jitter	RC _{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC _{SCCIIT}			172	ps
Operating current (V _{DD25})	RC _{SCVPPA}			599	μA

7.5.7 CPRI

The following table describes CPRI.

Table 66 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5.8 JESD204B

The following table describes JESD204B.

Table 67 • JESD204B

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps		0.35	UI
	6.25 Gbps		0.3	UI
	12.5 Gbps ¹			UI
Receive jitter tolerance	3.125 Gbps	0.56		UI
	6.25 Gbps	0.6		UI
	12.5 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable) ^{1, 4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1, 2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1, 3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ¹			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53 ¹	s
	MPF300T, TL, TS, TLS	90 ¹	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37 ²	s
	MPF300T, TL, TS, TLS	55 ²	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

Notes:

- Standalone verify is limited to 2,000 total device hours over the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T _{SNVM_Rd}	18H				Note 1
Digital signature service raw	T _{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T _{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	T _{Challenge}	20H	1.8	2.0	ms	
Nonce service	T _{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	T _{BIT_AUTH}	22H				Note 4
IAP Image authentication	T _{IAP_AUTH}	23H				Note 4
Reserved		26H–3FH				
In application programming by index	T _{IAP_Prg_Index}	42H				Note 2
In application programming by SPI address	T _{IAP_Prg_Addr}	43H				Note 2
In application verify by index	T _{IAP_Ver_Index}	44H				Note 5
In application verify by SPI address	T _{IAP_Ver_Addr}	45H				Note 5
Auto update	T _{AutoUpdate}	46H				Note 2
Digest check	T _{digest_chk}	47H				Note 3

1. See [sNVM Read/Write Characteristics](#) (see page 58).
2. See [SPI Master Programming Time](#) (see page 52).
3. See [Digest Times](#) (see page 54).
4. See [Authentication Services Time](#) (see page 58).
5. See [Verify Services Time](#) (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

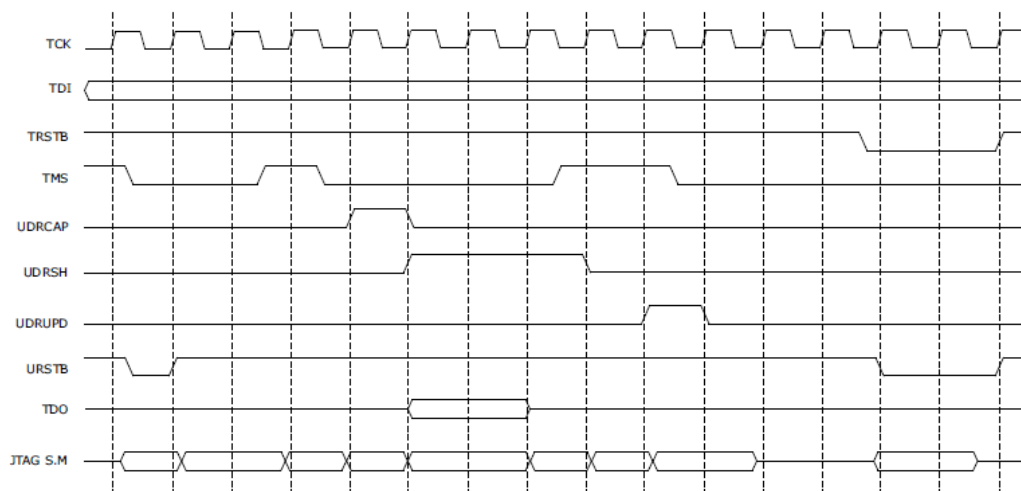
This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}			25	MHz	

Figure 3 • UJTAG Timing Diagram

7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 89 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}				MHz	

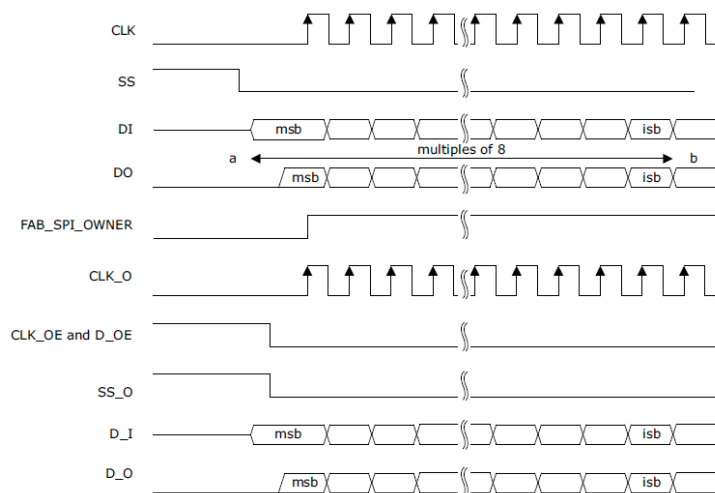
7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

Table 90 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V _{DDI} = 3.3 V Max	V _{DDI} = 2.5 V Max	V _{DDI} = 1.8 V Max	V _{DDI} = 1.5 V Max	V _{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins ¹	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Figure 4 • USPI Switching Characteristics

7.8.4

Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	