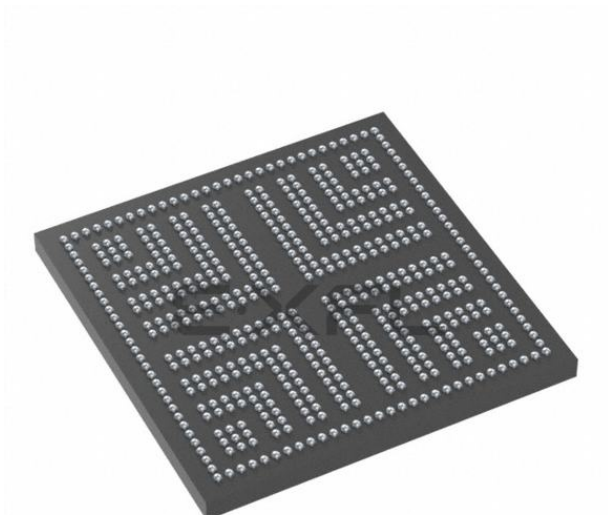




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	192000
Total RAM Bits	13619200
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf200ts-1fcsg536i

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3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Preliminary
MPF200T, TL, TS, TLS	Preliminary
MPF300T, TL, TS, TLS	Preliminary
MPF500T, TL, TS, TLS	Preliminary

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	−0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	−0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	−0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	−0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	−0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	−0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	−0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	−0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	−0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	−0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	−0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	−0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	−0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	−0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	−0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	−65	150	°C
Junction temperature ¹	T _J	−55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at $T_J = 100^\circ\text{C}$	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

Note: Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot Duration as % at $T_J = 100^\circ\text{C}$	Condition (V)
100	-0.05
100	-0.1
100	-0.15
100	-0.2
100	-0.25
100	-0.3
100	-0.35
100	-0.4
44	-0.45
14	-0.5
4.8	-0.55
1.6	-0.6

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18 ⁵	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18 ⁵	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18 ⁵	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

Standard	STD	–1	Unit
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps
LVC MOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with $V_{ID} \geq 200$ mV.

7.1.4 Output Buffer Speed

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVC MOS18 (12 mA)	500	500	Mbps
LVC MOS15 (10 mA)	500	500	Mbps

Table 44 • μ SRAM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	T_{ac}		2		2	ns	Read-port

Table 45 • μ PROM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit
Read access time	T_{ac}	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Tx data rate ^{1,2}	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled ²	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency ³	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode ²	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode ²	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Reference clock input rate ^{1,2}	$F_{TXREFCLK}$	20		800	20		800	MHz

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, see table Differential DC Input and Output Levels .
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVC MOS25	For DC input levels, see table DC Input and Output Levels .

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115 ¹		Ω
Power-up termination			>50K		Ω

1. Measured at V_{CM} = 1.2 V and V_{ID} = 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver TX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver RX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (-STD) / 4.25 Gbps (-1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (-STD) / 5.32 Gbps (-1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (-STD) / 8.5 Gbps (-1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (-STD) / 10.6 Gbps (-1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (-STD) / 4.25 Gbps (-1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (-STD) / 5.32 Gbps (-1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (-STD) / 8.5 Gbps (-1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (-STD) / 10.6 Gbps (-1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see [UG0677: PolarFire FPGA Transceiver User Guide](#).

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{TERM}		85		Ω	
	V_{TERM}		100		Ω	
	V_{TERM}		150		Ω	
Common mode voltage ¹	V_{OCM}	$0.44 \times V_{\text{DDA}}$	$0.525 \times V_{\text{DDA}}$	$0.59 \times V_{\text{DDA}}$	V	DC coupled 50% setting
	V_{OCM}	$0.52 \times V_{\text{DDA}}$	$0.6 \times V_{\text{DDA}}$	$0.66 \times V_{\text{DDA}}$	V	DC coupled 60% setting
	V_{OCM}	$0.61 \times V_{\text{DDA}}$	$0.7 \times V_{\text{DDA}}$	$0.75 \times V_{\text{DDA}}$	V	DC coupled 70% setting
	V_{OCM}	$0.63 \times V_{\text{DDA}}$	$0.8 \times V_{\text{DDA}}$	$0.83 \times V_{\text{DDA}}$	V	DC coupled 80% setting
Rise time ²	T_{TXRF}	41		70	ps	20% to 80%
Fall time ²		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew ³	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew ⁴	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time ⁷	$T_{\text{TxElTrEntry}}$				ns	
Electrical idle transition exit time ⁷	$T_{\text{TxElTrExit}}$				ns	
Electrical idle amplitude	V_{TxElpp}				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time ⁸	T_{DPLLlock}				REFCLK UIs	
Total jitter ^{5,6}	T_{J}				UI	Data rate ≥ 8.5 Gbps to 12.7 Gbps ⁹
Deterministic jitter ^{5,6}	T_{DJ}				UI	(Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter ^{5,6}	T_{J}			0.28	UI	Data rate ≥ 3.2 Gbps to 8.5 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.28	UI	Data rate ≥ 1.6 Gbps to 3.2 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.13	UI	Data rate ≥ 800 Mbps to 1.6 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.02	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.06	UI	Data rate = 250 Mbps to 800 Mbps
Deterministic jitter ^{5,6}	T_{DJ}			0.01	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps ¹			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps ¹			UI

- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

7.5.7 CPRI

The following table describes CPRI.

Table 66 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5.8 JESD204B

The following table describes JESD204B.

Table 67 • JESD204B

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps		0.35	UI
	6.25 Gbps		0.3	UI
	12.5 Gbps ¹			UI
Receive jitter tolerance	3.125 Gbps	0.56		UI
	6.25 Gbps	0.6		UI
	12.5 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T _{SNVM_Rd}	18H				Note 1
Digital signature service raw	T _{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T _{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	T _{Challenge}	20H	1.8	2.0	ms	
Nonce service	T _{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	T _{BIT_AUTH}	22H				Note 4
IAP Image authentication	T _{IAP_AUTH}	23H				Note 4
Reserved		26H–3FH				
In application programming by index	T _{IAP_Prg_Index}	42H				Note 2
In application programming by SPI address	T _{IAP_Prg_Addr}	43H				Note 2
In application verify by index	T _{IAP_Ver_Index}	44H				Note 5
In application verify by SPI address	T _{IAP_Ver_Addr}	45H				Note 5
Auto update	T _{AutoUpdate}	46H				Note 2
Digest check	T _{digest_chk}	47H				Note 3

1. See [sNVM Read/Write Characteristics](#) (see page 58).
2. See [SPI Master Programming Time](#) (see page 52).
3. See [Digest Times](#) (see page 54).
4. See [Authentication Services Time](#) (see page 58).
5. See [Verify Services Time](#) (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

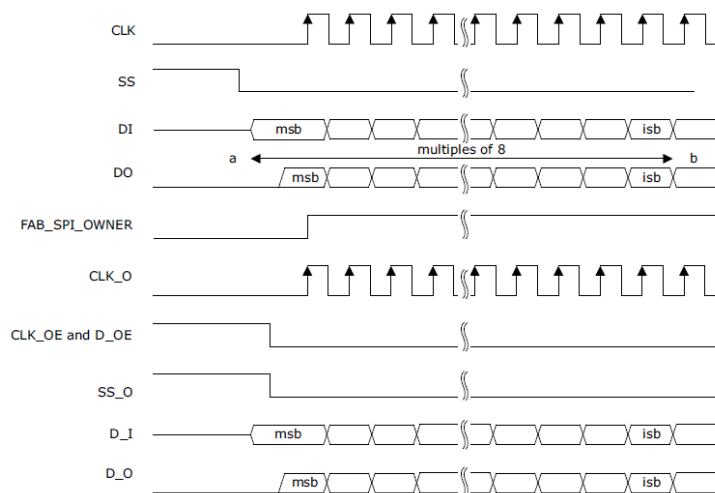
This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}			25	MHz	

Figure 4 • USPI Switching Characteristics

7.8.4

Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T _{JTAG_ACTIVE} ^{1, 2}	45	52	ns
	T _{MESH_ERR} ²	1.8	2.2	μs
	T _{CLK_GLITCH} ^{1, 2}			ns
	T _{CLK_FREQ} ^{1, 2}			μs
	T _{LOW_1P05} ²	70	108	μs
	T _{HIGH_1P8} ²	85	120	μs
	T _{HIGH_2P5} ²	130	520	μs
	T _{GLITCH_1P05} ²			μs
	T _{SECDEC} ^{1, 2}			μs
	T _{DRI_ERR} ²	14	18	μs
	T _{WDOG} ^{1, 2}			μs
	T _{LOCK_ERR} ²			μs
Time from system controller instruction execution to flag generation	T _{INST_BUF_ACCESS} ^{2, 3}	4	5	μs
	T _{INST_DEBUG} ^{2, 3}	3.3	4	μs
	T _{INST_CHK_DIGEST} ^{2, 3}	1.8	3	μs
	T _{INST_EC_SETUP} ^{2, 3}	1.8	2	μs
	T _{INST_FACT_PRIV} ^{2, 3}	3.8	5	μs
	T _{INST_KEY_VAL} ^{2, 3}	2.5	3.1	μs
	T _{INST_MISC} ^{2, 3}	1.5	2	μs
	T _{INST_PASSCODE_MATCH} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_SETUP} ^{2, 3}	4.2	5	μs
	T _{INST_PROG} ^{2, 3}	3.8	4.1	μs
	T _{INST_PUB_INFO} ^{2, 3}	4	4.5	μs
	T _{INST_ZERO_RECO} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_FAIL} ^{2, 3}	170	180	μs
	T _{INST_KEY_VAL_FAIL} ^{2, 3}	92	110	μs
	T _{INST_UNUSED} ^{2, 3}	4	5	μs
Time from sending the CLEAR to deassertion on FLAG	T _{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	T _{IO_DISABLE}	40	50	ns

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T _{FF_ENTRY}		59		μs	
The time from Flash*Freeze exit pin assertion to fabric operational state	T _{FF_FABRIC_UP}		133		μs	
The time from Flash*Freeze exit pin assertion to I/Os operational	T _{FF_IO_ACTIVE}		143		μs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T _{DISU}	TDI input setup time	0.0			ns	
T _{DIHD}	TDI input hold time	2.0			ns	
T _{TMSSU}	TMS input setup time	1.5			ns	
T _{TMSHD}	TMS input hold time	1.5			ns	
F _{TCK}	TCK frequency			25	MHz	
T _{TCKDC}	TCK duty cycle	40		60	%	
T _{TDOCQ}	TDO clock to Q out			8.4	ns	C _{LOAD} = 40 pf
T _{TRSTBCQ}	TRSTB clock to Q out			23.5	ns	C _{LOAD} = 40 pf
T _{TRSTBPW}	TRSTB min pulse width	50			ns	
T _{TRSTBREM}	TRSTB removal time	0.0			ns	
T _{TRSTBREC}	TRSTB recovery time	12.0			ns	
C _{INTDI}	TDI input pin capacitance			5.3	pf	
C _{INTMS}	TMS input pin capacitance			5.3	pf	
C _{INTCK}	TCK input pin capacitance			5.3	pf	
C _{INTTRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			20	MHz	

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 ¹ , 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384 ¹ , 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256 ¹ (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 ¹	512	2386	1579
	64K	77576	990
SHA-256 ¹	512	2516	884
	64K	84752	938
SHA-384 ¹	1024	4154	884
	64K	100222	938
SHA-512 ¹	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384 ¹	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155

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