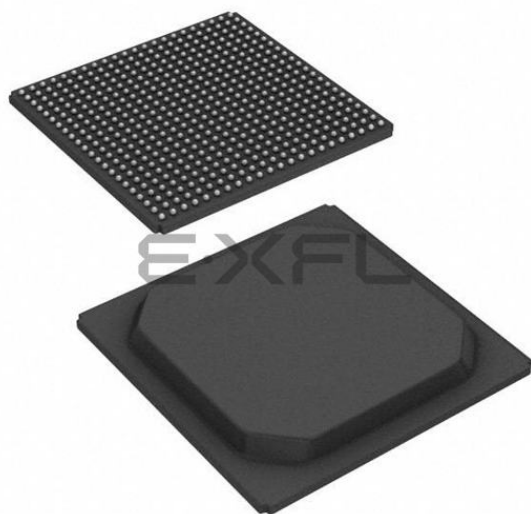




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-1fcg484e

2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V _{IN}) Overshoot Duration as % at T _J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V _{IN}) Undershoot Duration as % at T _J = 100 °C	Condition (V)
100	-0.5
100	-0.55
100	-0.6
100	-0.65
100	-0.7
100	-0.75
100	-0.8
100	-0.85
100	-0.9
100	-0.95
100	-1
100	-1.05
100	-1.1
100	-1.15
100	-1.2
69	-1.25
45	-1.3

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

I/O Standard	Bank Type	V _{OCM} ¹ Min (V)	V _{OCM} Typ (V)	V _{OCM} Max (V)	V _{OD} ² Min (V)	V _{OD} ² Typ (V)	V _{OD} ² Max (V)
MLVDSSE25 ³	GPIO		1.25		0.396	0.442	0.453
LVPECL33 ³	GPIO		1.65		0.664	0.722	0.755
MIPIE25 ³	GPIO		0.25		0.1	0.22	0.3

1. V_{OCM} is the output common mode voltage.
2. V_{OD} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
 - a. V_{ICM} must be less than V_{DDI} - 0.4V;
 - b. V_{ICM} + V_{ID}/2 must be < V_{DDI} + 0.4 V;
 - c. V_{ICM} - V_{ID}/2 must be > V_{SS} - 0.3 V.

Table 17 • Complementary Differential DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} ^{1,3} Min (V)	I _{OL} ² Min (mA)	I _{OH} ² Min (mA)
SSTL25I	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608	8.1	8.1
SSTL25II	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810	16.2	16.2
SSTL18I	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	6.7	6.7
SSTL18II	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	16	16
HSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSTL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSUL18I ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /55	(V _{DDI} – V _{OH})/55
HSUL18II ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSUL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
POD12I ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /48	(V _{DDI} – V _{OH})/48
POD12II ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34

1. V_{OH} is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers
3. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).

6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

Min (%)	Typ	Max (%)	Unit	Condition
–40	50	20	Ω	V _{DDI} = 1.8 V/1.5 V/1.35 V/1.2 V
–40	75	20	Ω	V _{DDI} = 1.8 V
–40	150	20	Ω	V _{DDI} = 1.8 V
–20	20	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	30	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	40	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	120	20	Ω	V _{DDI} = 1.5 V/1.35 V

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
SLVS25	SLVS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.350	0		V
BLVDSE25 ⁶	Bus LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
MLVDSE25 ⁶	Multipoint LVDS 2.5 V	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
LVPECL33 ⁶	Low-voltage positive emitter coupled logic	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	$V_{ICM} - .125$	$V_{ICM} + .125$	0.250	0.675	0		V

Standard	Description	V_L^1	V_H^1	V_{ID}^2	V_{ICM}^2	$V_{MEAS}^{3,4}$	$V_{REF}^{1,5}$	Unit
HSTL135II	Differential HSTL 1.35 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	$V_{ICM} -$.125	$V_{ICM} +$.125	0.250	0.200	0		V

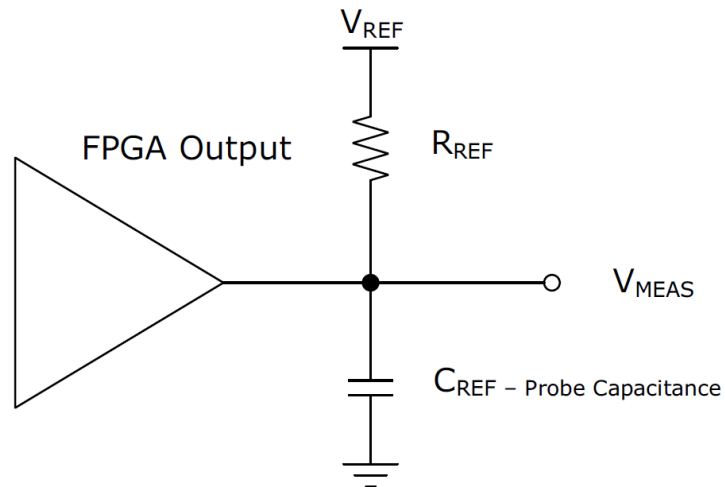
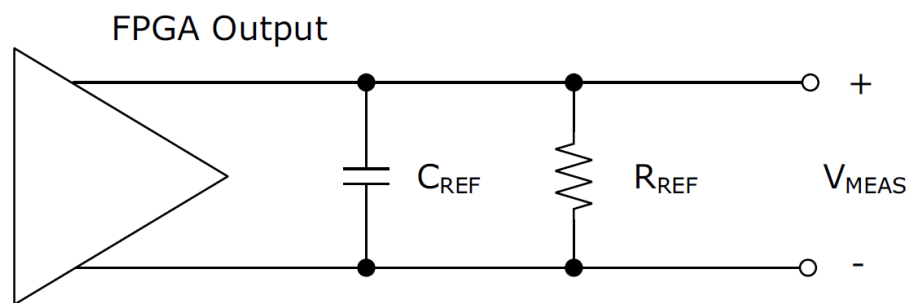
1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H . All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in [Output Delay Measurement—Single-Ended Test Setup](#) (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCI 3.3 V	25	10	1.65	
LVTTTL33	LVTTTL 3.3 V	1M	0	1.65	
LVC MOS33	LVC MOS 3.3 V	1M	0	1.65	
LVC MOS25	LVC MOS 2.5 V	1M	0	1.25	
LVC MOS18	LVC MOS 1.8 V	1M	0	0.90	
LVC MOS15	LVC MOS 1.5 V	1M	0	0.75	
LVC MOS12	LVC MOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

Figure 2 • Output Delay Measurement—Differential Test Setup


7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T _{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F _{MAX}	F _{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew ¹	F _{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F _{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F _{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F _{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion ²	T _{DCB}	90	90	90	90	ps	HSIO without bridging
	T _{DCB}	115	115	115	115	ps	HSIO with bridging
	T _{DCB}	90	90	90	90	ps	GPIO without bridging
	T _{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2

PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F _{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F _{INF}	10		1250	MHz
Minimum reference or feedback pulse width ¹	F _{INPULSE}	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F _{PHDET1}	1		312	MHz
Frequency at the PFD (fractional mode)	F _{PHDET2}	10	50	125	MHz
Allowable input duty cycle	F _{INDUTY}	25		75	%

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver RX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (-STD) / 4.25 Gbps (-1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (-STD) / 5.32 Gbps (-1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (-STD) / 8.5 Gbps (-1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (-STD) / 10.6 Gbps (-1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (-STD) / 4.25 Gbps (-1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (-STD) / 5.32 Gbps (-1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (-STD) / 8.5 Gbps (-1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (-STD) / 10.6 Gbps (-1) ¹		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (-STD) / 12.7 Gbps (-1) ¹		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see [UG0677: PolarFire FPGA Transceiver User Guide](#).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps ⁵
		0.41			UI	>1.6 to 3.2 Gbps ⁵
		0.41			UI	>0.8 to 1.6 Gbps ⁵
		0.41			UI	250 to 800 Mbps ⁵
Total jitter tolerance with stressed eye	T _{TJOLSE}	0.65			UI	3.125 Gbps ⁵
		0.65			UI	6.25 Gbps ⁶
		0.7			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
Sinusoidal jitter tolerance with stressed eye	T _{SJTOLSE}	0.1			UI	3.125 Gbps ⁵
		0.05			UI	6.25 Gbps ⁶
		0.05			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

- Valid at 3.2 Gbps and below.
- Data vs. Rx reference clock frequency.
- Achieves compliance with PCIe electrical idle detection.
- Achieves compliance with SATA OOB specification.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T _J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is $20 \times LF = 20 \times .8 = 16$ years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is $10 \times LF$ or 10 years over the industrial temperature range.

7.6.5**Digest Time**

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		μs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	35	μs
	MPF300T, TL, TS, TLS	33.2	35	μs
	MPF500T, TL, TS, TLS			μs
sNVM digest run time ¹	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	46.6	48.8	μs
	MPF300T, TL, TS, TLS	46.6	48.8	μs
	MPF500T, TL, TS, TLS			μs
User key digest run time ²	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	525.4	543.3	μs
	MPF300T, TL, TS, TLS	525.4	543.3	μs
	MPF500T, TL, TS, TLS			μs

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

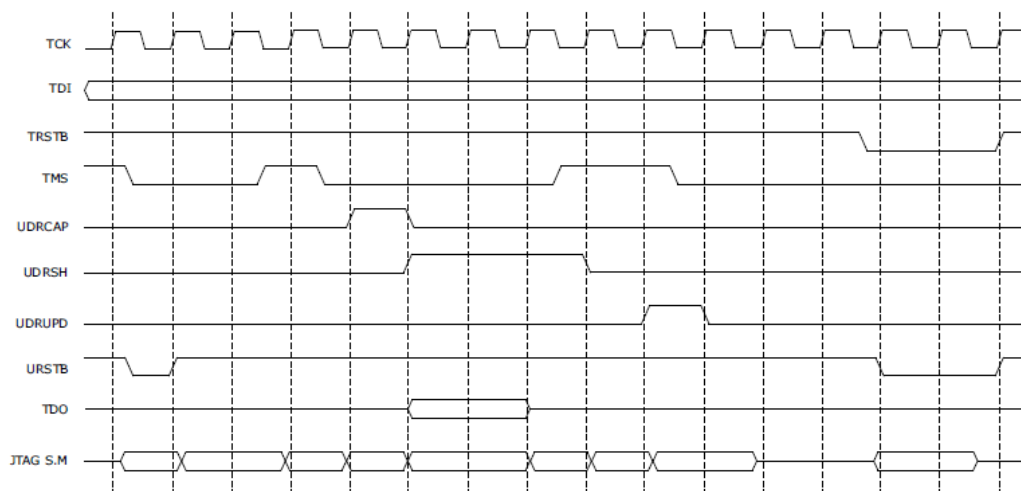
Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

Figure 3 • UJTAG Timing Diagram

7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 89 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}				MHz	

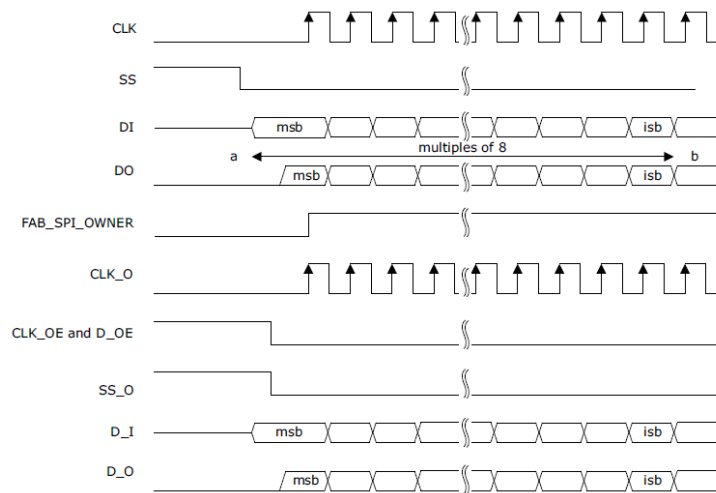
7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

Table 90 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V _{DDI} = 3.3 V Max	V _{DDI} = 2.5 V Max	V _{DDI} = 1.8 V Max	V _{DDI} = 1.5 V Max	V _{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins ¹	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Figure 4 • USPI Switching Characteristics

7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ ¹	Max
T _{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 μs		470 μs
T _{CONVN}	Time between subsequent channel conversions.		480 μs	
T _{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 μs.	0 ns		
T _{VALID} ²	Width of the valid pulse.	1.625 μs		2 μs
T _{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 μs	Rate × 32 μs	8128 μs

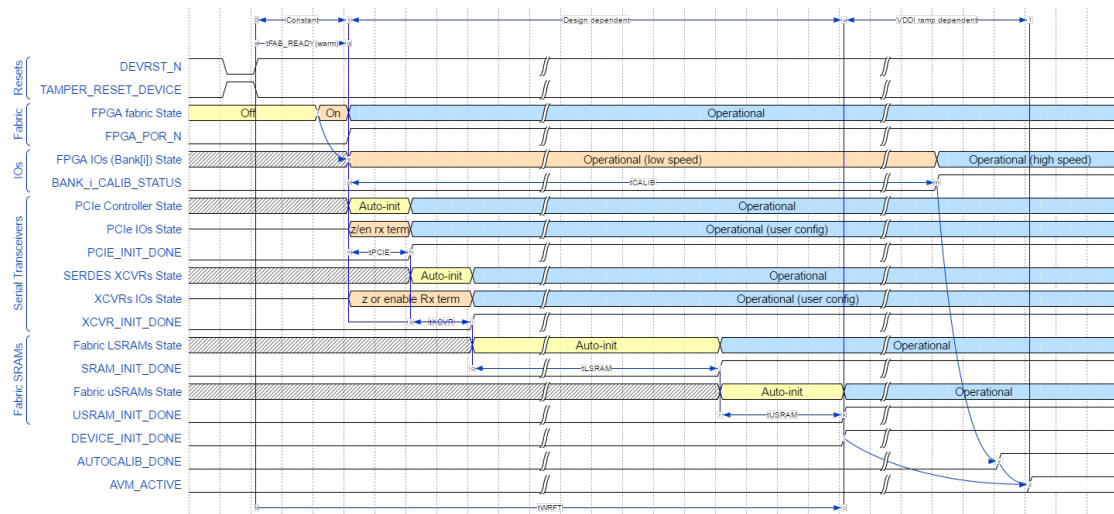
1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	-40		125	°C	
Temperature sensing accuracy	-10		10	°C	

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T _{FF_ENTRY}		59		μs	
The time from Flash*Freeze exit pin assertion to fabric operational state	T _{FF_FABRIC_UP}		133		μs	
The time from Flash*Freeze exit pin assertion to I/Os operational	T _{FF_IO_ACTIVE}		143		μs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T _{DISU}	TDI input setup time	0.0			ns	
T _{DIHD}	TDI input hold time	2.0			ns	
T _{TMSSU}	TMS input setup time	1.5			ns	
T _{TMSHD}	TMS input hold time	1.5			ns	
F _{TCK}	TCK frequency			25	MHz	
T _{TCKDC}	TCK duty cycle	40		60	%	
T _{TDOCQ}	TDO clock to Q out			8.4	ns	C _{LOAD} = 40 pf
T _{TRSTBCQ}	TRSTB clock to Q out			23.5	ns	C _{LOAD} = 40 pf
T _{TRSTBPW}	TRSTB min pulse width	50			ns	
T _{TRSTBREM}	TRSTB removal time	0.0			ns	
T _{TRSTBREC}	TRSTB recovery time	12.0			ns	
C _{INTDI}	TDI input pin capacitance			5.3	pf	
C _{INTMS}	TMS input pin capacitance			5.3	pf	
C _{INTCK}	TCK input pin capacitance			5.3	pf	
C _{INTTRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			20	MHz	

7.11 User Crypto

The following section describes user crypto.

7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 112 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V – 1	VDD = 1.05 V STD	VDD = 1.05 V – 1	Unit	Condition
Operating frequency	F _{MAX}	189		189		MHz	–40 °C to 100 °C

7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Throughput cycle count collected with Athena TeraFire Core and RISCv running at 100 MHz.

Table 113 • AES

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-ECB-128 encrypt ¹	128	515	1095
	64K	50157	933
AES-ECB-128 decrypt ¹	128	557	1760
	64K	48385	1524
AES-ECB-256 encrypt ¹	128	531	1203
	64K	58349	1203
AES-ECB-256 decrypt ¹	128	589	1676
	64K	56673	1671
AES-CBC-256 encrypt ¹	128	576	1169
	64K	52547	1169
AES-CBC-256 decrypt ¹	128	585	1744
	64K	48565	1652
AES-GCM-128 encrypt ¹ , 128-bit tag, (full message encrypted/authenticated)	128	1925	2740
	64K	60070	2158
AES-GCM-256 encrypt ¹ , 128-bit tag, (full message encrypted/authenticated)	128	1973	2268
	64K	60102	2151

1. With DPA counter measures.

Table 114 • GMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-GCM-256 ¹ , 128-bit tag, (message is only authenticated)	128	1863	2211
	64K	49707	2128

SigVer, DSA-2048/SHA-256	1024	9810527	10884
	8K	9597000	10719
Key Agreement (KAS), DH-3072 (p=3072, security=256)		4920705	9338
Key Agreement (KAS), DH-3072 (p=3072, security=256) ¹		78914533	9083

1. With DPA counter measures.

Table 122 • NRBG

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string		18221	2841
Reseed: no additional input, s=256		13585	1180
Reseed: 384-bit additional input, s=256		15922	1342
Generate: (no additional input), prediction resistance enabled, s= 256	128	15262	1755
	8K	27169	8223
Generate: (no additional input), prediction resistance disabled, s= 256	128	2138	1167
	8K	14045	8223
Generate: (384-bit additional input), prediction resistance enabled, s= 256	128	21299	1944
	8K	33206	8949
Generate: (384-bit additional input), prediction resistance disabled, s= 256	128	11657	1894
	8K	23564	8950
Un-instantiate		761	666

1. With DPA counter measures.