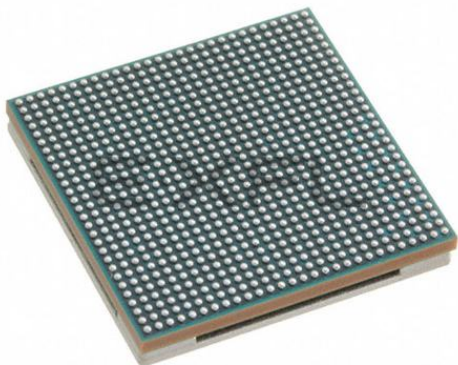




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	388
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-1fcg784i

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V _{DD}	−0.5	1.13	V
Transceiver Tx and Rx lanes supply	V _{DDA}	−0.5	1.13	V
Programming and HSIO receiver supply	V _{DD18}	−0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	−0.5	2.7	V
Transceiver PLL high-voltage supply	V _{DDA25}	−0.5	2.7	V
Transceiver reference clock supply	V _{DD_XCVR_CLK}	−0.5	3.6	V
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	−0.5	3.6	V
HSIO DC I/O supply ²	V _{DDIx}	−0.5	2.0	V
GPIO DC I/O supply ²	V _{DDIx}	−0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V _{DDI3}	−0.5	3.6	V
GPIO auxiliary power supply for I/O bank x ²	V _{DDAUXx}	−0.5	3.6	V
Maximum DC input voltage on GPIO	V _{IN}	−0.5	3.8	V
Maximum DC input voltage on HSIO	V _{IN}	−0.5	2.2	V
Transceiver Receiver absolute input voltage	Transceiver V _{IN}	−0.5	1.26	V
Transceiver Reference clock absolute input voltage	Transceiver REFCLK V _{IN}	−0.5	3.6	V
Storage temperature (ambient) ¹	T _{STG}	−65	150	°C
Junction temperature ¹	T _J	−55	135	°C
Maximum soldering temperature RoHS	T _{SOLROHS}		260	°C
Maximum soldering temperature leaded	T _{SOLPB}		220	°C

1. See [FPGA Programming Cycles vs Retention Characteristics](#) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as V_{DDIx} and V_{DDAUXx}.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode ¹	V _{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode ¹	V _{DD}	1.02	1.05	1.08	V
Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less) ¹	V _{DDA}	0.97	1.00	1.03	V

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section [Recommended Operating Conditions](#) (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V _{DD}	0.2	50	ms
Transceiver core supply	V _{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V _{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V _{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V _{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	V _{DDI} [0,1,6,7]	0.2	50	ms
GPIO bank I/O power supplies	V _{DDI} [2,4,5]	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V _{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	V _{DDAUX} [2,4,5]	0.2	50	ms
Transceiver reference clock supply	V _{DD_XCVR_CLK}	0.2	50	ms
Global V _{REF} for transceiver reference clocks	XCVR _{VREF}	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended) ^{1, 2}	XCVR _{RX_HS}			±4	mA	V _{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended) ³	XCVR _{TX_HS}			±10	mA	V _{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended) ⁴	XCVR _{REF_HS}			±1	mA	V _{DD_XCVR_CLK} = 0 V
Current per GPIO pin (P or N single-ended) ⁵	I _{GPIO_HS}			±1	mA	V _{DDI_X} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

- Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
- Each P and N transceiver input has less than the specified maximum input current.
- Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
- V_{DD_XCVR_CLK} is powered down and the device is driven to –0.3 V < V_{IN} < V_{DD_XCVR_CLK}.
- V_{DDI_X} is powered down and the device is driven to –0.3 V < V_{IN} < GPIO V_{DDI_{max}}.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	−0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTL	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	−0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	VDDAUX	VDDI	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3 ¹	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3 ¹	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3 ¹	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2 ¹	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2 ¹	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2 ¹	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	VDDAUX	VDDI	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2 ¹	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2 ¹	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
F _{MAX}	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
F _{MAX}	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
F _{MAX}	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX}	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
F _{MAX}	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
F _{MAX}	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
F _{MAX}	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
F _{MAX} 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F _{MAX} 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned ¹
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered ¹

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F _{MAX}	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output F _{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output F _{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter ¹	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency ²	F _{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F _{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	T _{OUTJITTERP}			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T _{SKEW}			±200	ps
DLL lock time	T _{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T _{MRPW}	3			ns
Minimum input pulse width ³	T _{MIPW}	20			ns
Minimum input clock pulse width high	T _{MPWH}	400			ps
Minimum input clock pulse width low	T _{MPWL}	400			ps
Delay step size	T _{DEL}	12.7	30	35	ps
Maximum delay block delay ⁴	T _{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input) ⁵	T _{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode) ⁵	T _{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4

RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{2FREQ}		2		MHz
Accuracy	RC _{2FACC}	−4		4	%
Duty cycle	RC _{2DC}	46		54	%
Peak-to-peak output period jitter	RC _{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC _{2CIIT}		5	10	ns
Operating current (V _{DD25})	RC _{2IVPPA}			60	μA
Operating current (V _{DD})	RC _{2IVDD}			2.6	μA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC _{SCFREQ}		160		MHz
Accuracy	RC _{SCFACC}	−4		4	%
Duty cycle	RC _{SCDC}	47		52	%
Peak-to-peak output period jitter	RC _{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC _{SCCIIT}			172	ps
Operating current (V _{DD25})	RC _{SCVPPA}			599	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

Table 44 • μ SRAM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	T_{ac}		2		2	ns	Read-port

Table 45 • μ PROM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit
Read access time	T_{ac}	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Tx data rate ^{1,2}	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled ²	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency ³	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode ²	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode ²	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Reference clock input rate ^{1,2}	$F_{TXREFCLK}$	20		800	20		800	MHz

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
FTxRefClk = 75 MHz with typical settings.
For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		$V_{DDA} + 0.3$	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC}^1	$0.7 \times V_{DDA}$		$0.9 \times V_{DDA}$	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance ²	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high) ⁹	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low) ⁹	$V_{DETLLOW}$	65		175	mV	Setting = PCIe ^{3,7}
	$V_{DETLLOW}$	95		190	mV	Setting = SATA ^{4,8}
	$V_{DETLLOW}$	75		170	mV	Setting = 1
	$V_{DETLLOW}$	95		185	mV	Setting = 2
	$V_{DETLLOW}$	100		190	mV	Setting = 3
	$V_{DETLLOW}$	140		210	mV	Setting = 4
	$V_{DETLLOW}$	155		240	mV	Setting = 5
	$V_{DETLLOW}$	165		245	mV	Setting = 6
	$V_{DETLLOW}$	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJITOL}				UI	>8.5 Gbps – 12.7 Gbps ^{5, 10}

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps ¹			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps ¹			UI

- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1,4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1,2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1,3}			s	Full scrubbing
Time to scrub the fabric data PNVM data (non-recoverable) ^{1,4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 79 • Zeroization Times for MPF300T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1,2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable) ^{1,4}			ms	One iteration of scrubbing
Time to scrub the fabric data ¹			s	Full scrubbing
Time to scrub the pNVM data (like new) ^{1,2}			s	Full scrubbing
Time to scrub the pNVM data (recoverable) ^{1,3}			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable) ^{1,4}			s	Full scrubbing
Time to verify ⁵			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 80 • Zeroization Times for MPF500T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data ¹			ms	Data erased
Time to destroy data in non-volatile memory (like new) ^{1,2}			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable) ^{1,3}			ms	One iteration of scrubbing

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

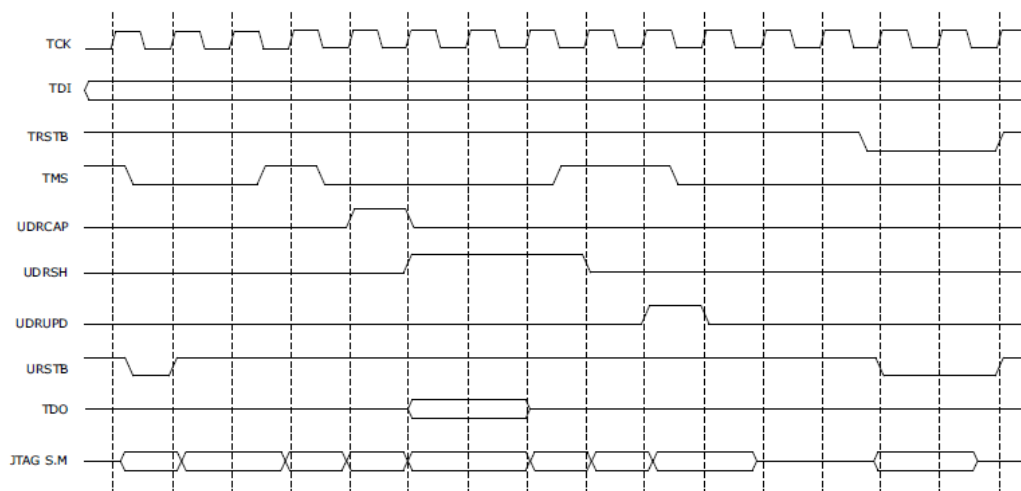
Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

Figure 3 • UJTAG Timing Diagram

7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 89 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F _{TCK}				MHz	

7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

Table 90 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V _{DDI} = 3.3 V Max	V _{DDI} = 2.5 V Max	V _{DDI} = 1.8 V Max	V _{DDI} = 1.5 V Max	V _{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins ¹	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Parameter	Min	Typ	Max	Unit	Condition
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 93 • Tamper Macro Timing Characteristics—Flags and Clearing

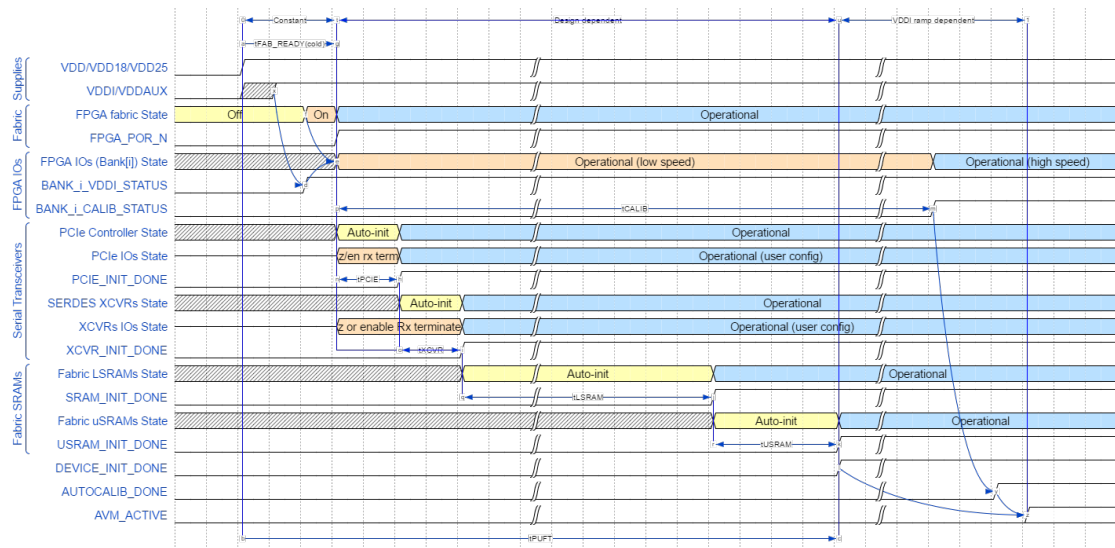
Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T _{JTAG_ACTIVE} ^{1, 2}	45	52	ns
	T _{MESH_ERR} ²	1.8	2.2	μs
	T _{CLK_GLITCH} ^{1, 2}			ns
	T _{CLK_FREQ} ^{1, 2}			μs
	T _{LOW_1P05} ²	70	108	μs
	T _{HIGH_1P8} ²	85	120	μs
	T _{HIGH_2P5} ²	130	520	μs
	T _{GLITCH_1P05} ²			μs
	T _{SECDEC} ^{1, 2}			μs
	T _{DRI_ERR} ²	14	18	μs
	T _{WDOG} ^{1, 2}			μs
	T _{LOCK_ERR} ²			μs
Time from system controller instruction execution to flag generation	T _{INST_BUF_ACCESS} ^{2, 3}	4	5	μs
	T _{INST_DEBUG} ^{2, 3}	3.3	4	μs
	T _{INST_CHK_DIGEST} ^{2, 3}	1.8	3	μs
	T _{INST_EC_SETUP} ^{2, 3}	1.8	2	μs
	T _{INST_FACT_PRIV} ^{2, 3}	3.8	5	μs
	T _{INST_KEY_VAL} ^{2, 3}	2.5	3.1	μs
	T _{INST_MISC} ^{2, 3}	1.5	2	μs
	T _{INST_PASSCODE_MATCH} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_SETUP} ^{2, 3}	4.2	5	μs
	T _{INST_PROG} ^{2, 3}	3.8	4.1	μs
	T _{INST_PUB_INFO} ^{2, 3}	4	4.5	μs
	T _{INST_ZERO_RECO} ^{2, 3}	2.5	3	μs
	T _{INST_PASSCODE_FAIL} ^{2, 3}	170	180	μs
	T _{INST_KEY_VAL_FAIL} ^{2, 3}	92	110	μs
	T _{INST_UNUSED} ^{2, 3}	4	5	μs
Time from sending the CLEAR to deassertion on FLAG	T _{CLEAR_FLAG}	17	23	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, but it is useful for security analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 94 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	T _{IO_DISABLE}	40	50	ns

Figure 5 • Cold Reset Timing

**Notes:**

- The previous diagram shows the case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
 - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
 - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
 - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2**Warm Reset Initialization Sequence**

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T _{FF_ENTRY}		59		μs	
The time from Flash*Freeze exit pin assertion to fabric operational state	T _{FF_FABRIC_UP}		133		μs	
The time from Flash*Freeze exit pin assertion to I/Os operational	T _{FF_IO_ACTIVE}		143		μs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T _{DISU}	TDI input setup time	0.0			ns	
T _{DIHD}	TDI input hold time	2.0			ns	
T _{TMSSU}	TMS input setup time	1.5			ns	
T _{TMSHD}	TMS input hold time	1.5			ns	
F _{TCK}	TCK frequency			25	MHz	
T _{TCKDC}	TCK duty cycle	40		60	%	
T _{TDOCQ}	TDO clock to Q out			8.4	ns	C _{LOAD} = 40 pf
T _{TRSTBCQ}	TRSTB clock to Q out			23.5	ns	C _{LOAD} = 40 pf
T _{TRSTBPW}	TRSTB min pulse width	50			ns	
T _{TRSTBREM}	TRSTB removal time	0.0			ns	
T _{TRSTBREC}	TRSTB recovery time	12.0			ns	
C _{INTDI}	TDI input pin capacitance			5.3	pf	
C _{INTMS}	TMS input pin capacitance			5.3	pf	
C _{INTCK}	TCK input pin capacitance			5.3	pf	
C _{INTTRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			20	MHz	

ECDSA SigVer, P-384/SHA-384	1024	6421841	5759
	8K	6273510	5759
Key Agreement (KAS), P-384		5039125	6514
Point Multiply, P-256 ¹		5176923	4482
Point Multiply, P-384 ¹		12043199	5319
Point Multiply, P-521 ¹		26887187	6698
Point Addition, P-384		3018067	5779
KeyGen (PKG), P-384		12055368	6908
Point Verification, P-384		5091	3049

1. With DPA counter measures.

Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048 ¹ , CRT	2048	26862392	15900
Decrypt, RSA-3072 ¹ , CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384 ¹ , CRT, PKCS #1 V 1.1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	148090970	14642
	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	970991	12000
	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	443493	8436
	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	973269	11313
	8K	983255	11146

1. With DPA counter measures.

Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SigGen, DSA-3072/SHA-384 ¹	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133