# Microchip Technology - MPF300T-1FCSG536E Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 300000 |
| Total RAM Bits | 21094400 |
| Number of I/O | 300 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.08V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 536-LFBGA, CSPBGA |
| Supplier Device Package | 536-CSPBGA (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-1fcsg536e |

# 6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

## 6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

### Table 3 • Absolute Maximum Rating

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| FPGA core power supply | $V_{DD}$ | –0.5 | 1.13 | V |
| Transceiver Tx and Rx lanes supply | $V_{DDA}$ | –0.5 | 1.13 | V |
| Programming and HSIO receiver supply | $V_{DD18}$ | –0.5 | 2.0 | V |
| FPGA core and FPGA PLL high-voltage supply | $V_{DD25}$ | –0.5 | 2.7 | V |
| Transceiver PLL high-voltage supply | $V_{DDA25}$ | –0.5 | 2.7 | V |
| Transceiver reference clock supply | $V_{DD\_XCVR\_CLK}$ | –0.5 | 3.6 | V |
| Global $V_{REF}$ for transceiver reference clocks | $XCVR_{VREF}$ | –0.5 | 3.6 | V |
| HSIO DC I/O supply[2] | $V_{DDIx}$ | –0.5 | 2.0 | V |
| GPIO DC I/O supply[2] | $V_{DDIx}$ | –0.5 | 3.6 | V |
| Dedicated I/O DC supply for JTAG and SPI | $V_{DDI3}$ | –0.5 | 3.6 | V |
| GPIO auxiliary power supply for I/O bank x[2] | $V_{DDAUXx}$ | –0.5 | 3.6 | V |
| Maximum DC input voltage on GPIO | $V_{IN}$ | –0.5 | 3.8 | V |
| Maximum DC input voltage on HSIO | $V_{IN}$ | –0.5 | 2.2 | V |
| Transceiver Receiver absolute input voltage | Transceiver $V_{IN}$ | –0.5 | 1.26 | V |
| Transceiver Reference clock absolute input voltage | Transceiver REFCLK $V_{IN}$ | –0.5 | 3.6 | V |
| Storage temperature (ambient)[1] | $T_{STG}$ | –65 | 150 | °C |
| Junction temperature[1] | $T_J$ | –55 | 135 | °C |
| Maximum soldering temperature RoHS | $T_{SOLROHS}$ |  | 260 | °C |
| Maximum soldering temperature leaded | $T_{SOLPB}$ |  | 220 | °C |

1. See FPGA Programming Cycles vs Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.
2. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

## 6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

### Table 4 • Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FPGA core supply at 1.0 V mode[1] | $V_{DD}$ | 0.97 | 1.00 | 1.03 | V |
| FPGA core supply at 1.05 V mode[1] | $V_{DD}$ | 1.02 | 1.05 | 1.08 | V |
| Transceiver TX and RX lanes supply at 1.0 V mode (when all lane rates are 10.3125 Gbps or less)[1] | $V_{DDA}$ | 0.97 | 1.00 | 1.03 | V |

### Table 8 • Maximum Overshoot During Transitions for GPIO

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 3.8 |
| 100 | 3.85 |
| 100 | 3.9 |
| 100 | 3.95 |
| 70 | 4 |
| 50 | 4.05 |
| 33 | 4.1 |
| 22 | 4.15 |
| 14 | 4.2 |
| 9.8 | 4.25 |
| 6.5 | 4.3 |
| 4.4 | 4.35 |
| 3 | 4.4 |
| 2 | 4.45 |
| 1.4 | 4.5 |
| 0.9 | 4.55 |
| 0.6 | 4.6 |

**Note:** Overshoot level is for $V_{DDI}$ at 3.3 V.

The following table shows the maximum AC input voltage ($V_{IN}$) undershoot duration for GPIO.

### Table 9 • Maximum Undershoot During Transitions for GPIO

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | –0.5 |
| 100 | –0.55 |
| 100 | –0.6 |
| 100 | –0.65 |
| 100 | –0.7 |
| 100 | –0.75 |
| 100 | –0.8 |
| 100 | –0.85 |
| 100 | –0.9 |
| 100 | –0.95 |
| 100 | –1 |
| 100 | –1.05 |
| 100 | –1.1 |
| 100 | –1.15 |
| 100 | –1.2 |
| 69 | –1.25 |
| 45 | –1.3 |

**Note**: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

## 6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

### 6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

**Table 12 • DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$[1] Max (V) |
|---|---|---|---|---|---|---|---|
| PCI | 3.15 | 3.3 | 3.45 | –0.3 | 0.3 × $V_{DDI}$ | 0.5 × $V_{DDI}$ | 3.45 |
| LVTTL | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 2.625 |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.89 |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.575 |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.26 |
| SSTL25I[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL25II[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL18I[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL18II[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| SSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Min (V) | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $V_{OH}$ Max (V) | $I_{OL}$[2,6] mA | $I_{OH}$[2,6] mA |
|---|---|---|---|---|---|---|---|---|---|
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | | $V_{OL}/50$ | $(V_{DDI} – V_{OH})/50$ |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | | $V_{OL}/50$ | $(V_{DDI} – V_{OH})/50$ |
| HSTL12II[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | | $V_{OL}/55$ | $(V_{DDI} – V_{OH})/55$ |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | | $V_{OL}/40$ | $(V_{DDI} – V_{OH})/40$ |
| POD12I[4,5] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | | $V_{OL}/48$ | $(V_{DDI} – V_{OH})/48$ |
| POD12II[4,5] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | | $V_{OL}/34$ | $(V_{DDI} – V_{OH})/34$ |

1. Drive strengths per PCI specification V/I curves.
2. Refer to UG0686: PolarFire FPGA User I/O User Guide for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. $I_{OL}/I_{OH}$ units for impedance standards in amps (not mA).
5. VOH_MAX based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
    a. HSIO lane: 120 mA per 12 IO buffers.
    b. GPIO lane: 160 mA per 12 IO buffers.

**Note:** 3.3 V and 2.5 V are only supported in GPIO banks.

### 6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

**Table 14 • Differential DC Input Levels**

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18[4] | GPIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| RSDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| MINILVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| SUBLVDS33 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS18[5] | HSIO | Mid (default) | 0.6 | 0.9 | 1.65 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS25 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS18[5] | HSIO | Mid (default) | 0.6 | 0.8 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| SLVS33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS18[5] | HSIO | Mid (default) | 0.6 | 1.00 | 1.65 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.3 |
| HCSL33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| HCSL25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL18[5] | HSIO | Mid (default) | 0.6 | 1.0 | 1.65 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.55 | 1.1 |
| BUSLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.1 | $V_{DDIn}$ |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.1 | $V_{DDIn}$ |
| MLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.35 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.35 | 2.4 |
| LVPECL33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| LVPECLE33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| MIPI25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.05 | 0.2 | 0.3 |

1. $V_{ICM}$ is the input common mode.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
    a. $V_{ICM}$ must be less than $V_{DDI}$ – 0.4 V;
    b. $V_{ICM} + V_{ID}/2$ must be $< V_{DDI} + 0.4$ V;
    c. $V_{ICM} - V_{ID}/2$ must be $> VSS - 0.3$ V;
    d. Any differential input with $V_{ICM} \leq 0.6$ V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

### Table 15 • Differential DC Output Levels

| I/O Standard | Bank Type | $V_{OCM}$[1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$[2] Min (V) | $V_{OD}$[2] Typ (V) | $V_{OD}$[2] Max (V) |
|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | | 1.2 | | 0.25 | 0.35 | 0.45 |
| LVDS25 | GPIO | | 1.2 | | 0.25 | 0.35 | 0.45 |
| LCMDS33 | GPIO | | 0.6 | | 0.25 | 0.35 | 0.45 |
| LCMDS25 | GPIO | | 0.6 | | 0.25 | 0.35 | 0.45 |
| RSDS33 | GPIO | | 1.2 | | 0.17 | 0.2 | 0.23 |
| RSDS25 | GPIO | | 1.2 | | 0.17 | 0.2 | 0.23 |
| MINILVDS33 | GPIO | | 1.2 | | 0.3 | 0.4 | 0.6 |
| MINILVDS25 | GPIO | | 1.2 | | 0.3 | 0.4 | 0.6 |
| SUBLVDS33 | GPIO | | 0.9 | | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | | 0.9 | | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | | 0.8 | | 0.17 | 0.2 | 0.23 |
| PPDS25 | GPIO | | 0.8 | | 0.17 | 0.2 | 0.23 |
| SLVSE15[3] | GPIO,<br>HSIO | | 0.2 | | 0.12 | 0.135 | 0.15 |
| BUSLVDSE25[3] | GPIO | | 1.25 | | 0.24 | 0.262 | 0.272 |

| I/O Standard | Bank Type | $V_{OCM}$[1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$[2] Min (V) | $V_{OD}$[2] Typ (V) | $V_{OD}$[2] Max (V) |
|---|---|---|---|---|---|---|---|
| MLVDSE25[3] | GPIO |  | 1.25 |  | 0.396 | 0.442 | 0.453 |
| LVPECLE33[3] | GPIO |  | 1.65 |  | 0.664 | 0.722 | 0.755 |
| MIPIE25[3] | GPIO |  | 0.25 |  | 0.1 | 0.22 | 0.3 |

1. $V_{OCM}$ is the output common mode voltage.
2. $V_{OD}$ is the output differential voltage.
3. Emulated output only.

### 6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

**Table 16 • Complementary Differential DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 |  |
| SSTL25II | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 |  |
| SSTL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 |  |
| SSTL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 |  |
| SSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 |  |
| SSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 |  |
| SSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 |  |
| SSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 |  |
| HSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 |  |
| HSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 |  |
| HSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 |  |
| HSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 |  |
| HSTL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 |  |
| HSUL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 |  |
| HSUL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 |  |
| HSUL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 |  |
| POD12I | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 |  |
| POD12II | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 |  |

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
   a. $V_{ICM}$ must be less than $V_{DDI}$ -0.4V;
   b. $V_{ICM}$ + $V_{ID}$/2 must be <$V_{DDI}$ + 0.4 V;
   c. $V_{ICM}$ – $V_{ID}$/2 must be >VSS – 0.3 V.

### Table 17 • Complementary Differential DC Output Levels

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Min (V) | $V_{OL}$ Max (V) | $V_{OH}$[1,3] Min (V) | $I_{OL}$[2] Min (mA) | $I_{OH}$[2] Min (mA) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | 8.1 |
| SSTL25II | 2.375 | 2.5 | 2.625 | | $V_{TT}$ – 0.810 | $V_{TT}$ + 0.810 | 16.2 | 16.2 |
| SSTL18I | 1.71 | 1.8 | 1.89 | | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | 6.7 |
| SSTL18II | 1.71 | 1.8 | 1.89 | | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| HSTL15I | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI}$ – 0.4 | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI}$ – 0.4 | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/55 | ($V_{DDI}$ – $V_{OH}$)/55 |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| POD12I[3,4] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | $V_{OL}$/48 | ($V_{DDI}$ – $V_{OH}$)/48 |
| POD12II[3,4] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |

1. $V_{OH}$ is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers
3. $V_{OH\_MAX}$ based on external pull-up termination (pseudo-open drain).
4. $I_{OL}$/$I_{OH}$ units for impedance standards in amps (not mA).

### 6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

### Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V/1.35 V/1.2 V |
| –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

**Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 34 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 48 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 80 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 80% of $V_{DDI}$.

**Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 50% of $V_{DDI}$.

### 6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

**Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank**

| Parameter | Description | Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination[1] | Internal differential termination | –20 | 100 | 20 | Ω | $V_{ICM} < 0.8$ V |
| | | –20 | 100 | 40 | Ω | 0.6 V < $V_{ICM}$ < 1.65 V |
| | | –20 | 100 | 80 | Ω | 1.4 V < $V_{ICM}$ |
| Single-ended thevenin termination[2, 3] | Internal parallel thevenin termination | –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| | | –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V |

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |

## Table 27 • GPIO Maximum Output Buffer Speed

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS25/LCMDS25 | 1250 | 1250 | Mbps |
| LVDS33/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25 | 800 | 800 | Mbps |
| MINILVDS25 | 800 | 800 | Mbps |
| SUBLVDS25 | 800 | 800 | Mbps |
| PPDS25 | 800 | 800 | Mbps |
| SLVSE15 | 500 | 500 | Mbps |
| BUSLVDSE25 | 500 | 500 | Mbps |
| MLVDSE25 | 500 | 500 | Mbps |
| LVPECLE33 | 500 | 500 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL25I (differential) | 800 | 800 | Mbps |
| SSTL25II (differential) | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL18I (differential) | 800 | 800 | Mbps |
| SSTL18II (differential) | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| SSTL15I (differential) | 800 | 1066 | Mbps |
| SSTL15II (differential) | 800 | 1066 | Mbps |
| HSTL15I | 900 | 900 | Mbps |
| HSTL15II | 900 | 900 | Mbps |
| HSTL15I (differential) | 900 | 900 | Mbps |
| HSTL15II (differential) | 900 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL18I (differential) | 400 | 400 | Mbps |
| HSUL18II (differential) | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS25 (16 mA) | 500 | 500 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |
| MIPIE25 | 500 | 500 | Mbps |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|---|---|
| FMAX 4:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 8:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 2:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 4:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |

**Table 48 • Transceiver Differential Reference Clock I/O Standards**

| I/O Standard | Comment |
|---|---|
| LVDS25 | For DC input levels, se e table Differential DC Input and Output Levels. |
| HCSL25 (for PCIe) | |

**Note:** The transceiver reference clock differential receiver supports $V_{CM}$ common mode.

## 7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

**Table 49 • Transceiver Single-Ended Reference Clock I/O Standards**

| I/O Standard | Comment |
|---|---|
| LVCMOS25 | For DC input levels, see table DC Input and Output Levels. |

## 7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

**Table 50 • Transceiver Reference Clock Input Termination**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Single-ended termination | RefTerm | | 50 | | Ω |
| Single-ended termination | RefTerm | | 75 | | Ω |
| Single-ended termination | RefTerm | | 150 | | Ω |
| Differential termination | RefDiffTerm | | 115[1] | | Ω |
| Power-up termination | | | >50K | | Ω |

1. Measured at VCM= 1.2 V and VID= 350 mV.

**Note**: All pull-ups are disabled at power-up to allow hot plug capability.

**Table 51 • PolarFire Transceiver User Interface Clocks**

| Parameter | Modes [1] | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|---|
| Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 4.8 Gbps | | 300 | | 300 | MHz |
| | 20-bit, max data rate = 6.0 Gbps | | 300 | | 300 | MHz |
| | 32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 325 | | 325 | MHz |
| | 40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 260 | | 320 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 165 | | 160 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps(–STD) / 12.7 Gbps (–1)[1] | | 130 | | 130 | MHz |
| | Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | | 150 | | 150 | MHz |
| | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |

### Table 75 • FPGA Programming Cycles Lifetime Factor

| Programming $T_J$ | Programming Cycles | LF |
|---|---|---|
| –40 °C to 100 °C | 500 | 1 |
| –40 °C to 85 °C | 1000 | 0.8 |
| –40 °C to 55 °C | 2000 | 0.6 |

**Notes:**

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures ($T_J$).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C $T_J$. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

## 7.6.5 Digest Time

The following table describes digest time.

### Table 76 • Digest Times

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| Setup time | All | 2 | | µs |
| Fabric digest run time | MPF100T, TL, TS, TLS | | | ms |
| | MPF200T, TL, TS, TLS | 1005 | 1072 | ms |
| | MPF300T, TL, TS, TLS | 1503.9 | 1582 | ms |
| | MPF500T, TL, TS, TLS | | | ms |
| UFS CC digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 33.2 | 35 | µs |
| | MPF300T, TL, TS, TLS | 33.2 | 35 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| sNVM digest run time[1] | MPF100T, TL, TS, TLS | | | ms |
| | MPF200T, TL, TS, TLS | 4.4 | 4.8 | ms |
| | MPF300T, TL, TS, TLS | 4.4 | 4.8 | ms |
| | MPF500T, TL, TS, TLS | | | ms |
| UFS UL digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 46.6 | 48.8 | µs |
| | MPF300T, TL, TS, TLS | 46.6 | 48.8 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| User key digest run time[2] | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 525.4 | 543.3 | µs |
| | MPF300T, TL, TS, TLS | 525.4 | 543.3 | µs |
| | MPF500T, TL, TS, TLS | | | µs |

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| UFS UPERM digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 33.2 | 34.9 | µs |
| | MPF300T, TL, TS, TLS | 33.2 | 34.9 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| Factory digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 493.6 | 510.1 | µs |
| | MPF300T, TL, TS, TLS | 493.6 | 510.1 | µs |
| | MPF500T, TL, TS, TLS | | | µs |

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

**Note:** These times do not include the power-up to functional timing overhead when using digest checks on power-up.

### 7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

**Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | | | ms | Zip flag set |
| Time to destroy the fabric data[1] | | | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | | | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | | | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | | | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | | | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | | | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | | | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1, 4] | | | s | Full scrubbing |
| Time to verify[5] | | | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

**Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | | | ms | Zip flag set |
| Time to destroy the fabric data[1] | | | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | | | ms | One iteration of scrubbing |

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | | | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | | | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | | | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | | | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1] | | | s | Full scrubbing |
| Time to verify[5] | | | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

### 7.6.7 Verify Time

The following tables describe verify time.

**Table 81 • Standalone Fabric Verify Times**

| Parameter | Devices | Max | Unit |
|---|---|---|---|
| Standalone verification over JTAG | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 53[1] | s |
| | MPF300T, TL, TS, TLS | 90[1] | s |
| | MPF500T, TL, TS, TLS | | s |
| Standalone verification over SPI | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 37[2] | s |
| | MPF300T, TL, TS, TLS | 55[2] | s |
| | MPF500T, TL, TS, TLS | | s |

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

**Notes:**

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

**Table 82 • Verify Time by Programming Hardware**

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF100T, TL, TS, TLS | | | | | | |
| MPF200T, TL, TS, TLS | 9 | 67 | 53 | | | s |
| MPF300T, TL, TS, TLS | 14 | 95 | 90 | | | s |

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF500T, TL, TS, TLS | | | | | | |

**Notes:**

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

**Table 83 • Verify System Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| In application verify by index | $T_{IAP\_Ver\_Index}$ | 44H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | | | s |
| In application verify by SPI address | $T_{IAP\_Ver\_Addr}$ | 45H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | | | s |

## 7.6.8 Authentication Time

The following tables describe authentication system service time.

**Table 84 • Authentication Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Bitstream Authentication | $T_{BIT\_AUTH}$ | 22H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | | | s |
| IAP Image Authentication | $T_{IAP\_AUTH}$ | 23H | MPF100T, TL, TS, TLS | | | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | | | |

## 7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

**Table 85 • sNVM Read/Write Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Plain text programming | | 7.0 | 7.2 | 7.9 | ms | |
| Authenticated text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authenticated and encrypted text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authentication R/W 1st access from power-up overhead | $T_{PUF\_OVHD}$ | | 100 | 111 | ms | From $T_{FAB\_READY}$ |
| Plain text read | | 7.67 | 7.79 | 8.2 | µs | |

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Authenticated text read |  | 113.25 | 114.02 | 118.5 | µs |  |
| Authenticated and decrypted text read |  | 159.59 | 160.53 | 166.5 | µs |  |

**Notes:**

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- $T_{PUF\_OVHD}$ is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

### 7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

**Table 86 • sNVM Programming Cycles vs. Retention Characteristics**

| Programming Temperature | Programming Cycles per Page, Max | Programming Cycles per Block, Max | Retention Years |
|---|---|---|---|
| –40 °C to 100 °C | 10,000 | 100,000 | 20 |
| –40 °C to 85 °C | 10,000 | 100,000 | 20 |
| –40 °C to 55 °C | 10,000 | 100,000 | 20 |

**Note:** Page size = 128 bytes. Block size = 56 KBytes.

## 7.7 System Services

This section describes system switching and throughput characteristics.

### 7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

**Table 87 • System Services Throughput Characteristics**

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Serial number | $T_{Serial}$ | 00H | 65 | 67 | µs |  |
| User code | $T_{User}$ | 01H | 0.8 | 1.05 | µs |  |
| Design information | $T_{Design}$ | 02H | 2.4 | 2.7 | µs |  |
| Device certificate | $T_{Cert}$ | 03H | 255 | 271 | ms |  |
| Read digests | $T_{digest\_read}$ | 04H | 201 | 215 | µs |  |
| Query security locks | $T_{sec\_Query}$ | 05H | 15 | 17 | µs |  |
| Read debug information | $T_{Rd\_debug}$ | 06H | 34 | 38 | µs |  |
| Reserved |  | 07H–0FH |  |  |  |  |
| Secure NVM write plain text | $T_{SNVM\_Wr\_Plain}$ | 10H |  |  |  | Note 1 |
| Secure NVM write authenticated plain text | $T_{SNVM\_Wr\_Auth}$ | 11H |  |  |  | Note 1 |
| Secure NVM write authenticated cipher text | $T_{SNVM\_Wr\_Cipher}$ | 12H |  |  |  | Note 1 |
| Reserved |  | 13H–17H |  |  |  |  |

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Secure NVM read | $T_{SNVM\_Rd}$ | 18H | | | | Note 1 |
| Digital signature service raw | $T_{SIG\_RAW}$ | 19H | 174 | 187 | ms | |
| Digital signature service DER | $T_{SIG\_DER}$ | 1AH | 174 | 187 | ms | |
| Reserved | | 1BH–1FH | | | | |
| PUF emulation | $T_{Challenge}$ | 20H | 1.8 | 2.0 | ms | |
| Nonce service | $T_{Nonce}$ | 21H | 1.2 | 1.4 | ms | |
| Bitstream authentication | TBIT_AUTH | 22H | | | | Note 4 |
| IAP Image authentication | TIAP_AUTH | 23H | | | | Note 4 |
| Reserved | | 26H–3FH | | | | |
| In application programming by index | $T_{IAP\_Prg\_Index}$ | 42H | | | | Note 2 |
| In application programming by SPI address | $T_{IAP\_Prg\_Addr}$ | 43H | | | | Note 2 |
| In application verify by index | TIAP_Ver_Index | 44H | | | | Note 5 |
| In application verify by SPI address | TIAP_Ver_Addr | 45H | | | | Note 5 |
| Auto update | $T_{AutoUpdate}$ | 46H | | | | Note 2 |
| Digest check | $T_{digest\_chk}$ | 47H | | | | Note 3 |

1. See sNVM Read/Write Characteristics (see page 58).
2. See SPI Master Programming Time (see page 52).
3. See Digest Times (see page 54).
4. See Authentication Services Time (see page 58).
5. See Verify Services Time (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

## 7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

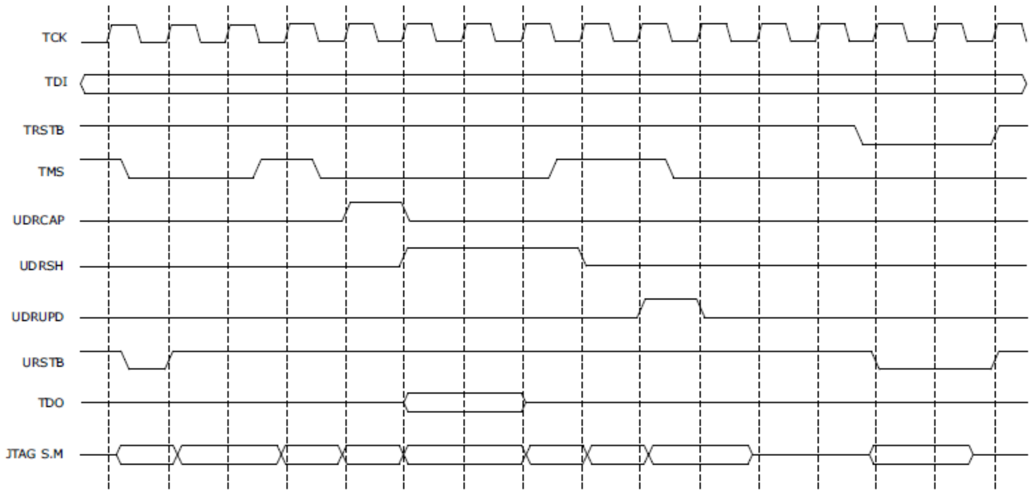
### 7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

**Table 88 • UJTAG Performance Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | | | 25 | MHz | |

**Figure 3 • UJTAG Timing Diagram**



## 7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

**Table 89 • UJTAG Security Performance Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | | | | MHz | |

## 7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

**Table 90 • SPI Macro Interface Timing Characteristics**

| Parameter | Symbol | $V_{DDI}$ = 3.3 V Max | $V_{DDI}$ = 2.5 V Max | $V_{DDI}$ = 1.8 V Max | $V_{DDI}$ = 1.5 V Max | $V_{DDI}$ = 1.2 V Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay from the fabric to pins[1] | TPD_MOSI | 0.8 | 1 | 1.2 | 1.4 | 1.6 | ns |
| | TPD_MISO | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SS | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SCK | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_MOSI_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SS_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SCK_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

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