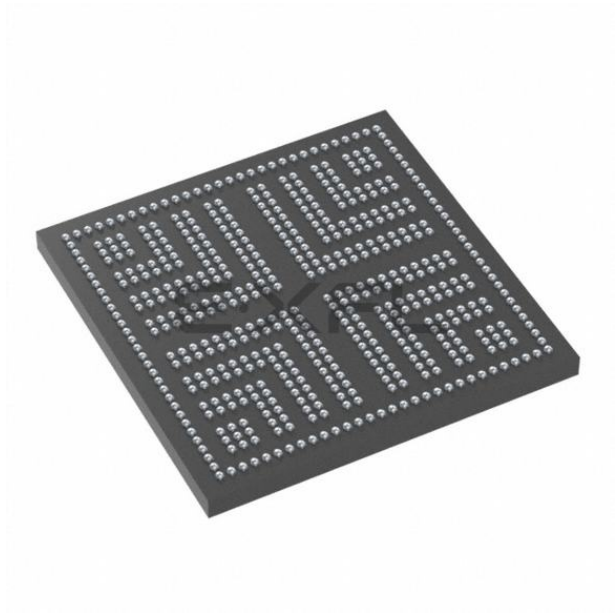

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-1fcsg536i

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see System Services (see page 59).
- The Non-Volatile Characteristics section was updated. For more information, see Non-Volatile Characteristics (see page 51).
- The Fabric Macros section was updated. For more information, see Fabric Macros (see page 60).
- The Transceiver Switching Characteristics section was updated. For more information, see Transceiver Switching Characteristics (see page 42).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed and HSIO Maximum Output Buffer Speed.
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications.
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics.
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
PCI	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45
LVTTL	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89
LVCMOS15	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575
LVCMOS12	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26
SSTL25I[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL25II[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL18I[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL18II[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575

Table 13 • DC Output Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{OL} Min (V)	V_{OL} Max (V)	V_{OH} Min (V)	V_{OH} Max (V)	I_{OL}[2,6] mA	I_{OH}[2,6] mA
PCI[1]	3.15	3.3	3.45		0.1 × V_{DDI}	0.9 × V_{DDI}		1.5	0.5
LVTTL	3.15	3.3	3.45		0.4	2.4			
LVCMOS33	3.15	3.3	3.45		0.4	V_{DDI} – 0.4			
LVCMOS25	2.375	2.5	2.625		0.4	V_{DDI} – 0.4			
LVCMOS18	1.71	1.8	1.89		0.45	V_{DDI} – 0.45			
LVCMOS15	1.425	1.5	1.575		0.25 × V_{DDI}	0.75 × V_{DDI}			
LVCMOS12	1.14	1.2	1.26		0.25 × V_{DDI}	0.75 × V_{DDI}			
SSTL25I[3]	2.375	2.5	2.625		V_{TT} – 0.608	V_{TT} + 0.608		8.1	8.1
SSTL25II[3]	2.375	2.5	2.625		V_{TT} – 0.810	V_{TT} + 0.810		16.2	16.2
SSTL18I[3]	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603		6.7	6.7
SSTL18II[3]	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603		13.4	13.4
SSTL15I[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
SSTL15II[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH}) /34
SSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
SSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH}) /34
HSTL15I	1.425	1.5	1.575		0.4	V_{DDI} – 0.4		8	8
HSTL15II	1.425	1.5	1.575		0.4	V_{DDI} – 0.4		16	16

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
HCSL25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18[5]	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V_{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V_{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} – 0.4 V;
   b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
   c. V_{ICM} – V_{ID}/2 must be >VSS – 0.3 V;
   d. Any differential input with V_{ICM} ≤0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15[3]	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25[3]	GPIO		1.25		0.24	0.262	0.272

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
MLVDSE25[3]	GPIO		1.25		0.396	0.442	0.453
LVPECLE33[3]	GPIO		1.65		0.664	0.722	0.755
MIPIE25[3]	GPIO		0.25		0.1	0.22	0.3

1. V_{OCM} is the output common mode voltage.
2. V_{OD} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} -0.4V;
   b. $V_{ICM} + V_{ID}/2$ must be $<V_{DDI} + 0.4$ V;
   c. $V_{ICM} – V_{ID}/2$ must be >VSS – 0.3 V.

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL18I	SSTL 1.8 V Class I	50	0	V_{REF}	0.9
SSTL18II	SSTL 1.8 V Class II	50	0	V_{REF}	0.9
SSTL15I	SSTL 1.5 V Class I	50	0	V_{REF}	0.75
SSTL15II	SSTL 1.5 V Class II	50	0	V_{REF}	0.75
SSTL135I	SSTL 1.35 V Class I	50	0	V_{REF}	0.675
SSTL135II	SSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL15I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	V_{REF}	0.75
HSTL15II	HSTL 1.5 V Class II	50	0	V_{REF}	0.75
HSTL135I	HSTL 1.35 V Class I	50	0	V_{REF}	0.675
HSTL135II	HSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL12	HSTL 1.2 V	50	0	V_{REF}	0.6
HSUL18I	High-speed unterminated logic 1.8 V Class I	50	0	V_{REF}	0.9
HSUL18II	HSUL 1.8 V Class II	50	0	V_{REF}	0.9
HSUL12	HSUL 1.2 V	50	0	V_{REF}	0.6
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	V_{REF}	0.84
POD12II	POD 1.2 V Class II	50	0	V_{REF}	0.84
LVDS33	LVDS 3.3 V	100	0	0[1]	0
LVDS25	LVDS 2.5 V	100	0	0[1]	0
LVDS18	LVDS 1.8 V	100	0	0[1]	0
RSDS33	Reduced swing differential signaling 3.3 V	100	0	0[1]	0
RSDS25	RSDS 2.5 V	100	0	0[1]	0
RSDS18	RSDS 1.8 V	100	0	0[1]	0
MINILVDS33	Mini-LVDS 3.3 V	100	0	0[1]	0
MINILVDS25	Mini-LVDS 2.5 V	100	0	0[1]	0
SUBLVDS33	Sub-LVDS 3.3 V	100	0	0[1]	0
SUBLVDS25	Sub-LVDS 2.5 V	100	0	0[1]	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	0[1]	0
PPDS25	PPDS 2.5 V	100	0	0[1]	0
BUSLVDSE25	Bus LVDS	100	0	0[1]	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	0[1]	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	0[1]	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	0[1]	0

1. The value given is the differential output voltage.

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps

1. Performance is achieved with V_{ID} ≥200 mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps

Standard	STD	–1	Unit
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
FMAX	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
FMAX	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
FMAX	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
FMAX	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
FMAX	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
FMAX	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
FMAX 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
FMAX 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
FMAX 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	µA
Operating current (V_{DD})	RC_{SCVDD}			60.7	µA

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2, 3]	$F_{XCVRREFCLKMAX\ CASCADE}$	20		156	20		156	MHz
Reference clock rate at the PFD[4]	$F_{TXREFCLKPFD}$	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4]	$F_{TXREFCLKPFD10G}$	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5]	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 10 KHz	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 100 KHz	$F_{TXREFPN}$			–115			–115	dBc /Hz
Phase noise at 1 MHz	$F_{TXREFPN}$			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	$T_{REFRISE}$		200	500		200	500	ps
Reference clock input fall time (90%–10%)	$T_{REFFALL}$		200	500		200	500	ps
Reference clock duty cycle	$T_{REFDUTY}$	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	Mhz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

		Retention Since Programmed (N = Number Digests During that Time)[1]								
Digest T_J	Storage and Operating T_J	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	$T_{IAP\_Ver\_Index}$	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	$T_{IAP\_Ver\_Addr}$	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T_{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T_{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T_{PUF_OVHD}		100	111	ms	From T_{FAB_READY}
Plain text read		7.67	7.79	8.2	µs	

Table 104 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T_{FF_ENTRY}		59		µs	
The time from Flash*Freeze exit pin assertion to fabric operational state	$T_{FF\_FABRIC\_UP}$		133		µs	
The time from Flash*Freeze exit pin assertion to I/Os operational	$T_{FF\_IO\_ACTIVE}$		143		µs	

7.10 Dedicated Pins

The following section describes the dedicated pins.

7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 105 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T_{DISU}	TDI input setup time	0.0			ns	
T_{DIHD}	TDI input hold time	2.0			ns	
T_{TMSSU}	TMS input setup time	1.5			ns	
T_{TMSHD}	TMS input hold time	1.5			ns	
F_{TCK}	TCK frequency			25	MHz	
T_{TCKDC}	TCK duty cycle	40		60	%	
T_{TDOCQ}	TDO clock to Q out			8.4	ns	C_{LOAD} = 40 pf
T_{RSTBCQ}	TRSTB clock to Q out			23.5	ns	C_{LOAD} = 40 pf
T_{RSTBPW}	TRSTB min pulse width	50			ns	
$T_{RSTBREM}$	TRSTB removal time	0.0			ns	
$T_{RSTBREC}$	TRSTB recovery time	12.0			ns	
CIN_{TDI}	TDI input pin capacitance			5.3	pf	
CIN_{TMS}	TMS input pin capacitance			5.3	pf	
CIN_{TCK}	TCK input pin capacitance			5.3	pf	
CIN_{TRSTB}	TRSTB input pin capacitance			5.3	pf	

7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 106 • SPI Master Mode (PolarFire Master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			20	MHz	

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F_{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T_{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T_{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR_{RAMP}		10		µs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR_{ASSERT}	1			µs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	$DR_{DEASSERT}$	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF_{RAMP}		10		µs	
Minimum FF_EXIT_N assert time	FF_{ASSERT}	1			µs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	$FF_{DEASSERT}$	170			µs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

ECDSA SigVer, P-384/SHA-384	1024	6421841	5759
	8K	6273510	5759
Key Agreement (KAS), P-384		5039125	6514
Point Multiply, P-256[1]		5176923	4482
Point Multiply, P-384[1]		12043199	5319
Point Multiply, P-521[1]		26887187	6698
Point Addition, P-384		3018067	5779
KeyGen (PKG), P-384		12055368	6908
Point Verification, P-384		5091	3049

1. With DPA counter measures.

Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048[1], CRT	2048	26862392	15900
Decrypt, RSA-3072[1], CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384[1] ,CRT, PKCS #1 V 1 1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	148090970	14642
	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	970991	12000
	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	443493	8436
	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	973269	11313
	8K	983255	11146

1. With DPA counter measures.

Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SigGen, DSA-3072/SHA-384[1]	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133