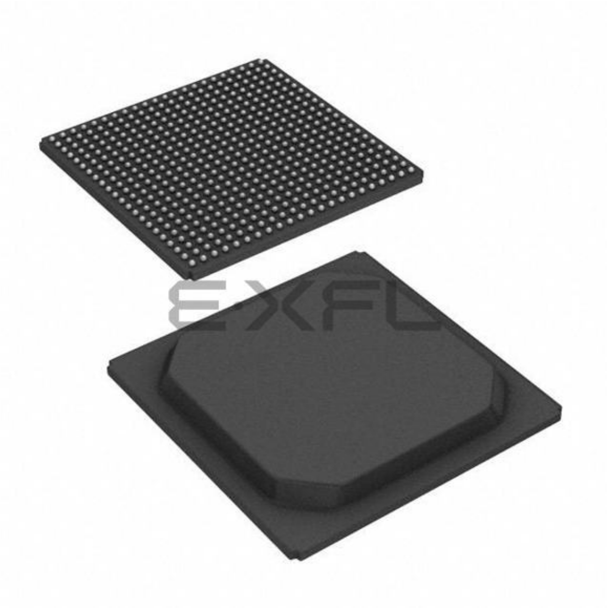

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (19x19)
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Contents

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V_{IN}) Undershoot Duration as % at T_J = 100 °C	Condition (V)
100	–0.5
100	–0.55
100	–0.6
100	–0.65
100	–0.7
100	–0.75
100	–0.8
100	–0.85
100	–0.9
100	–0.95
100	–1
100	–1.05
100	–1.1
100	–1.15
100	–1.2
69	–1.25
45	–1.3

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{OL} Min (V)	V_{OL} Max (V)	V_{OH} Min (V)	V_{OH} Max (V)	I_{OL}[2,6] mA	I_{OH}[2,6] mA
HSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH}) /50
HSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSTL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH}) /50
HSTL12II[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSUL18I[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/55	(V_{DDI} – V_{OH}) /55
HSUL18II[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSUL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
POD12I[4,5]	1.14	1.2	1.26		0.5 × V_{DDI}			V_{OL}/48	(V_{DDI} – V_{OH}) /48
POD12II[4,5]	1.14	1.2	1.26		0.5 × V_{DDI}			V_{OL}/34	(V_{DDI} – V_{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to UG0686: PolarFire FPGA User I/O User Guide for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. VOH_MAX based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18[4]	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18[5]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18[5]	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18[5]	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18[5]	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
PCI	PCIE 3.3 V	0	VDDI			VDDI/2		V
LVTTL33	LVTTL 3.3 V	0	VDDI			VDDI/2		V
LVCMOS33	LVCMOS 3.3 V	0	VDDI			VDDI/2		V
LVCMOS25	LVCMOS 2.5 V	0	VDDI			VDDI/2		V
LVCMOS18	LVCMOS 1.8 V	0	VDDI			VDDI/2		V
LVCMOS15	LVCMOS 1.5 V	0	VDDI			VDDI/2		V
LVCMOS12	LVCMOS 1.2 V	0	VDDI			VDDI/2		V
SSTL25I	SSTL 2.5 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL25II	SSTL 2.5 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL18I	SSTL 1.8 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL18II	SSTL 1.8 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL15I	SSTL 1.5 V Class I	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL15II	SSTL 1.5 V Class II	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL135I	SSTL 1.35 V Class I	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
SSTL135II	SSTL 1.35 V Class II	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
HSTL15I	HSTL 1.5 V Class I	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL15II	HSTL 1.5 V Class II	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL135I	HSTL 1.35 V Class I	V_{REF} – 0.45	V_{REF} + .45			V_{REF}	0.675	V
HSTL135II	HSTL 1.35 V Class II	V_{REF} – .45	V_{REF} + .45			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	V_{REF} – .4	V_{REF} + .4			V_{REF}	0.60	V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSUL18I	HSUL 1.8 V Class I	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL18II	HSUL 1.8 V Class II	V_{REF} – 0.54	V_{REF} + 0.54			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	V_{REF} – .22	V_{REF} + .22			V_{REF}	0.60	V
POD12I	Pseudo open drain (POD) logic 1.2 V Class I	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
POD12II	POD 1.2 V Class II	V_{REF} – .15	V_{REF} + .15			V_{REF}	0.84	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS18	LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS33	Mini-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS25	Mini-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MINILVDS18	Mini-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SUBLVDS33	Sub-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS25	Sub-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SUBLVDS18	Sub-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
SLVS33	Scalable low-voltage signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Standard	STD	–1	Unit
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_SDR_G_A	Rx SDR							MHz	From a global clock source, aligned
FMAX	RX_SDR_L_A	Rx SDR							MHz	From a lane clock source, aligned
FMAX	RX_SDR_G_C	Rx SDR							MHz	From a global clock source, centered
FMAX	RX_SDR_L_C	Rx SDR							MHz	From a lane clock source, centered

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_DDR_G_A	Rx DDR		335			335	MHz	MHz	From a global clock source, aligned
FMAX	RX_DDR_L_A	Rx DDR		250			250		MHz	From a lane clock source, aligned
FMAX	RX_DDR_G_C	Rx DDR		335			335		MHz	From a global clock source, centered
FMAX	RX_DDR_L_C	Rx DDR		250			250		MHz	From a lane clock source, centered
FMAX 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned[1]
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered[1]

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output FMAX 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Parameter	Symbol	Min	Typ	Max	Unit
Maximum input period clock jitter (reference and feedback clocks)[2]	F_{MAXINJ}		120	1000	ps
PLL VCO frequency	F_{VCO}	800		5000	MHz
Loop bandwidth (Int)[3]	F_{BW}	F_{PHDET}/55	F_{PHDET}/44	F_{PHDET}/30	MHz
Loop bandwidth (FRAC)[3]	F_{BW}	F_{PHDET}/91	F_{PHDET}/77	F_{PHDET}/56	MHz
Static phase offset of the PLL outputs[4]	T_{SPO}			Max (±60 ps, ±0.5 degrees)	ps
	$T_{OUTJITTER}$				ps
PLL output duty cycle precision	$T_{OUTDUTY}$	48		54	%
PLL lock time[5]	T_{LOCK}			Max (6.0 µs, 625 PFD cycles)	µs
PLL unlock time[6]	T_{UNLOCK}	2		8	PFD cycles
PLL output frequency	F_{OUT}	0.050		1250	MHz
Minimum reset pulse width	T_{MRPW}				µs
Maximum delay in the feedback path[7]	F_{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread[8]	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency[9]	Mod_Freq	F_{PHDETF}/(128x63)	32	F_{PHDETF}/(128)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

Note: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

7.2.3 DLL

The following table provides information about DLL.

Table 38 • DLL Electrical Characteristics

Parameter[1]	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F_{INF}	133		800	MHz
Input feedback clock frequency	F_{INFDBF}	133		800	MHz
Primary output clock frequency	F_{OUTPF}	133		800	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 44 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 45 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1,2]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled[2]	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[3]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode[2]	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode [2]	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz

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Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}		85		Ω	
	V_{OTERM}		100		Ω	
	V_{OTERM}		150		Ω	
Common mode voltage[1]	V_{OCM}	0.44 × V_{DDA}	0.525 × V_{DDA}	0.59 × V_{DDA}	V	DC coupled 50% setting
	V_{OCM}	0.52 × V_{DDA}	0.6 × V_{DDA}	0.66 × V_{DDA}	V	DC coupled 60% setting
	V_{OCM}	0.61 × V_{DDA}	0.7 × V_{DDA}	0.75 × V_{DDA}	V	DC coupled 70% setting
	V_{OCM}	0.63 × V_{DDA}	0.8 × V_{DDA}	0.83 × V_{DDA}	V	DC coupled 80% setting
Rise time[2]	T_{TxRF}	41		70	ps	20% to 80%
Fall time[2]		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew[3]	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew[4]	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time[7]	TTxEITrEntry				ns	
Electrical idle transition exit time[7]	TTxEITrExit				ns	
Electrical idle amplitude	VTxEIpp				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time[8]	$T_{DPLLLock}$				REFCLK UIs	
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}				UI UI	Data rate ≥8.5 Gbps to 12.7 Gbps[9] (Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥3.2 Gbps to 8.5 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥1.6 Gbps to 3.2 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.13 0.02	UI UI	Data rate ≥ 800 Mbps to 1.6 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.06 0.01	UI UI	Data rate = 250 Mbps to 800 Mbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps[5]
		0.41			UI	>1.6 to 3.2 Gbps[5]
		0.41			UI	>0.8 to 1.6 Gbps [5]
		0.41			UI	250 to 800 Mpbs [5]
Total jitter tolerance with stressed eye	$T_{TJTOLSE}$	0.65			UI	3.125 Gbps[5]
		0.65			UI	6.25 Gbps[6]
		0.7			UI	10.3125 Gbps[6]
					UI	12.7 Gbps[6, 10]
Sinusoidal jitter tolerance with stressed eye	$T_{SJTOLSE}$	0.1			UI	3.125 Gbps[5]
		0.05			UI	6.25 Gbps[6]
		0.05			UI	10.3125 Gbps[6]
					UI	12.7 Gbps[6, 10]
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

1. Valid at 3.2 Gbps and below.
2. Data vs. Rx reference clock frequency.
3. Achieves compliance with PCIe electrical idle detection.
4. Achieves compliance with SATA OOB specification.
5. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
6. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
7. For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
8. For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
9. Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
10. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	µs	
Authenticated and decrypted text read		159.59	160.53	166.5	µs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	µs	
User code	T_{User}	01H	0.8	1.05	µs	
Design information	T_{Design}	02H	2.4	2.7	µs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	µs	
Query security locks	T_{sec_Query}	05H	15	17	µs	
Read debug information	T_{Rd_debug}	06H	34	38	µs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM\_Wr\_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM\_Wr\_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM\_Wr\_Cipher}$	12H				Note 1
Reserved		13H–17H				

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