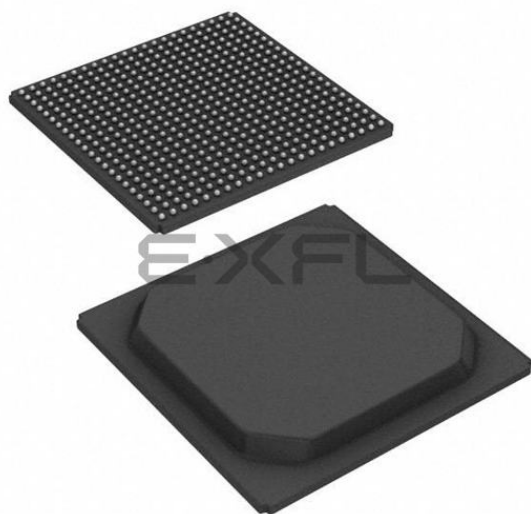




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-fcg484e

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see [System Services \(see page 59\)](#).
- The Non-Volatile Characteristics section was updated. For more information, see [Non-Volatile Characteristics \(see page 51\)](#).
- The Fabric Macros section was updated. For more information, see [Fabric Macros \(see page 60\)](#).
- The Transceiver Switching Characteristics section was updated. For more information, see [Transceiver Switching Characteristics \(see page 42\)](#).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see [HSIO Maximum Input Buffer Speed](#) and [HSIO Maximum Output Buffer Speed](#).
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see [I/O Standards Specifications](#).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see [Non-Volatile Characteristics](#).
- A note was added defining power down conditions for programming recovery conditions. For more information, see [Power-Supply Ramp Times](#).

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps) ¹	V _{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V _{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V _{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V _{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	V _{DD_XCVR_CLK}	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	V _{DD_XCVR_CLK}	2.375	2.5	2.625	V
Global V _{REF} for transceiver reference clocks ³	XCVR _{VREF}	Ground		V _{DD_XCVR_CLK}	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V ⁴	V _{DDI_x}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V ^{2,4}	V _{DDI_x}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V _{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDI_x} = 3.3 V nominal ^{2,4}	V _{DDAUX_x}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V _{DDI_x} = 2.5 V nominal or lower ^{2,4}	V _{DDAUX_x}	2.375	2.5	2.625	V
Extended commercial temperature range	T _J	0		100	°C
Industrial temperature range	T _J	–40		100	°C
Extended commercial programming temperature range	T _{PRG}	0		100	°C
Industrial programming temperature range	T _{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDI_x} is 2.5 V nominal or 3.3 V nominal, V_{DDAUX_x} must be connected to the V_{DDI_x} supply for that bank. If V_{DDI_x} for a given GPIO bank is <2.5 V nominal, V_{DDAUX_x} per I/O bank must be powered at 2.5 V nominal.
3. XCVR_{VREF} globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near V_{DD_XCVR_CLK}/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDI_x and VDDAUX_x.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	−0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTL	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	−0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	-0.3	0.3 x V _{DDI}	0.7 x V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	-0.3	V _{REF} - 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} Min (V)	V _{OH} Max (V)	I _{OL} ^{2,6} mA	I _{OH} ^{2,6} mA
HSTL135I ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL135II ⁴	1.283	1.35	1.418		0.2 x V _{DDI}	0.8 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSTL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /50	(V _{DDI} – V _{OH}) /50
HSTL12II ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL18I ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /55	(V _{DDI} – V _{OH}) /55
HSUL18II ⁴	1.71	1.8	1.89		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /25	(V _{DDI} – V _{OH}) /25
HSUL12I ⁴	1.14	1.2	1.26		0.1 x V _{DDI}	0.9 x V _{DDI}		V _{OL} /40	(V _{DDI} – V _{OH}) /40
POD12I ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /48	(V _{DDI} – V _{OH}) /48
POD12II ^{4,5}	1.14	1.2	1.26		0.5 x V _{DDI}			V _{OL} /34	(V _{DDI} – V _{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to [UG0686: PolarFire FPGA User I/O User Guide](#) for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 ⁴	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

Table 17 • Complementary Differential DC Output Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{OL} Min (V)	V _{OL} Max (V)	V _{OH} ^{1,3} Min (V)	I _{OL} ² Min (mA)	I _{OH} ² Min (mA)
SSTL25I	2.375	2.5	2.625		V _{TT} – 0.608	V _{TT} + 0.608	8.1	8.1
SSTL25II	2.375	2.5	2.625		V _{TT} – 0.810	V _{TT} + 0.810	16.2	16.2
SSTL18I	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	6.7	6.7
SSTL18II	1.71	1.8	1.89		V _{TT} – 0.603	V _{TT} + 0.603	13.4	13.4
SSTL15I ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL15II ⁴	1.425	1.5	1.575		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
SSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
SSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /34	(V _{DDI} – V _{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	8	8
HSTL15II	1.425	1.5	1.575		0.4	V _{DDI} – 0.4	16	16
HSTL135I ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSTL135II ⁴	1.283	1.35	1.418		0.2 × V _{DDI}	0.8 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSTL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /50	(V _{DDI} – V _{OH})/50
HSUL18I ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /55	(V _{DDI} – V _{OH})/55
HSUL18II ⁴	1.71	1.8	1.89		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /25	(V _{DDI} – V _{OH})/25
HSUL12I ⁴	1.14	1.2	1.26		0.1 × V _{DDI}	0.9 × V _{DDI}	V _{OL} /40	(V _{DDI} – V _{OH})/40
POD12I ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /48	(V _{DDI} – V _{OH})/48
POD12II ^{3,4}	1.14	1.2	1.26		0.5 × V _{DDI}		V _{OL} /34	(V _{DDI} – V _{OH})/34

1. V_{OH} is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
 - a. HSIO lane: 120 mA per 12 IO buffers.
 - b. GPIO lane: 160 mA per 12 IO buffers
3. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).

6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

Min (%)	Typ	Max (%)	Unit	Condition
–40	50	20	Ω	V _{DDI} = 1.8 V/1.5 V/1.35 V/1.2 V
–40	75	20	Ω	V _{DDI} = 1.8 V
–40	150	20	Ω	V _{DDI} = 1.8 V
–20	20	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	30	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	40	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V _{DDI} = 1.5 V/1.35 V
–20	120	20	Ω	V _{DDI} = 1.5 V/1.35 V

Standard	STD	–1	Unit
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMS18 (12 mA)	500	500	Mbps
LVCMS15 (10 mA)	500	500	Mbps
LVCMS12 (8 mA)	300	300	Mbps

1. Performance is achieved with $V_{ID} \geq 200$ mV.

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33	1250	1600	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
HSTL15I	800	900	Mbps
HSTL15II	800	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
PCI	500	500	Mbps
LVTTTL33 (20 mA)	500	500	Mbps
LVCMS33 (20 mA)	500	500	Mbps
LVCMS25 (16 mA)	500	500	Mbps

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit	Clock-to-Data Condition
F _{MAX} 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F _{MAX} 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F _{MAX} 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	μA
Operating current (V_{DD})	RC_{SCVDD}			60.7	μA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F _{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V _{DD} = 1.0 V – STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V – STD	V _{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 48 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	Comment
LVDS25	For DC input levels, see table Differential DC Input and Output Levels .
HCSL25 (for PCIe)	

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

7.4.4 Transceiver Interface Performance

The following table describes the single-ended I/O standards supported as transceiver reference clocks.

Table 49 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	Comment
LVC MOS25	For DC input levels, see table DC Input and Output Levels .

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 50 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		115 ¹		Ω
Power-up termination			>50K		Ω

1. Measured at V_{CM} = 1.2 V and V_{ID} = 350 mV.

Note: All pull-ups are disabled at power-up to allow hot plug capability.

Table 51 • PolarFire Transceiver User Interface Clocks

Parameter	Modes ¹	STD Min	STD Max	-1 Min	-1 Max	Unit
Transceiver TX_CLK range (non- deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		165		160	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1) ¹		130		130	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
	8-bit, max data rate = 1.6 Gbps		200		200	MHz

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{TERM}		85		Ω	
	V_{TERM}		100		Ω	
	V_{TERM}		150		Ω	
Common mode voltage ¹	V_{OCM}	$0.44 \times V_{\text{DDA}}$	$0.525 \times V_{\text{DDA}}$	$0.59 \times V_{\text{DDA}}$	V	DC coupled 50% setting
	V_{OCM}	$0.52 \times V_{\text{DDA}}$	$0.6 \times V_{\text{DDA}}$	$0.66 \times V_{\text{DDA}}$	V	DC coupled 60% setting
	V_{OCM}	$0.61 \times V_{\text{DDA}}$	$0.7 \times V_{\text{DDA}}$	$0.75 \times V_{\text{DDA}}$	V	DC coupled 70% setting
	V_{OCM}	$0.63 \times V_{\text{DDA}}$	$0.8 \times V_{\text{DDA}}$	$0.83 \times V_{\text{DDA}}$	V	DC coupled 80% setting
Rise time ²	T_{TXRF}	41		70	ps	20% to 80%
Fall time ²		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew ³	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew ⁴	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time ⁷	$T_{\text{TxElTrEntry}}$				ns	
Electrical idle transition exit time ⁷	$T_{\text{TxElTrExit}}$				ns	
Electrical idle amplitude	V_{TxElpp}				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time ⁸	T_{DPLLlock}				REFCLK UIs	
Total jitter ^{5,6}	T_{J}				UI	Data rate ≥ 8.5 Gbps to 12.7 Gbps ⁹
Deterministic jitter ^{5,6}	T_{DJ}				UI	(Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter ^{5,6}	T_{J}			0.28	UI	Data rate ≥ 3.2 Gbps to 8.5 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.28	UI	Data rate ≥ 1.6 Gbps to 3.2 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.07	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.13	UI	Data rate ≥ 800 Mbps to 1.6 Gbps
Deterministic jitter ^{5,6}	T_{DJ}			0.02	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter ^{5,6}	T_{J}			0.06	UI	Data rate = 250 Mbps to 800 Mbps
Deterministic jitter ^{5,6}	T_{DJ}			0.01	UI	(Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
		0.41			UI	>3.2–8.5 Gbps ⁵
		0.41			UI	>1.6 to 3.2 Gbps ⁵
		0.41			UI	>0.8 to 1.6 Gbps ⁵
		0.41			UI	250 to 800 Mbps ⁵
Total jitter tolerance with stressed eye	T _{TJOLSE}	0.65			UI	3.125 Gbps ⁵
		0.65			UI	6.25 Gbps ⁶
		0.7			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
Sinusoidal jitter tolerance with stressed eye	T _{SJTOLSE}	0.1			UI	3.125 Gbps ⁵
		0.05			UI	6.25 Gbps ⁶
		0.05			UI	10.3125 Gbps ⁶
					UI	12.7 Gbps ^{6, 10}
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				7.5	dB	

- Valid at 3.2 Gbps and below.
- Data vs. Rx reference clock frequency.
- Achieves compliance with PCIe electrical idle detection.
- Achieves compliance with SATA OOB specification.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
- Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
- For PCIe: Low Threshold Setting = 1, High Threshold Setting = 2.
- For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
- Loss of signal detection is valid for input signals that transition at a density ≥1 Gbps for PRBS7 data or 6 Gbps for PRBS31 data.
- For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describe the PCI express.

Table 54 • PCI Express Gen1

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps		0.25	UI
Receiver jitter tolerance	2.5 Gbps	0.4		UI

Note: With add-in card, as specified in PCI Express CEM Rev 2.0.

7.5.7 CPRI

The following table describes CPRI.

Table 66 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.5.8 JESD204B

The following table describes JESD204B.

Table 67 • JESD204B

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps		0.35	UI
	6.25 Gbps		0.3	UI
	12.5 Gbps ¹			UI
Receive jitter tolerance	3.125 Gbps	0.56		UI
	6.25 Gbps	0.6		UI
	12.5 Gbps ¹			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section [Recommended Operating Conditions \(see page 6\)](#).

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T _i	Programming Cycles, Max	Retention Years	Retention Years at T _i
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41 ¹		s
		MPF300T, TL, TS, TLS	50 ¹	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T _{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS ¹		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

Parameter	Symbol	Typ	Max	Unit
Time from negation of RESPONSE to all I/Os re-enabled	T _{CLR_IO_DISABLE}	28	38	μs
Time from triggering the response to security locked	T _{LOCKDOWN}			ns
Time from negation of RESPONSE to earlier security unlock condition	T _{CLR_LOCKDOWN}			ns
Time from triggering the response to device enters RESET	T _{tr_RESET}	11.7	14	μs
Time from triggering the response to start of zeroization	T _{tr_ZEROLISE}	7.4	8.2	ms

7.8.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

Table 95 • System Controller Suspend Entry and Exit Characteristics

Parameter	Symbol	Definition	Typ	Max	Unit
Time from TRSTb falling edge to SUSPEND_EN signal assertion	T _{suspend_tr} ^{1,2}	Suspend entry time from TRST_N assertion	42	44	ns
Time from TRSTb rising edge to ACTIVE signal assertion	T _{suspend_exit}	Suspend exit time from TRST_N negation	361	372	ns

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

7.8.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

Table 96 • Dynamic Reconfiguration Interface Timing Characteristics

Parameter	Symbol	Max	Unit
PCLK frequency	F _{PD_PCLK}	200	MHz

7.9 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

7.9.1 Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 ¹ , 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384 ¹ , 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256 ¹ (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 ¹	512	2386	1579
	64K	77576	990
SHA-256 ¹	512	2516	884
	64K	84752	938
SHA-384 ¹	1024	4154	884
	64K	100222	938
SHA-512 ¹	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384 ¹	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155