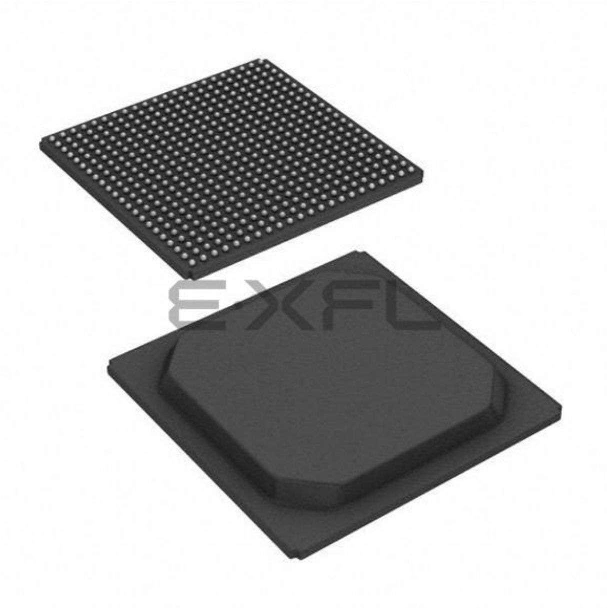

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-fcg484i

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see System Services (see page 59).
- The Non-Volatile Characteristics section was updated. For more information, see Non-Volatile Characteristics (see page 51).
- The Fabric Macros section was updated. For more information, see Fabric Macros (see page 60).
- The Transceiver Switching Characteristics section was updated. For more information, see Transceiver Switching Characteristics (see page 42).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed and HSIO Maximum Output Buffer Speed.
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications.
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics.
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps)[1]	V_{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V_{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V_{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	$V_{DD\_XCVR\_CLK}$	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	$V_{DD\_XCVR\_CLK}$	2.375	2.5	2.625	V
Global V_{REF} for transceiver reference clocks[3]	$XCVR_{VREF}$	Ground		$V_{DD\_XCVR\_CLK}$	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V[4]	V_{DDIx}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V[2,4]	V_{DDIx}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V_{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 3.3 V nominal[2,4]	V_{DDAUXx}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 2.5 V nominal or lower[2,4]	V_{DDAUXx}	2.375	2.5	2.625	V
Extended commercial temperature range	T_J	0		100	°C
Industrial temperature range	T_J	–40		100	°C
Extended commercial programming temperature range	T_{PRG}	0		100	°C
Industrial programming temperature range	T_{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDIx} is 2.5 V nominal or 3.3 V nominal, V_{DDAUXx} must be connected to the V_{DDIx} supply for that bank. If V_{DDIx} for a given GPIO bank is <2.5 V nominal, V_{DDAUXx} per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}$/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section Recommended Operating Conditions (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V_{DD}	0.2	50	ms
Transceiver core supply	V_{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V_{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V_{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V_{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	$V_{DDI[0,1,6,7]}$	0.2	50	ms
GPIO bank I/O power supplies	$V_{DDI[2,4,5]}$	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V_{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	$V_{DDAUX[2,4,5]}$	0.2	50	ms
Transceiver reference clock supply	$V_{DD\_XCVR\_CLK}$	0.2	50	ms
Global V_{REF} for transceiver reference clocks	$XCVR_{VREF}$	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended)[1, 2]	XCVRRX_HS			±4	mA	V_{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended)[3]	XCVRTX_HS			±10	mA	V_{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended)[4]	XCVRREF_HS			±1	mA	$V_{DD\_XCVR\_CLK}$ = 0 V
Current per GPIO pin (P or N single-ended)[5]	I_{GPIO_HS}			±1	mA	V_{DDIx} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

1. Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
2. Each P and N transceiver input has less than the specified maximum input current.
3. Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
4. $V_{DD\_XCVR\_CLK}$ is powered down and the device is driven to –0.3 V < V_{IN} < $V_{DD\_XCVR\_CLK}$.
5. V_{DDIx} is powered down and the device is driven to –0.3 V < V_{IN} < GPIO V_{DDImax}.

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
SSTL135I	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89
HSUL18II	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89
HSUL12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to V_{SS}[4, 5]	Internal parallel termination to V_{SS}	–20	120	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V
		–20	240	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of V_{DDI}.
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F_{MAX} 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F_{MAX} 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F_{MAX} 2:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F_{MAX} 4:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F_{MAX} 8:1	RX_DDRX_B_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F_{MAX} 2:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F_{MAX} 4:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F_{MAX} 8:1	RX_DDRX_BL_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
F_{MAX} 2:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered
F_{MAX} 4:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	370	470	440	500	MHz
		18 × 18 multiplication summed with 48-bit input	370	470	440	500	MHz
		18 × 19 multiplier pre-adder ROM mode	365	465	435	500	MHz
		Two 9 × 9 multiplication	370	470	440	500	MHz
		9 × 9 dot product (DOTP)	370	470	440	500	MHz
		Complex 18 × 19 multiplication	360	455	430	500	MHz

Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	365	465	435	500	MHz
		18 × 18 multiplication summed with 48-bit input	365	465	435	500	MHz
		18 × 19 multiplier pre-adder ROM mode	355	460	430	500	MHz
		Two 9 × 9 multiplication	365	465	435	500	MHz
		9 × 9 DOTP	365	465	435	500	MHz
		Complex 18 × 19 multiplication	350	450	425	500	MHz

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7.3.2 SRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 43 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	343	428	343	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	Mhz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 72 • Initialization Client Sizes

Device	Plaintext	Ciphertext
MPF100T, TL, TS, TLS		
MPF200T, TL, TS, TLS	2916 KB	3006 KB
MPF300T, TL, TS, TLS	4265 KB	4403 KB
MPF500T, TL, TS, TLS		

Note: Worst case initializing all fabric LSRAM, USRAM, and UPROM.

Table 73 • Bitstream Sizes

File	Devices	FPGA	Security	SNVM (all pages)	FPGA+ SNVM	FPGA+ Sec	SNVM+ Sec	FPGA+ SNVM+ Sec
SPI	MPF100T, TL, TS, TLS							
DAT	MPF100T, TL, TS, TLS							
SPI	MPF200T, TL, TS, TLS	5.9 MB	3.4 KB	59.7 KB	5.9 MB	5.9 MB	62.2 KB	6.0 MB
DAT	MPF200T, TL, TS, TLS	5.9 MB	7.3 KB	61.2 KB	6.0 MB	5.9 MB	66.3 KB	6.0 MB
SPI	MPF300T, TL, TS, TLS	9.3 MB	3.5 KB	59.7 KB	9.6 MB	9.5 MB	62.2 KB	9.6 MB
DAT	MPF300T, TL, TS, TLS	9.3 MB	7.6 KB	61.2 KB	9.6 MB	9.5 MB	66.3 KB	9.6 MB
SPI	MPF500T, TL, TS, TLS							
DAT	MPF500T, TL, TS, TLS							

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 74 • Maximum Number of Digest Cycles

		Retention Since Programmed (N = Number Digests During that Time)[1]								
Digest T_J	Storage and Operating T_J	N ≤300	N = 500	N = 1000	N = 1500	N = 2000	N = 4000	N = 6000	Unit	Retention
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T_J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

7.6.5 Digest Time

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		µs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	35	µs
	MPF300T, TL, TS, TLS	33.2	35	µs
	MPF500T, TL, TS, TLS			µs
sNVM digest run time[1]	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	46.6	48.8	µs
	MPF300T, TL, TS, TLS	46.6	48.8	µs
	MPF500T, TL, TS, TLS			µs
User key digest run time[2]	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	525.4	543.3	µs
	MPF300T, TL, TS, TLS	525.4	543.3	µs
	MPF500T, TL, TS, TLS			µs

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	34.9	µs
	MPF300T, TL, TS, TLS	33.2	34.9	µs
	MPF500T, TL, TS, TLS			µs
Factory digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	493.6	510.1	µs
	MPF300T, TL, TS, TLS	493.6	510.1	µs
	MPF500T, TL, TS, TLS			µs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	µs	
Authenticated and decrypted text read		159.59	160.53	166.5	µs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

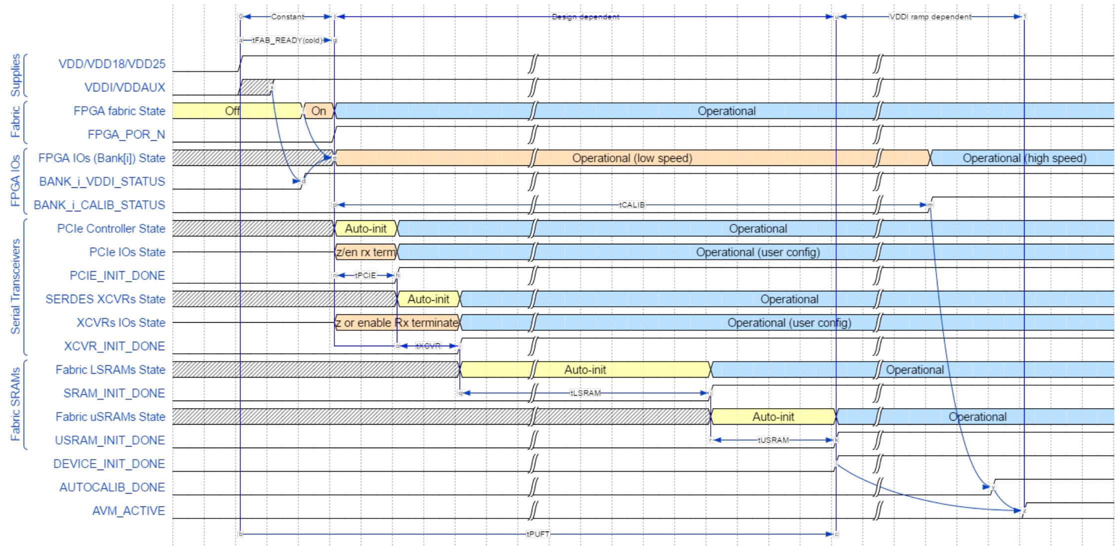
7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	µs	
User code	T_{User}	01H	0.8	1.05	µs	
Design information	T_{Design}	02H	2.4	2.7	µs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	µs	
Query security locks	T_{sec_Query}	05H	15	17	µs	
Read debug information	T_{Rd_debug}	06H	34	38	µs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM\_Wr\_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM\_Wr\_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM\_Wr\_Cipher}$	12H				Note 1
Reserved		13H–17H				

Figure 5 • Cold Reset Timing



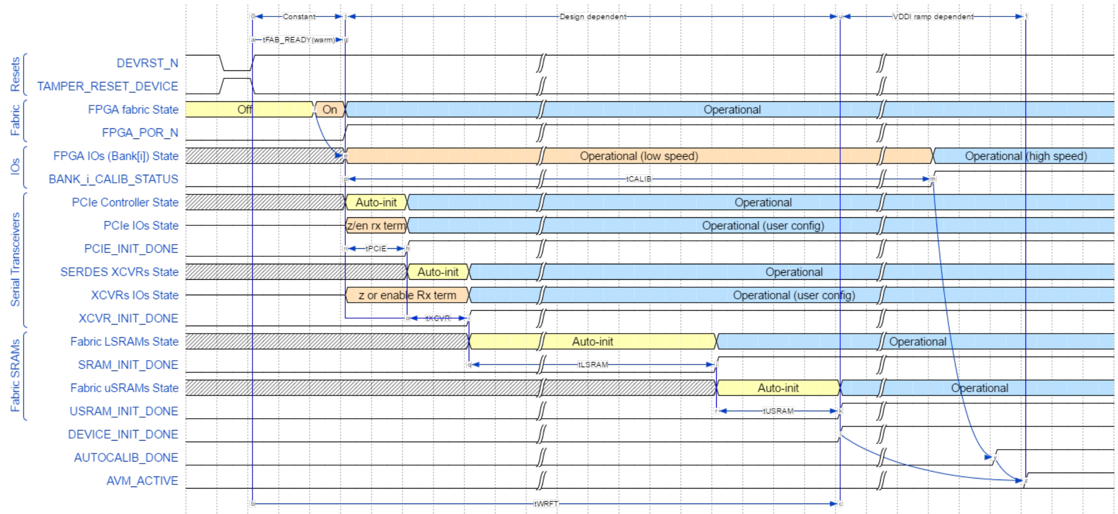
Notes:

- The previous diagram showsthe case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
  - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
  - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
  - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2 Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

Figure 6 • Warm Reset Timing



7.9.3 Power-On Reset Voltages

7.9.3.1 Main Supplies

The start of power-up to functional time (T_{PUFT}) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

Table 97 • POR Ref Voltages

Supply	Power-On Reset Start Point (V)	Note
VDD	0.95	Applies to both 1.0 V and 1.05 V operation.
VDD18	1.71	
VDD25	2.25	

7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

Table 98 • I/O-Related Supplies

Supply	I/O Power-Up Start Point (V)
VDDI	0.85
VDDAUX	1.6

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

7.9.4 Design Dependence of T PUFT and T WRFT

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note T_{PCIE} , T_{XCVR}, T_{LSRAM}, and T_{USRAM} can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$$T_{PUFT} = T_{FAB\_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

$$T_{WRFT} = T_{FAB\_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

Note: T_{PCIE}, T_{XCVR}, T_{LSRAM}, T_{USRAM}, and T_{CALIB} are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond T_{PUFT} (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

7.9.5 Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 99 • Cold Boot

Power-On (Cold) Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when weak pull-ups are enabled – $T_{PU\_PD\_ACTIVE(cold)}$	1.17	4.51	7.84	ms
Time when fabric is operational – $T_{FAB\_READY(cold)}$	1.20	4.54	7.87	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(cold)}$	1.22	4.56	7.89	ms

7.9.6 Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

Table 100 • Warm Boot

Warm Reset to Fabric and I/O Operational	Min	Typ	Max	Unit
Time when input pins start working – $T_{IN\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when weak pull-ups/pull-downs are enabled – $T_{PU\_PD\_ACTIVE(warm)}$	0.91	1.76	2.62	ms
Time when fabric is operational – $T_{FAB\_READY(warm)}$	0.94	1.79	2.65	ms
Time when output pins start driving – $T_{OUT\_ACTIVE(warm)}$	0.96	1.81	2.67	ms

7.9.7 Miscellaneous Initialization Parameters

In the following table, T_{FAB_READY} refers to either $T_{FAB\_READY(cold)}$ or $T_{FAB\_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F_{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T_{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T_{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR_{RAMP}		10		µs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR_{ASSERT}	1			µs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	$DR_{DEASSERT}$	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF_{RAMP}		10		µs	
Minimum FF_EXIT_N assert time	FF_{ASSERT}	1			µs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	$FF_{DEASSERT}$	170			µs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

7.11 User Crypto

The following section describes user crypto.

7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 112 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V – 1	VDD = 1.05 V STD	VDD = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	189		189		MHz	–40 °C to 100 °C

7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Throughput cycle count collected with Athena TeraFire Core and RISCV running at 100 MHz.

Table 113 • AES

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-ECB-128 encrypt[1]	128	515	1095
	64K	50157	933
AES-ECB-128 decrypt[1]	128	557	1760
	64K	48385	1524
AES-ECB-256 encrypt[1]	128	531	1203
	64K	58349	1203
AES-ECB-256 decrypt[1]	128	589	1676
	64K	56673	1671
AES-CBC-256 encrypt[1]	128	576	1169
	64K	52547	1169
AES-CBC-256 decrypt[1]	128	585	1744
	64K	48565	1652
AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1925	2740
	64K	60070	2158
AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1973	2268
	64K	60102	2151

1. With DPA counter measures.

Table 114 • GMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-GCM-256[1], 128-bit tag, (message is only authenticated)	128	1863	2211
	64K	49707	2128

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