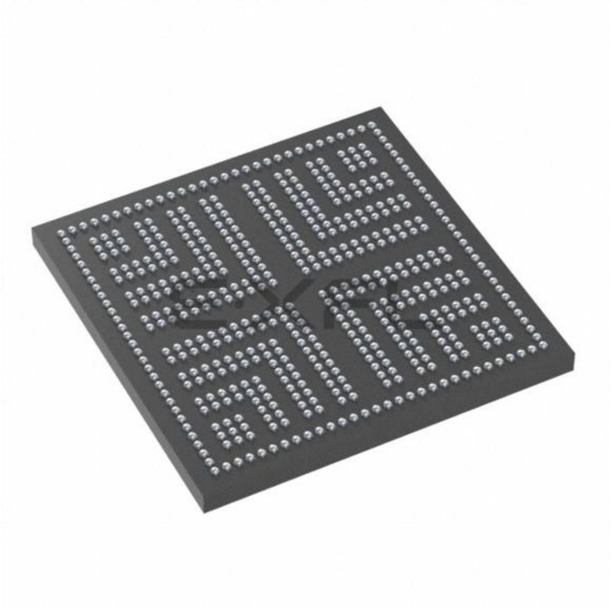
Microchip Technology - MPF300T-FCSG536E Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300t-fcsg536e

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps)[1]	V_{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply	V_{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V_{DDA25}	2.425	2.50	2.575	V
Transceiver reference clock supply –3.3 V nominal	$V_{DD\_XCVR\_CLK}$	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	$V_{DD\_XCVR\_CLK}$	2.375	2.5	2.625	V
Global V_{REF} for transceiver reference clocks[3]	$XCVR_{VREF}$	Ground		$V_{DD\_XCVR\_CLK}$	V
HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V[4]	V_{DDIx}	1.14	Various	1.89	V
GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V[2,4]	V_{DDIx}	1.14	Various	3.465	V
Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V	V_{DDI3}	1.71	Various	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 3.3 V nominal[2,4]	V_{DDAUXx}	3.135	3.3	3.465	V
GPIO auxiliary supply for I/O bank x with V_{DDIx} = 2.5 V nominal or lower[2,4]	V_{DDAUXx}	2.375	2.5	2.625	V
Extended commercial temperature range	T_J	0		100	°C
Industrial temperature range	T_J	–40		100	°C
Extended commercial programming temperature range	T_{PRG}	0		100	°C
Industrial programming temperature range	T_{PRG}	–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if V_{DDIx} is 2.5 V nominal or 3.3 V nominal, V_{DDAUXx} must be connected to the V_{DDIx} supply for that bank. If V_{DDIx} for a given GPIO bank is <2.5 V nominal, V_{DDAUXx} per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}/2$ V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
SSTL135I	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89
HSUL18II	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89
HSUL12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
MLVDSE25[3]	GPIO		1.25		0.396	0.442	0.453
LVPECLE33[3]	GPIO		1.65		0.664	0.722	0.755
MIPIE25[3]	GPIO		0.25		0.1	0.22	0.3

1. V_{OCM} is the output common mode voltage.
2. V_{OD} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
    a. V_{ICM} must be less than V_{DDI} -0.4V;
    b. $V_{ICM} + V_{ID}/2$ must be $< V_{DDI} + 0.4$ V;
    c. $V_{ICM} – V_{ID}/2$ must be $> VSS – 0.3$ V.

Table 17 • Complementary Differential DC Output Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{OL} Min (V)	V_{OL} Max (V)	V_{OH}[1,3] Min (V)	I_{OL}[2] Min (mA)	I_{OH}[2] Min (mA)
SSTL25I	2.375	2.5	2.625		V_{TT} – 0.608	V_{TT} + 0.608	8.1	8.1
SSTL25II	2.375	2.5	2.625		V_{TT} – 0.810	V_{TT} + 0.810	16.2	16.2
SSTL18I	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603	6.7	6.7
SSTL18II	1.71	1.8	1.89		V_{TT} – 0.603	V_{TT} + 0.603	13.4	13.4
SSTL15I[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40
SSTL15II[4]	1.425	1.5	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/34	(V_{DDI} – V_{OH})/34
SSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40
SSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/34	(V_{DDI} – V_{OH})/34
HSTL15I	1.425	1.5	1.575		0.4	V_{DDI} – 0.4	8	8
HSTL15II	1.425	1.5	1.575		0.4	V_{DDI} – 0.4	16	16
HSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/50	(V_{DDI} – V_{OH})/50
HSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/25	(V_{DDI} – V_{OH})/25
HSTL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/50	(V_{DDI} – V_{OH})/50
HSUL18I[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/55	(V_{DDI} – V_{OH})/55
HSUL18II[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/25	(V_{DDI} – V_{OH})/25
HSUL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40
POD12I[3,4]	1.14	1.2	1.26		0.5 × V_{DDI}		V_{OL}/48	(V_{DDI} – V_{OH})/48
POD12II[3,4]	1.14	1.2	1.26		0.5 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH})/34

1. V_{OH} is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers
3. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).

6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

Min (%)	Typ	Max (%)	Unit	Condition
–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V/1.35 V/1.2 V
–40	75	20	Ω	V_{DDI} = 1.8 V
–40	150	20	Ω	V_{DDI} = 1.8 V
–20	20	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	30	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	40	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	120	20	Ω	V_{DDI} = 1.5 V/1.35 V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSTL135II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
MIPI25	Mobile Industry Processor Interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 27).
6. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	
SSTL25I	Stub-series terminated logic 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

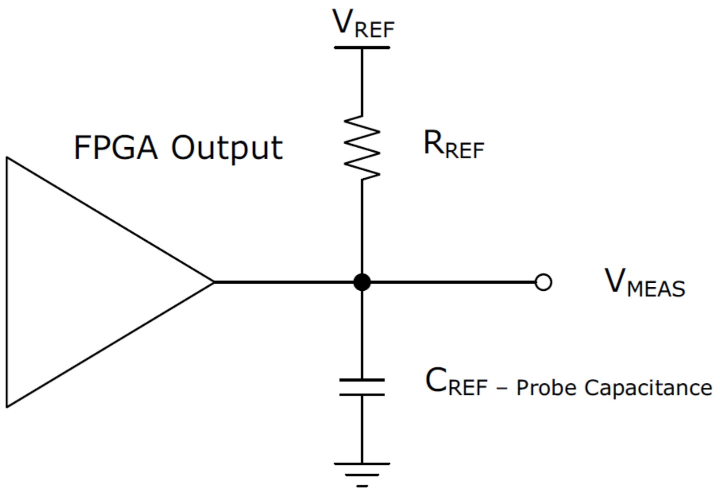
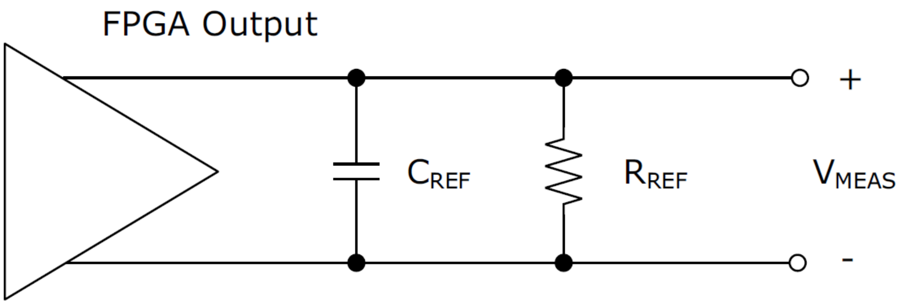


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

Standard	STD	–1	Unit
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with V_{ID} ≥200 mV.

7.1.4 Output Buffer Speed

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 8:1	RX_DDRX_BL_C	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_SDR_G_A	Tx SDR							MHz	From a global clock source, aligned[1]
	TX_SDR_G_C	Tx SDR							MHz	From a global clock source, centered[1]

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output FMAX	TX_DDR_G_A	Tx DDR			335			335	MHz	From a global clock source, aligned
	TX_DDR_G_C	Tx DDR			335			335	MHz	From a global clock source, centered
	TX_DDR_L_A	Tx DDR			250			250	MHz	From a lane clock source, aligned
	TX_DDR_L_C	Tx DDR			250			250	MHz	From a lane clock source, centered
Output FMAX 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned
Output FMAX 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned

Table 44 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 45 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V – STD	V_{DD} = 1.0 V – 1	V_{DD} = 1.05 V – STD	V_{DD} = 1.05 V – 1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1,2]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled[2]	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[3]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode[2]	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode [2]	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2, 3]	FXCVRREFCLKMAX CASCADE	20		156	20		156	MHz
Reference clock rate at the PFD[4]	FTXREFCLKPFD	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4]	FTXREFCLKPFD10G	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5]	FTXREFPN			–110			–110	dBc /Hz
Phase noise at 10 KHz	FTXREFPN			–110			–110	dBc /Hz
Phase noise at 100 KHz	FTXREFPN			–115			–115	dBc /Hz
Phase noise at 1 MHz	FTXREFPN			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	TREFRISE		200	500		200	500	ps
Reference clock input fall time (90%–10%)	TREFFALL		200	500		200	500	ps
Reference clock duty cycle	TREFDUTY	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual FTxRefClkPFD value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps[1]			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps[1]			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

Table 60 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4 1GbE (1000BASE-T)

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5 SGMII and QSGMII

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6 SDI

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T_J	Programming Cycles, Max	Retention Years	Retention Years at T_J
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41[1]		s
		MPF300T, TL, TS, TLS	50[1]	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS[1]		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	µs	
Authenticated and decrypted text read		159.59	160.53	166.5	µs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

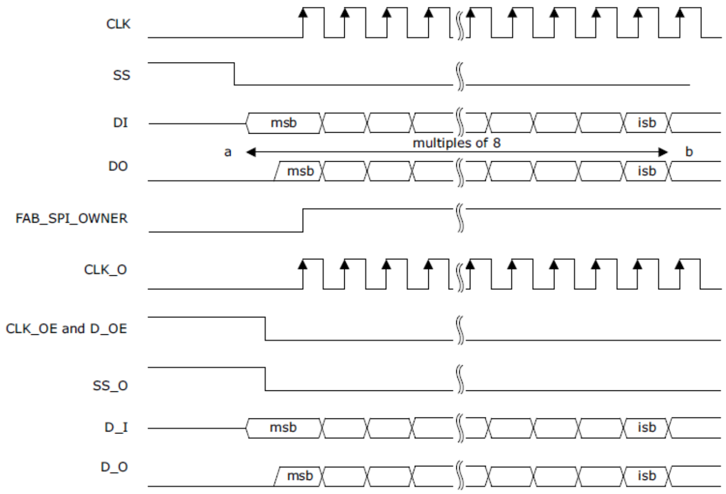
7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	µs	
User code	T_{User}	01H	0.8	1.05	µs	
Design information	T_{Design}	02H	2.4	2.7	µs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	µs	
Query security locks	T_{sec_Query}	05H	15	17	µs	
Read debug information	T_{Rd_debug}	06H	34	38	µs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM\_Wr\_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM\_Wr\_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM\_Wr\_Cipher}$	12H				Note 1
Reserved		13H–17H				

Figure 4 • USPI Switching Characteristics



7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ[1]	Max
T_{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 µs		470 µs
T_{CONVN}	Time between subsequent channel conversions.		480 µs	
T_{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs.	0 ns		
T_{VALID}[2]	Width of the valid pulse.	1.625 µs		2 µs
T_{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 µs	Rate × 32 µs	8128 µs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4’b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	–40		125	°C	
Temperature sensing accuracy	–10		10	°C	

Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T_{FAB_READY} to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T_{FAB_READY} to auto-update start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to programming recovery start			T_{PUF_OVHD}[1]	T_{PUF_OVHD}[1]	ms	
The time from T_{FAB_READY} to the tamper flags being available	T_{TAMPER_READY}	0	0	0	ms	
The time from T_{FAB_READY} to the Athena Crypto co-processor being available (for S devices only)	T_{CRYPTO_READY}	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to T_{PUF_OVHD} at section Secure NVM Performance (see page 58).

7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in I/O-Related Supplies (see page 66).

Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

Note: In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash*Freeze Mode and to exit Flash*Freeze mode.

ECDSA SigVer, P-384/SHA-384	1024	6421841	5759
	8K	6273510	5759
Key Agreement (KAS), P-384		5039125	6514
Point Multiply, P-256[1]		5176923	4482
Point Multiply, P-384[1]		12043199	5319
Point Multiply, P-521[1]		26887187	6698
Point Addition, P-384		3018067	5779
KeyGen (PKG), P-384		12055368	6908
Point Verification, P-384		5091	3049

1. With DPA counter measures.

Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048[1], CRT	2048	26862392	15900
Decrypt, RSA-3072[1], CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384[1] ,CRT, PKCS #1 V 1 1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	148090970	14642
	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	970991	12000
	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	443493	8436
	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	973269	11313
	8K	983255	11146

1. With DPA counter measures.

Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SigGen, DSA-3072/SHA-384[1]	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133

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