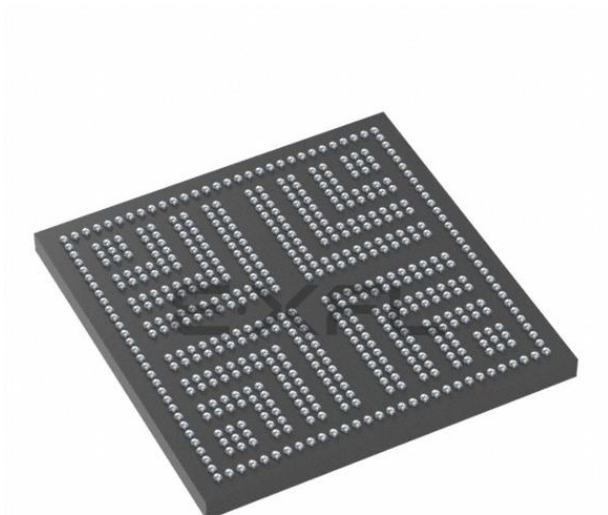




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300tl-fcsg536e

7.3.2	SRAM Blocks	41
7.4	Transceiver Switching Characteristics	42
7.4.1	Transceiver Performance	42
7.4.2	Transceiver Reference Clock Performance	42
7.4.3	Transceiver Reference Clock I/O Standards	43
7.4.4	Transceiver Interface Performance	44
7.4.5	Transmitter Performance	44
7.4.6	Receiver Performance	47
7.5	Transceiver Protocol Characteristics	48
7.5.1	PCI Express	48
7.5.2	Interlaken	49
7.5.3	10GbE (10GBASE-R, and 10GBASE-KR)	49
7.5.4	1GbE (1000BASE-T)	50
7.5.5	SGMII and QSGMII	50
7.5.6	SDI	50
7.5.7	CPRI	51
7.5.8	JESD204B	51
7.6	Non-Volatile Characteristics	51
7.6.1	FPGA Programming Cycle and Retention	52
7.6.2	FPGA Programming Time	52
7.6.3	FPGA Bitstream Sizes	53
7.6.4	Digest Cycles	53
7.6.5	Digest Time	54
7.6.6	Zeroization Time	55
7.6.7	Verify Time	57
7.6.8	Authentication Time	58
7.6.9	Secure NVM Performance	58
7.6.10	Secure NVM Programming Cycles	59
7.7	System Services	59
7.7.1	System Services Throughput Characteristics	59
7.8	Fabric Macros	60
7.8.1	UJTAG Switching Characteristics	60
7.8.2	UJTAG_SEC Switching Characteristics	61
7.8.3	USPI Switching Characteristics	62
7.8.4	Tamper Detectors	62
7.8.5	System Controller Suspend Switching Characteristics	64
7.8.6	Dynamic Reconfiguration Interface	64
7.9	Power-Up to Functional Timing	64
7.9.1	Power-On (Cold) Reset Initialization Sequence	64
7.9.2	Warm Reset Initialization Sequence	65
7.9.3	Power-On Reset Voltages	66

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see [System Services \(see page 59\)](#).
- The Non-Volatile Characteristics section was updated. For more information, see [Non-Volatile Characteristics \(see page 51\)](#).
- The Fabric Macros section was updated. For more information, see [Fabric Macros \(see page 60\)](#).
- The Transceiver Switching Characteristics section was updated. For more information, see [Transceiver Switching Characteristics \(see page 42\)](#).

1.2 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

1.3 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see [HSIO Maximum Input Buffer Speed](#) and [HSIO Maximum Output Buffer Speed](#).
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see [I/O Standards Specifications](#).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see [Non-Volatile Characteristics](#).
- A note was added defining power down conditions for programming recovery conditions. For more information, see [Power-Supply Ramp Times](#).

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the [PolarFire Power Estimator Spreadsheet](#).

- [PO0137](#): PolarFire FPGA Product Overview
- [ER0217](#): PolarFire FPGA Pre-Production Device Errata
- [UG0722](#): PolarFire FPGA Packaging and Pin Descriptions Users Guide
- [UG0726](#): PolarFire FPGA Board Design User Guide
- [UG0686](#): PolarFire FPGA User I/O User Guide
- [UG0680](#): PolarFire FPGA Fabric User Guide
- [UG0714](#): PolarFire FPGA Programming User Guide
- [UG0684](#): PolarFire FPGA Clocking Resources User Guide
- [UG0687](#): PolarFire FPGA 1G Ethernet Solutions User Guide
- [UG0727](#): PolarFire FPGA 10G Ethernet Solutions User Guide
- [UG0748](#): PolarFire FPGA Low Power User Guide
- [UG0676](#): PolarFire FPGA DDR Memory Controller User Guide
- [UG0743](#): PolarFire FPGA Debugging User Guide
- [UG0725](#): PolarFire FPGA Device Power-Up and Resets User Guide
- [UG0677](#): PolarFire FPGA Transceiver User Guide
- [UG0685](#): PolarFire FPGA PCI Express User Guide
- [UG0753](#): PolarFire FPGA Security User Guide
- [UG0752](#): PolarFire FPGA Power Estimator User Guide

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance ¹	C _{IN} (dedicated GPIO)		5.6	pf	
	C _{IN} (GPIO)		5.6	pf	
	C _{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I _L (GPIO)		10	μA	I/O disabled, high – Z
	I _L (HSIO)		10	μA	I/O disabled, high – Z
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}	T _{RISE}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input rise time (10%–90% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}	T _{FALL}	0.66	2.64	ns	V _{DDIX} = 3.3 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.50	2.00	ns	V _{DDIX} = 2.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.36	1.44	ns	V _{DDIX} = 1.8 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.30	1.20	ns	V _{DDIX} = 1.5 V
Input fall time (90%–10% of V _{DDIX}) ^{2, 3, 4}		0.24	0.96	ns	V _{DDIX} = 1.2 V
Pad pull-up when V _{IN} = 0 ⁵	I _{PU}	137	220	μA	V _{DDIX} = 3.3 V
Pad pull-up when V _{IN} = 0 ⁵		102	166	μA	V _{DDIX} = 2.5 V
Pad pull-up when V _{IN} = 0		68	115	μA	V _{DDIX} = 1.8 V
Pad pull-up when V _{IN} = 0		51	88	μA	V _{DDIX} = 1.5 V
Pad pull-up when V _{IN} = 0 ⁶		29	73	μA	V _{DDIX} = 1.35 V
Pad pull-up when V _{IN} = 0	I _{PD}	16	46	μA	V _{DDIX} = 1.2 V
Pad pull-down when V _{IN} = 3.3 V ⁵		65	187	μA	V _{DDIX} = 3.3 V
Pad pull-down when V _{IN} = 2.5 V ⁵		63	160	μA	V _{DDIX} = 2.5 V
Pad pull-down when V _{IN} = 1.8 V		60	117	μA	V _{DDIX} = 1.8 V
Pad pull-down when V _{IN} = 1.5 V		57	95	μA	V _{DDIX} = 1.5 V
Pad pull-down when V _{IN} = 1.35 V		52	86	μA	V _{DDIX} = 1.35 V
Pad pull-down when V _{IN} = 1.2 V		47	79	μA	V _{DDIX} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
PCI	3.15	3.3	3.45	−0.3	0.3 x V _{DDI}	0.5 x V _{DDI}	3.45
LVTTL	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS33	3.15	3.3	3.45	−0.3	0.8	2	3.45
LVC MOS25	2.375	2.5	2.625	−0.3	0.7	1.7	2.625
LVC MOS18	1.71	1.8	1.89	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.89
LVC MOS15	1.425	1.5	1.575	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.575
LVC MOS12	1.14	1.2	1.26	−0.3	0.35 x V _{DDI}	0.65 x V _{DDI}	1.26
SSTL25I ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL25II ²	2.375	2.5	2.625	−0.3	V _{REF} − 0.15	V _{REF} + 0.15	2.625
SSTL18I ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL18II ²	1.71	1.8	1.89	−0.3	V _{REF} − 0.125	V _{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575

I/O Standard	V _{DDI} Min (V)	V _{DDI} Typ (V)	V _{DDI} Max (V)	V _{IL} Min (V)	V _{IL} Max (V)	V _{IH} Min (V)	V _{IH} ¹ Max (V)
SSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
SSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL15I	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL15II	1.425	1.5	1.575	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.575
HSTL135I	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL135II	1.283	1.35	1.418	−0.3	V _{REF} − 0.09	V _{REF} + 0.09	1.418
HSTL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSTL12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
HSUL18I	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL18II	1.71	1.8	1.89	−0.3	0.3 × V _{DDI}	0.7 × V _{DDI}	1.89
HSUL12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.1	V _{REF} + 0.1	1.26
POD12I	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26
POD12II	1.14	1.2	1.26	−0.3	V _{REF} − 0.08	V _{REF} + 0.08	1.26

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.

2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V _{ICM} ^{1,3} Min (V)	V _{ICM} ^{1,3} Typ (V)	V _{ICM} ^{1,3} Max (V)	V _{ID} ² Min (V)	V _{ID} Typ (V)	V _{ID} Max (V)
LVDS18	HSIO	Low	0.05	0.4	0.8	0.1	0.35	0.6
		Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS18	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LCMDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
RSDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
RSDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
MINILVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
MINILVDS18 ⁵	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.3	0.6
		Low	0.05	0.4	0.8	0.1	0.3	0.6
SUBLVDS33	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS25	GPIO	Mid (default)	0.6	0.9	2.35	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
SUBLVDS18 ⁵	HSIO	Mid (default)	0.6	0.9	1.65	0.1	0.15	0.3
		Low	0.05	0.4	0.8	0.1	0.15	0.3
PPDS33	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS25	GPIO	Mid (default)	0.6	0.8	2.35	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
PPDS18 ⁵	HSIO	Mid (default)	0.6	0.8	1.65	0.1	0.2	0.6
		Low	0.05	0.4	0.8	0.1	0.2	0.6
SLVS33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS25 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.2	0.3
		Low	0.05	0.2	0.8	0.1	0.2	0.3
SLVS18 ⁵	HSIO	Mid (default)	0.6	1.00	1.65	0.1	0.2	0.3
		Low	0.05	0.4	0.8	0.1	0.2	0.3
HCSL33 ⁶	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3 ¹	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3 ¹	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3 ¹	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2 ¹	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2 ¹	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2 ¹	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V _{DDAUX}	V _{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2 ¹	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2 ¹	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
Regional clock duty cycle distortion	T _{DCDR}	120	120	120	120	ps	At 250 MHz

The following table provides clocking specifications from –40 °C to 100 °C.

Table 36 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V –1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F _{MAX}	F _{MAXB}	1000	1250	1000	1250	MHz	HSIO and GPIO
High-speed I/O clock skew ¹	F _{SKEWB}	30	20	30	20	ps	HSIO without bridging
	F _{SKEWB}	600	500	600	500	ps	HSIO with bridging
	F _{SKEWB}	45	35	45	35	ps	GPIO without bridging
	F _{SKEWB}	75	60	75	60	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion ²	T _{DCB}	90	90	90	90	ps	HSIO without bridging
	T _{DCB}	115	115	115	115	ps	HSIO with bridging
	T _{DCB}	90	90	90	90	ps	GPIO without bridging
	T _{DCB}	115	115	115	115	ps	GPIO with bridging

1. F_{SKEWB} is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

7.2.2

PLL

The following table provides information about PLL.

Table 37 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F _{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F _{INF}	10		1250	MHz
Minimum reference or feedback pulse width ¹	F _{INPULSE}	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F _{PHDET1}	1		312	MHz
Frequency at the PFD (fractional mode)	F _{PHDET2}	10	50	125	MHz
Allowable input duty cycle	F _{INDUTY}	25		75	%

Parameter	Symbol	Min	Typ	Max	Unit
Operating current (V_{DD18})	RC_{SCVPP}			0.1	μA
Operating current (V_{DD})	RC_{SCVDD}			60.7	μA

Table 44 • μ SRAM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	T_{ac}		2		2	ns	Read-port

Table 45 • μ PROM Performance

Parameter	Symbol	$V_{DD} = 1.0\text{ V} - \text{STD}$	$V_{DD} = 1.0\text{ V} - 1$	$V_{DD} = 1.05\text{ V} - \text{STD}$	$V_{DD} = 1.05\text{ V} - 1$	Unit
Read access time	T_{ac}	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 46 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Tx data rate ^{1,2}	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled ²	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency ³	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz
Rx CDR mode	F_{RXCDR}	0.25		10.3125	0.25		10.3125	Gbps
Rx DFE mode ²	F_{RXDFE}	3.0		10.3125	3.0		12.7	Gbps
Rx Eye Monitor mode ²	$F_{RXEyeMon}$	3.0		10.3125	3.0		12.7	Gbps

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 47 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	-1 Min	-1 Typ	-1 Max	Unit
Reference clock input rate ^{1,2}	$F_{TXREFCLK}$	20		800	20		800	MHz

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate ^{1, 2, 3}	F _{XCVRREFCLKMAX} CASCADE	20		156	20		156	MHz
Reference clock rate at the PFD ⁴	F _{TXREFCLKPFD}	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above ⁴	F _{TXREFCLKPFD10G}	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input) ⁵	F _{TXREFPN}			–110			–110	dBc /Hz
Phase noise at 10 KHz	F _{TXREFPN}			–110			–110	dBc /Hz
Phase noise at 100 KHz	F _{TXREFPN}			–115			–115	dBc /Hz
Phase noise at 1 MHz	F _{TXREFPN}			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	T _{REFRISE}		200	500		200	500	ps
Reference clock input fall time (90%–10%)	T _{REFFALL}		200	500		200	500	ps
Reference clock duty cycle	T _{REFDUTY}	40		60	40		60	%
Spread spectrum modulation spread ⁶	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency ⁷	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual F_{TxRefClkPFD} value by $20 \times \log_{10} (\text{TxRefClkPFD} / 156 \text{ MHz})$. It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
FTxRefClk = 75 MHz with typical settings.
For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section [Recommended Operating Conditions](#) (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		$V_{DDA} + 0.3$	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC}^1	$0.7 \times V_{DDA}$		$0.9 \times V_{DDA}$	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance ²	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high) ⁹	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low) ⁹	$V_{DETLLOW}$	65		175	mV	Setting = PCIe ^{3,7}
	$V_{DETLLOW}$	95		190	mV	Setting = SATA ^{4,8}
	$V_{DETLLOW}$	75		170	mV	Setting = 1
	$V_{DETLLOW}$	95		185	mV	Setting = 2
	$V_{DETLLOW}$	100		190	mV	Setting = 3
	$V_{DETLLOW}$	140		210	mV	Setting = 4
	$V_{DETLLOW}$	155		240	mV	Setting = 5
	$V_{DETLLOW}$	165		245	mV	Setting = 6
	$V_{DETLLOW}$	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJITOL}				UI	>8.5 Gbps – 12.7 Gbps ^{5, 10}

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T _J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is $20 \times LF = 20 \times .8 = 16$ years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is $10 \times LF$ or 10 years over the industrial temperature range.

7.6.5**Digest Time**

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		μs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	33.2	35	μs
	MPF300T, TL, TS, TLS	33.2	35	μs
	MPF500T, TL, TS, TLS			μs
sNVM digest run time ¹	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	46.6	48.8	μs
	MPF300T, TL, TS, TLS	46.6	48.8	μs
	MPF500T, TL, TS, TLS			μs
User key digest run time ²	MPF100T, TL, TS, TLS			μs
	MPF200T, TL, TS, TLS	525.4	543.3	μs
	MPF300T, TL, TS, TLS	525.4	543.3	μs
	MPF500T, TL, TS, TLS			μs

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF500T, TL, TS, TLS						

Notes:

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Table 83 • Verify System Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
In application verify by index	T _{IAP_Ver_Index}	44H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s
In application verify by SPI address	T _{IAP_Ver_Addr}	45H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	8.2	9	s
			MPF300T, TL, TS, TLS	12.4	13	s
			MPF500T, TL, TS, TLS			s

7.6.8 Authentication Time

The following tables describe authentication system service time.

Table 84 • Authentication Services

Parameter	Symbol	ServiceID	Devices	Typ	Max	Unit
Bitstream Authentication	T _{BIT_AUTH}	22H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s
IAP Image Authentication	T _{IAP_AUTH}	23H	MPF100T, TL, TS, TLS			s
			MPF200T, TL, TS, TLS	3.3	3.7	s
			MPF300T, TL, TS, TLS	4.9	5.4	s
			MPF500T, TL, TS, TLS			s

7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

Table 85 • sNVM Read/Write Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Plain text programming		7.0	7.2	7.9	ms	
Authenticated text programming		7.2	7.4	9.4	ms	
Authenticated and encrypted text programming		7.2	7.4	9.4	ms	
Authentication R/W 1st access from power-up overhead	T _{PUF_OVHD}		100	111	ms	From T _{FAB_READY}
Plain text read		7.67	7.79	8.2	μs	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Authenticated text read		113.25	114.02	118.5	μs	
Authenticated and decrypted text read		159.59	160.53	166.5	μs	

Notes:

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- T_{PUF_OVHD} is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 86 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles per Page, Max	Programming Cycles per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 bytes. Block size = 56 KBytes.

7.7 System Services

This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 87 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Serial number	T_{Serial}	00H	65	67	μs	
User code	T_{User}	01H	0.8	1.05	μs	
Design information	T_{Design}	02H	2.4	2.7	μs	
Device certificate	T_{Cert}	03H	255	271	ms	
Read digests	T_{digest_read}	04H	201	215	μs	
Query security locks	T_{sec_Query}	05H	15	17	μs	
Read debug information	T_{Rd_debug}	06H	34	38	μs	
Reserved		07H–0FH				
Secure NVM write plain text	$T_{SNVM_Wr_Plain}$	10H				Note 1
Secure NVM write authenticated plain text	$T_{SNVM_Wr_Auth}$	11H				Note 1
Secure NVM write authenticated cipher text	$T_{SNVM_Wr_Cipher}$	12H				Note 1
Reserved		13H–17H				

Table 101 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T _{FAB_READY} to ready to program through JTAG/SPI-Slave		0	0	0	ms	
The time from T _{FAB_READY} to auto-update start			T _{PUF_OVHD} ¹	T _{PUF_OVHD} ¹	ms	
The time from T _{FAB_READY} to programming recovery start			T _{PUF_OVHD} ¹	T _{PUF_OVHD} ¹	ms	
The time from T _{FAB_READY} to the tamper flags being available	T _{TAMPER_READY}	0	0	0	ms	
The time from T _{FAB_READY} to the Athena Crypto co-processor being available (for S devices only)	T _{CRYPTO_READY}	0	0	0	ms	

1. Programming depends on the PUF to power up. Refer to T_{PUF_OVHD} at section [Secure NVM Performance](#) (see page 58).

7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

Table 102 • I/O Initial Calibration Time (TCALIB)

Ramp Time	Min (ms)	Max (ms)	Condition
0.2 ms	0.98	2.63	Applies to HSIO and GPIO banks
50 ms	41.62	62.19	Applies to HSIO and GPIO banks

Notes:

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in [I/O-Related Supplies](#) (see page 66).

Table 103 • I/O Fast Recalibration Time (TRECALIB)

I/O Type	Min (ms)	Typ (ms)	Max (ms)	Condition
GPIO bank	0.16	0.20	0.24	GPIO configured for 3.3 V operation
HSIO bank	0.20	0.25	0.30	HSIO configured for 1.8 V operation

Note: In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

The following table describes the time to enter Flash*Freeze Mode and to exit Flash*Freeze mode.

Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{MSCK}			40	MHz	

Table 108 • SPI Slave Mode (PolarFire Slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F _{SSCK}			80	MHz	

7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 109 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V _{DD} = 1.0 V STD	V _{DD} = 1.0 V – 1	V _{DD} = 1.05 V STD	V _{DD} = 1.05 V – 1	Unit
Maximum frequency of probe signal	F _{MAX}	100	100	100	100	MHz
Minimum delay of probe signal	T _{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T _{Max_delay}	13	12	13	12	ns

7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 110 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR _{RAMP}		10		μs	It must be a normal clean digital signal, with typical rise and fall times
DEVRST_N assert time	DR _{ASSERT}	1			μs	The minimum time for DEVRST_N assertion to be recognized
DEVRST_N de-assert time	DR _{DEASSERT}	2.75			ms	The minimum time DEVRST_N needs to be de-asserted before assertion

7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 111 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF _{RAMP}		10		μs	
Minimum FF_EXIT_N assert time	FF _{ASSERT}	1			μs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	FF _{DEASSERT}	170			μs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256 ¹ , 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384 ¹ , 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256 ¹ (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1 ¹	512	2386	1579
	64K	77576	990
SHA-256 ¹	512	2516	884
	64K	84752	938
SHA-384 ¹	1024	4154	884
	64K	100222	938
SHA-512 ¹	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384 ¹	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155

SigVer, DSA-2048/SHA-256	1024	9810527	10884
	8K	9597000	10719
Key Agreement (KAS), DH-3072 (p=3072, security=256)		4920705	9338
Key Agreement (KAS), DH-3072 (p=3072, security=256) ¹		78914533	9083

1. With DPA counter measures.

Table 122 • NRBG

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string		18221	2841
Reseed: no additional input, s=256		13585	1180
Reseed: 384-bit additional input, s=256		15922	1342
Generate: (no additional input), prediction resistance enabled, s= 256	128	15262	1755
	8K	27169	8223
Generate: (no additional input), prediction resistance disabled, s= 256	128	2138	1167
	8K	14045	8223
Generate: (384-bit additional input), prediction resistance enabled, s= 256	128	21299	1944
	8K	33206	8949
Generate: (384-bit additional input), prediction resistance disabled, s= 256	128	11657	1894
	8K	23564	8950
Un-instantiate		761	666

1. With DPA counter measures.