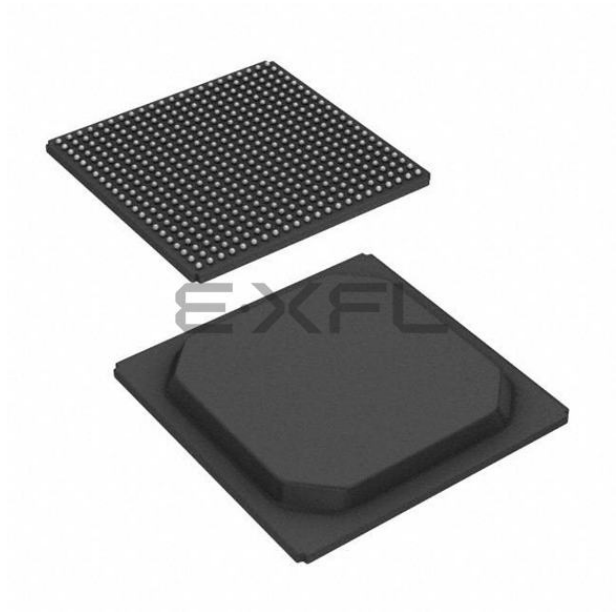

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	244
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300tls-fcg484i

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

6.2.2.1 Power-Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section Recommended Operating Conditions (see page 6). All supplies must rise and fall monotonically.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V_{DD}	0.2	50	ms
Transceiver core supply	V_{DDA}	0.2	50	ms
Must connect to 1.8 V supply	V_{DD18}	0.2	50	ms
Must connect to 2.5 V supply	V_{DD25}	0.2	50	ms
Must connect to 2.5 V supply	V_{DDA25}	0.2	50	ms
HSIO bank I/O power supplies	$V_{DDI[0,1,6,7]}$	0.2	50	ms
GPIO bank I/O power supplies	$V_{DDI[2,4,5]}$	0.2	50	ms
Bank 3 dedicated I/O buffers (GPIO)	V_{DDI3}	0.2	50	ms
GPIO bank auxiliary power supplies	$V_{DDAUX[2,4,5]}$	0.2	50	ms
Transceiver reference clock supply	$V_{DD\_XCVR\_CLK}$	0.2	50	ms
Global V_{REF} for transceiver reference clocks	$XCVR_{VREF}$	0.2	50	ms

Note: For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • Hot Socketing DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended)[1, 2]	I_{XCVRRX_HS}			±4	mA	V_{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended)[3]	I_{XCVRTX_HS}			±10	mA	V_{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended)[4]	$I_{XCVRREF\_HS}$			±1	mA	$V_{DD\_XCVR\_CLK}$ = 0 V
Current per GPIO pin (P or N single-ended)[5]	I_{GPIO_HS}			±1	mA	V_{DDIx} = 0 V
Current per HSIO pin (P or N single-ended)						Hot socketing is not supported in HSIO.

1. Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
2. Each P and N transceiver input has less than the specified maximum input current.
3. Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
4. $V_{DD\_XCVR\_CLK}$ is powered down and the device is driven to $–0.3\ V < V_{IN} < V_{DD\_XCVR\_CLK}$.
5. V_{DDIx} is powered down and the device is driven to $–0.3\ V < V_{IN} <$ GPIO V_{DDImax}.

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{OL} Min (V)	V_{OL} Max (V)	V_{OH} Min (V)	V_{OH} Max (V)	I_{OL}[2,6] mA	I_{OH}[2,6] mA
HSTL135I[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH}) /50
HSTL135II[4]	1.283	1.35	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSTL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH}) /50
HSTL12II[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSUL18I[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/55	(V_{DDI} – V_{OH}) /55
HSUL18II[4]	1.71	1.8	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH}) /25
HSUL12I[4]	1.14	1.2	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH}) /40
POD12I[4,5]	1.14	1.2	1.26		0.5 × V_{DDI}			V_{OL}/48	(V_{DDI} – V_{OH}) /48
POD12II[4,5]	1.14	1.2	1.26		0.5 × V_{DDI}			V_{OL}/34	(V_{DDI} – V_{OH}) /34

1. Drive strengths per PCI specification V/I curves.
2. Refer to UG0686: PolarFire FPGA User I/O User Guide for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. I_{OL}/I_{OH} units for impedance standards in amps (not mA).
5. VOH_MAX based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

Table 14 • Differential DC Input Levels

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18[4]	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6

I/O Standard	Bank Type	VICM_RANGE Libero Setting	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
HCSL25[6]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.55	1.1
		Low	0.05	0.35	0.8	0.1	0.55	1.1
HCSL18[5]	HSIO	Mid (default)	0.6	1.0	1.65	0.1	0.55	1.1
		Low	0.05	0.4	0.8	0.1	0.55	1.1
BUSLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.1	V_{DDIn}
		Low	0.05	0.4	0.8	0.05	0.1	V_{DDIn}
MLVDSE25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.35	2.4
		Low	0.05	0.4	0.8	0.05	0.35	2.4
LVPECL33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
LVPECLE33	GPIO	Mid (default)	0.6	1.65	2.35	0.05	0.8	2.4
		Low	0.05	0.4	0.8	0.05	0.8	2.4
MIPI25	GPIO	Mid (default)	0.6	1.25	2.35	0.05	0.2	0.3
		Low	0.05	0.2	0.8	0.05	0.2	0.3

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} – 0.4 V;
   b. V_{ICM} + V_{ID}/2 must be <V_{DDI} + 0.4 V;
   c. V_{ICM} – V_{ID}/2 must be >VSS – 0.3 V;
   d. Any differential input with V_{ICM} ≤0.6 V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

Table 15 • Differential DC Output Levels

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
LVDS33	GPIO		1.2		0.25	0.35	0.45
LVDS25	GPIO		1.2		0.25	0.35	0.45
LCMDS33	GPIO		0.6		0.25	0.35	0.45
LCMDS25	GPIO		0.6		0.25	0.35	0.45
RSDS33	GPIO		1.2		0.17	0.2	0.23
RSDS25	GPIO		1.2		0.17	0.2	0.23
MINILVDS33	GPIO		1.2		0.3	0.4	0.6
MINILVDS25	GPIO		1.2		0.3	0.4	0.6
SUBLVDS33	GPIO		0.9		0.1	0.15	0.3
SUBLVDS25	GPIO		0.9		0.1	0.15	0.3
PPDS33	GPIO		0.8		0.17	0.2	0.23
PPDS25	GPIO		0.8		0.17	0.2	0.23
SLVSE15[3]	GPIO, HSIO		0.2		0.12	0.135	0.15
BUSLVDSE25[3]	GPIO		1.25		0.24	0.262	0.272

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
SLVS25	SLVS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
BLVDSE25[6]	Bus LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MLVDSE25[6]	Multipoint LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
LVPECLE33[6]	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
SSTL25I	Differential SSTL 2.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL25II	Differential SSTL 2.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL18I	Differential SSTL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL18II	Differential SSTL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15I	Differential HSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15II	Differential HSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL135I	Differential HSTL 1.35 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V

Standard	STD	–1	Unit
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps
MIPI25/MIPI33	800	800	Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with V_{ID} ≥200 mV.

7.1.4 Output Buffer Speed

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL18I (differential)	800	1066	Mbps
SSTL18II (differential)	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL15I (differential)	1066	1333	Mbps
SSTL15II (differential)	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps
SSTL135I (differential)	1066	1333	Mbps
SSTL135II (differential)	1066	1333	Mbps
HSTL15I	900	1100	Mbps
HSTL15II	900	1100	Mbps
HSTL15I (differential)	900	1100	Mbps
HSTL15II (differential)	900	1100	Mbps
HSTL135I	1066	1066	Mbps
HSTL135II	1066	1066	Mbps
HSTL135I (differential)	1066	1066	Mbps
HSTL135II (differential)	1066	1066	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12I (differential)	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12I (differential)	1066	1266	Mbps
POD12I	1333	1600	Mbps
POD12II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps

Standard	STD	–1	Unit
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25/LCMDS25	1250	1250	Mbps
LVDS33/LCMDS33	1250	1600	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
SSTL25I	800	800	Mbps
SSTL25II	800	800	Mbps
SSTL25I (differential)	800	800	Mbps
SSTL25II (differential)	800	800	Mbps
SSTL18I	800	800	Mbps
SSTL18II	800	800	Mbps
SSTL18I (differential)	800	800	Mbps
SSTL18II (differential)	800	800	Mbps
SSTL15I	800	1066	Mbps
SSTL15II	800	1066	Mbps
SSTL15I (differential)	800	1066	Mbps
SSTL15II (differential)	800	1066	Mbps
HSTL15I	900	900	Mbps
HSTL15II	900	900	Mbps
HSTL15I (differential)	900	900	Mbps
HSTL15II (differential)	900	900	Mbps
HSUL18I	400	400	Mbps
HSUL18II	400	400	Mbps
HSUL18I (differential)	400	400	Mbps
HSUL18II (differential)	400	400	Mbps
PCI	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps
MIPIE25	500	500	Mbps

Parameter[1]	Symbol	Min	Typ	Max	Unit
Secondary output clock frequency[2]	F_{OUTSF}	33.3		800	MHz
Input clock cycle-to-cycle jitter	F_{INJ}			200	ps
Output clock period cycle-to-cycle jitter (w/clean input)	$T_{OUTJITTERP}$			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T_{SKEW}			±200	ps
DLL lock time	T_{LOCK}	16		16K	Reference clock cycles
Minimum reset pulse width	T_{MRPW}	3			ns
Minimum input pulse width[3]	T_{MIPW}	20			ns
Minimum input clock pulse width high	T_{MPWH}	400			ps
Minimum input clock pulse width low	T_{MPWL}	400			ps
Delay step size	T_{DEL}	12.7	30	35	ps
Maximum delay block delay[4]	T_{DELMAX}	1.8		4.8	ns
Output clock duty cycle (with 50% duty cycle input)[5]	T_{DUTY}	40		60	%
Output clock duty cycle (in phase reference mode)[5]	T_{DUTY50}	45		55	%

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 39 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{2FREQ}		2		MHz
Accuracy	RC_{2FACC}	–4		4	%
Duty cycle	RC_{2DC}	46		54	%
Peak-to-peak output period jitter	RC_{2PJIT}		5	10	ns
Peak-to-peak output cycle-to-cycle jitter	RC_{2CJIT}		5	10	ns
Operating current (V_{DD25})	RC_{2IVPPA}			60	µA
Operating current (V_{DD})	RC_{2IVDD}			2.6	µA

Table 40 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{SCFREQ}		160		MHz
Accuracy	RC_{SCFACC}	–4		4	%
Duty cycle	RC_{SCDC}	47		52	%
Peak-to-peak output period jitter	RC_{SCPJIT}			600	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{SCCJIT}			172	ps
Operating current (V_{DD25})	RC_{SCVPPA}			599	µA

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2, 3]	$F_{XCVRREFCLKMAX\ CASCADE}$	20		156	20		156	MHz
Reference clock rate at the PFD[4]	$F_{TXREFCLKPFD}$	20		156	20		156	MHz
Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4]	$F_{TXREFCLKPFD10G}$	75		156	75		156	MHz
Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5]	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 10 KHz	$F_{TXREFPN}$			–110			–110	dBc /Hz
Phase noise at 100 KHz	$F_{TXREFPN}$			–115			–115	dBc /Hz
Phase noise at 1 MHz	$F_{TXREFPN}$			–135			–135	dBc /Hz
Reference clock input rise time (10%–90%)	$T_{REFRISE}$		200	500		200	500	ps
Reference clock input fall time (90%–10%)	$T_{REFFALL}$		200	500		200	500	ps
Reference clock duty cycle	$T_{REFDUTY}$	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	TxREF CLKPFD/ (128)	32	TxREF CLKPFD/ (128*63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential I/O standards supported as transceiver reference clocks.

Table 52 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}		85		Ω	
	V_{OTERM}		100		Ω	
	V_{OTERM}		150		Ω	
Common mode voltage[1]	V_{OCM}	0.44 × V_{DDA}	0.525 × V_{DDA}	0.59 × V_{DDA}	V	DC coupled 50% setting
	V_{OCM}	0.52 × V_{DDA}	0.6 × V_{DDA}	0.66 × V_{DDA}	V	DC coupled 60% setting
	V_{OCM}	0.61 × V_{DDA}	0.7 × V_{DDA}	0.75 × V_{DDA}	V	DC coupled 70% setting
	V_{OCM}	0.63 × V_{DDA}	0.8 × V_{DDA}	0.83 × V_{DDA}	V	DC coupled 80% setting
Rise time[2]	T_{TxRF}	41		70	ps	20% to 80%
Fall time[2]		41		70	ps	80% to 20%
Differential peak-to-peak amplitude	V_{ODPP}		1040		mV	1000 mV setting
	V_{ODPP}		840		mV	800 mV setting
	V_{ODPP}		630		mV	600 mV setting
	V_{ODPP}		620		mV	500 mV setting
	V_{ODPP}		530		mV	400 mV setting
	V_{ODPP}		360		mV	300 mV setting
	V_{ODPP}		240		mV	200 mV setting
	V_{ODPP}		160		mV	100 mV setting
Transmit lane P to N skew[3]	T_{OSKEW}		8	15	ps	
Lane to lane transmit skew[4]	T_{LLSKEW}			75	ps	Single PLL
					ps	Multiple PLL
Electrical idle transition entry time[7]	TTxEITrEntry				ns	
Electrical idle transition exit time[7]	TTxEITrExit				ns	
Electrical idle amplitude	VTxEIpp				mV	
TXPLL lock time	T_{TXLock}			1600	PFD cycles	
Digital PLL lock time[8]	$T_{DPLLLock}$				REFCLK UIs	
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}				UI UI	Data rate ≥8.5 Gbps to 12.7 Gbps[9] (Tx V_{CO} rate 4.25 GHz to 6.35 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥3.2 Gbps to 8.5 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.28 0.07	UI UI	Data rate ≥1.6 Gbps to 3.2 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.13 0.02	UI UI	Data rate ≥ 800 Mbps to 1.6 Gbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)
Total jitter[5,6] Deterministic jitter[5,6]	T_J T_{DJ}			0.06 0.01	UI UI	Data rate = 250 Mbps to 800 Mbps (Tx V_{CO} rate 2.5 GHz to 5.0 GHz)

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

Table 75 • FPGA Programming Cycles Lifetime Factor

Programming T_J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Notes:

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures (T_J).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

7.6.5 Digest Time

The following table describes digest time.

Table 76 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		µs
Fabric digest run time	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	1005	1072	ms
	MPF300T, TL, TS, TLS	1503.9	1582	ms
	MPF500T, TL, TS, TLS			ms
UFS CC digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	35	µs
	MPF300T, TL, TS, TLS	33.2	35	µs
	MPF500T, TL, TS, TLS			µs
sNVM digest run time[1]	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS	4.4	4.8	ms
	MPF300T, TL, TS, TLS	4.4	4.8	ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	46.6	48.8	µs
	MPF300T, TL, TS, TLS	46.6	48.8	µs
	MPF500T, TL, TS, TLS			µs
User key digest run time[2]	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	525.4	543.3	µs
	MPF300T, TL, TS, TLS	525.4	543.3	µs
	MPF500T, TL, TS, TLS			µs

Parameter	Devices	Typ	Max	Unit
UFS UPERM digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	33.2	34.9	µs
	MPF300T, TL, TS, TLS	33.2	34.9	µs
	MPF500T, TL, TS, TLS			µs
Factory digest run time	MPF100T, TL, TS, TLS			µs
	MPF200T, TL, TS, TLS	493.6	510.1	µs
	MPF300T, TL, TS, TLS	493.6	510.1	µs
	MPF500T, TL, TS, TLS			µs

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 77 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 78 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53[1]	s
	MPF300T, TL, TS, TLS	90[1]	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37[2]	s
	MPF300T, TL, TS, TLS	55[2]	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

Notes:

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Parameter	Symbol	Service ID	Typ	Max	Unit	Conditions
Secure NVM read	T_{SNVM_Rd}	18H				Note 1
Digital signature service raw	T_{SIG_RAW}	19H	174	187	ms	
Digital signature service DER	T_{SIG_DER}	1AH	174	187	ms	
Reserved		1BH–1FH				
PUF emulation	$T_{Challenge}$	20H	1.8	2.0	ms	
Nonce service	T_{Nonce}	21H	1.2	1.4	ms	
Bitstream authentication	TBIT_AUTH	22H				Note 4
IAP Image authentication	TIAP_AUTH	23H				Note 4
Reserved		26H–3FH				
In application programming by index	$T_{IAP\_Prg\_Index}$	42H				Note 2
In application programming by SPI address	$T_{IAP\_Prg\_Addr}$	43H				Note 2
In application verify by index	TIAP_Ver_Index	44H				Note 5
In application verify by SPI address	TIAP_Ver_Addr	45H				Note 5
Auto update	$T_{AutoUpdate}$	46H				Note 2
Digest check	T_{digest_chk}	47H				Note 3

1. See sNVM Read/Write Characteristics (see page 58).
2. See SPI Master Programming Time (see page 52).
3. See Digest Times (see page 54).
4. See Authentication Services Time (see page 58).
5. See Verify Services Time (see page 58).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

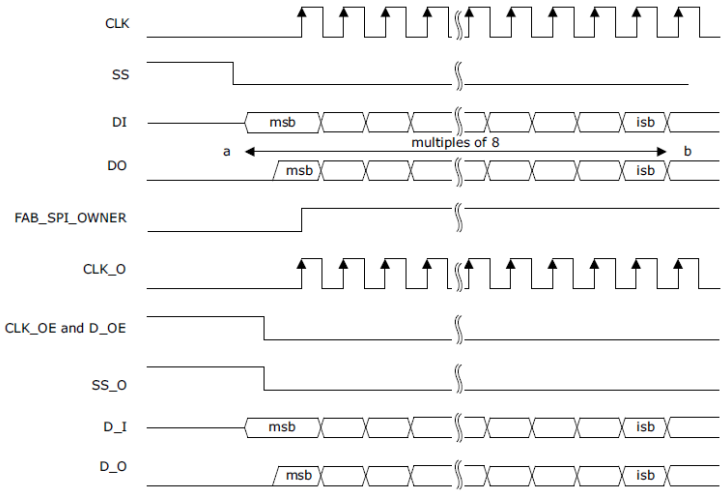
7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 88 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F_{TCK}			25	MHz	

Figure 4 • USPI Switching Characteristics



7.8.4 Tamper Detectors

The following section describes tamper detectors.

Table 91 • ADC Conversion Rate

Parameter	Description	Min	Typ[1]	Max
T_{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0.	420 µs		470 µs
T_{CONVN}	Time between subsequent channel conversions.		480 µs	
T_{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs.	0 ns		
T_{VALID}[2]	Width of the valid pulse.	1.625 µs		2 µs
T_{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 µs	Rate × 32 µs	8128 µs

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

Table 92 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	–40		125	°C	
Temperature sensing accuracy	–10		10	°C	

Parameter	Symbol	Typ	Max	Unit
Time from negation of RESPONSE to all I/Os re-enabled	$T_{CLR\_IO\_DISABLE}$	28	38	µs
Time from triggering the response to security locked	$T_{LOCKDOWN}$			ns
Time from negation of RESPONSE to earlier security unlock condition	$T_{CLR\_LOCKDOWN}$			ns
Time from triggering the response to device enters RESET	T_{tr_RESET}	11.7	14	µs
Time from triggering the response to start of zeroization	$T_{tr\_ZEROLISE}$	7.4	8.2	ms

7.8.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

Table 95 • System Controller Suspend Entry and Exit Characteristics

Parameter	Symbol	Definition	Typ	Max	Unit
Time from TRSTb falling edge to SUSPEND_EN signal assertion	$T_{suspend\_Tr}$[1, 2]	Suspend entry time from TRST_N assertion	42	44	ns
Time from TRSTb rising edge to ACTIVE signal assertion	$T_{suspend\_exit}$	Suspend exit time from TRST_N negation	361	372	ns

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

7.8.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

Table 96 • Dynamic Reconfiguration Interface Timing Characteristics

Parameter	Symbol	Max	Unit
PCLK frequency	F_{PD_PCLK}	200	MHz

7.9 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

7.9.1 Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.

ECDSA SigVer, P-384/SHA-384	1024	6421841	5759
	8K	6273510	5759
Key Agreement (KAS), P-384		5039125	6514
Point Multiply, P-256[1]		5176923	4482
Point Multiply, P-384[1]		12043199	5319
Point Multiply, P-521[1]		26887187	6698
Point Addition, P-384		3018067	5779
KeyGen (PKG), P-384		12055368	6908
Point Verification, P-384		5091	3049

1. With DPA counter measures.

Table 120 • IFC (RSA)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	436972	8,972
Encrypt, RSA-3072, e=65537	3072	962162	12,583
Decrypt, RSA-2048[1], CRT	2048	26862392	15900
Decrypt, RSA-3072[1], CRT	3072	75153782	22015
Decrypt, RSA-4096, CRT	4096	89235615	23710
Decrypt, RSA-3072, CRT	3072	37880180	18638
SigGen, RSA-3072/SHA-384[1] ,CRT, PKCS #1 V 1 1.5	1024	75197644	20032
	8K	75213653	19303
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	148090970	14642
	8K	148102576	13936
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	970991	12000
	8K	982011	11769
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	443493	8436
	8K	453007	8436
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	147138254	13945
	8K	147155896	13523
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	973269	11313
	8K	983255	11146

1. With DPA counter measures.

Table 121 • FFC (DH)

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SigGen, DSA-3072/SHA-384[1]	1024	27932907	13969
	8K	27942415	13501
SigGen, DSA-3072/SHA-384	1024	12086356	13602
SigVer, DSA-3072/SHA-384	1024	24597916	15662
	8K	24229420	15133

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