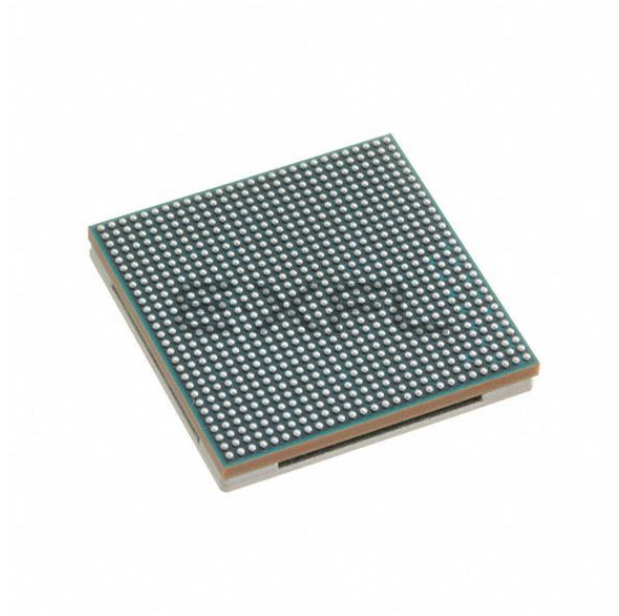

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	300000
Total RAM Bits	21094400
Number of I/O	388
Number of Gates	-
Voltage - Supply	0.97V ~ 1.08V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mpf300tls-fcg784i

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		10	µA	I/O disabled, high – Z
	I_L (HSIO)		10	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	137	220	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		102	166	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		68	115	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		47	79	µA	V_{DDIx} = 1.2 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20%–80% of swing and maximum value of 500 ps 20%–80% of swing.
5. GPIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

Note: Overshoot level is for V_{DDI} at 3.3 V.

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V_{IN}) Undershoot Duration as % at T_J = 100 °C	Condition (V)
100	–0.5
100	–0.55
100	–0.6
100	–0.65
100	–0.7
100	–0.75
100	–0.8
100	–0.85
100	–0.9
100	–0.95
100	–1
100	–1.05
100	–1.1
100	–1.15
100	–1.2
69	–1.25
45	–1.3

Note: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

Table 12 • DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH}[1] Max (V)
PCI	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45
LVTTL	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS33	3.15	3.3	3.45	–0.3	0.8	2	3.45
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625
LVCMOS18	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89
LVCMOS15	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575
LVCMOS12	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26
SSTL25I[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL25II[2]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625
SSTL18I[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL18II[2]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89
SSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575
SSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575

I/O Standard	Bank Type	V_{OCM}[1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD}[2] Min (V)	V_{OD}[2] Typ (V)	V_{OD}[2] Max (V)
MLVDSE25[3]	GPIO		1.25		0.396	0.442	0.453
LVPECLE33[3]	GPIO		1.65		0.664	0.722	0.755
MIPIE25[3]	GPIO		0.25		0.1	0.22	0.3

1. V_{OCM} is the output common mode voltage.
2. V_{OD} is the output differential voltage.
3. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

Table 16 • Complementary Differential DC Input Levels

I/O Standard	V_{DDI} Min (V)	V_{DDI} Typ (V)	V_{DDI} Max (V)	V_{ICM}[1,3] Min (V)	V_{ICM}[1,3] Typ (V)	V_{ICM}[1,3] Max (V)	V_{ID}[2] Min (V)	V_{ID} Max (V)
SSTL25I	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL25II	2.375	2.5	2.625	1.164	1.250	1.339	0.1	
SSTL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
SSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
SSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
SSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL15I	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL15II	1.425	1.5	1.575	0.698	0.750	0.803	0.1	
HSTL135I	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL135II	1.283	1.35	1.418	0.629	0.675	0.723	0.1	
HSTL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
HSUL18I	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL18II	1.71	1.8	1.89	0.838	0.900	0.964	0.1	
HSUL12I	1.14	1.2	1.26	0.559	0.600	0.643	0.1	
POD12I	1.14	1.2	1.26	0.787	0.840	0.895	0.1	
POD12II	1.14	1.2	1.26	0.787	0.840	0.895	0.1	

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{ICM} rules are as follows:
   a. V_{ICM} must be less than V_{DDI} -0.4V;
   b. $V_{ICM} + V_{ID}/2$ must be $<V_{DDI} + 0.4$ V;
   c. $V_{ICM} – V_{ID}/2$ must be >VSS – 0.3 V.

Min (%)	Typ	Max (%)	Unit	Condition
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 80% of V_{DDI}.

Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	20	Ω	V_{ICM} < 0.8 V
		–20	100	40	Ω	0.6 V < V_{ICM} < 1.65 V
		–20	100	80	Ω	1.4 V < V_{ICM}
Single-ended thevenin termination[2, 3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Single-ended termination to V_{SS}[4, 5]	Internal parallel termination to V_{SS}	–20	120	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V
		–20	240	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V/1.2 V

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of V_{DDI}.
5. Supported terminations vary with the IO type regardless of V_{DDI} nominal voltage. Refer to Libero for available combinations.

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
PCI	PCIE 3.3 V	0	VDDI			VDDI/2		V
LVTTL33	LVTTL 3.3 V	0	VDDI			VDDI/2		V
LVCMOS33	LVCMOS 3.3 V	0	VDDI			VDDI/2		V
LVCMOS25	LVCMOS 2.5 V	0	VDDI			VDDI/2		V
LVCMOS18	LVCMOS 1.8 V	0	VDDI			VDDI/2		V
LVCMOS15	LVCMOS 1.5 V	0	VDDI			VDDI/2		V
LVCMOS12	LVCMOS 1.2 V	0	VDDI			VDDI/2		V
SSTL25I	SSTL 2.5 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL25II	SSTL 2.5 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	1.25	V
SSTL18I	SSTL 1.8 V Class I	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL18II	SSTL 1.8 V Class II	V_{REF} – 0.5	V_{REF} + 0.5			V_{REF}	0.90	V
SSTL15I	SSTL 1.5 V Class I	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL15II	SSTL 1.5 V Class II	V_{REF} – .175	V_{REF} + .175			V_{REF}	0.75	V
SSTL135I	SSTL 1.35 V Class I	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
SSTL135II	SSTL 1.35 V Class II	V_{REF} – .16	V_{REF} + .16			V_{REF}	0.675	V
HSTL15I	HSTL 1.5 V Class I	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL15II	HSTL 1.5 V Class II	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.75	V
HSTL135I	HSTL 1.35 V Class I	V_{REF} – 0.45	V_{REF} + . 45			V_{REF}	0.675	V
HSTL135II	HSTL 1.35 V Class II	V_{REF} – .45	V_{REF} + .45			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	V_{REF} – .4	V_{REF} + .4			V_{REF}	0.60	V

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

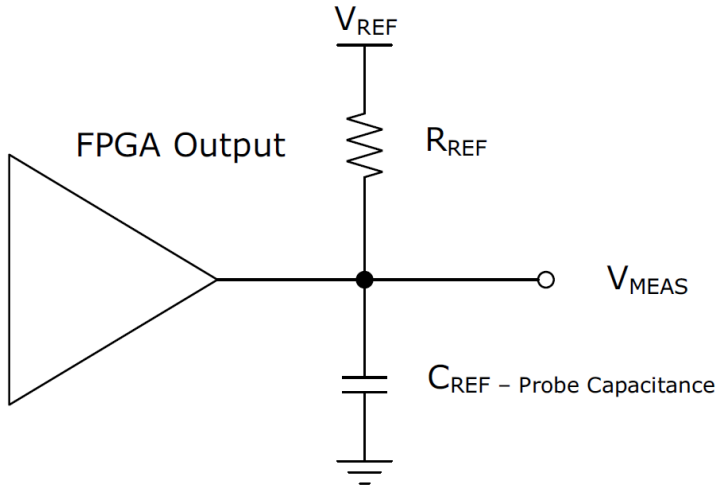
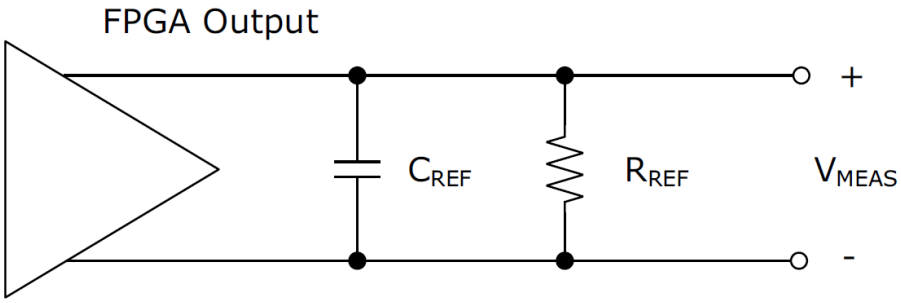


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	1250	1250	Mbps
RSDS18	800	800	Mbps
MINILVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18I	800	1066	Mbps
SSTL18II	800	1066	Mbps
SSTL15I	1066	1333	Mbps
SSTL15II	1066	1333	Mbps
SSTL135I	1066	1333	Mbps
SSTL135II	1066	1333	Mbps

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
QDRII+	8:1	1.8 V	1.5 V	900	1100	112.5	137.5
RLDRAM3[1]	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3[1]	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3[1]	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2[1]	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2[1]	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2[1]	2:1	1.8 V	1.8 V	333	400	167	200

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2[1]	4:1	2.5 V	1.8 V	800	800	200	200
RLDRAM2[1]	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is currently not supported with a soft IP controller.

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F_{MAX} 2:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 4:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
Output F_{MAX} 8:1	TX_DDRX_B_C	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, centered with PLL
In delay, out delay, DLL delay step sizes			12.7	30	35	12.7	25	29.5	ps	

Table 34 • I/O CDR Switching Characteristics

Parameter	Min	Max	Unit
Data rate	266	1250	Mbps
Receiver Sinusoidal jitter tolerance[1]	0.2		UI

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

Note: See the LVDS output buffer specifications for transmit characteristics.

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications.

Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Global clock F_{MAX}	F_{MAXG}	500	500	500	500	MHz	
Regional clock F_{MAX}	F_{MAXR}	375	375	375	375	MHz	Transceiver interfaces only
	F_{MAXR}	250	250	250	250	MHz	All other interfaces
Global clock duty cycle distortion	T_{DCDG}	190	190	190	190	ps	At 500 MHz

Parameter	Modes [1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		260		320	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	Mhz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1)		225		266	MHz
	20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1)		225		266	MHz
	32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1)		225		266	MHz
	40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1]		225		266	MHz
	64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		165		200	MHz
	80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1]		130		160	MHz

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

Note: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 53 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}		85		Ω	
	V_{ITERM}		100		Ω	
	V_{ITERM}		150		Ω	
Common mode voltage	V_{ICMDC} [1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			200	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}				CDR_{REFCLK} UI	
CDR lock-to-ref time	T_{LTF}				CDR_{REFCLK} UI	
Loss-of-signal detect (Peak Detect Range setting = high)[9]	$V_{DETLHIGH}$				mV	Setting = 1
	$V_{DETLHIGH}$				mV	Setting = 2
	$V_{DETLHIGH}$				mV	Setting = 3
	$V_{DETLHIGH}$				mV	Setting = 4
	$V_{DETLHIGH}$				mV	Setting = 5
	$V_{DETLHIGH}$				mV	Setting = 6
	$V_{DETLHIGH}$				mV	Setting = 7
Loss-of-signal detect (Peak Detect Range setting = low)[9]	V_{DETLOW}	65		175	mV	Setting = PCIe[3,7]
	V_{DETLOW}	95		190	mV	Setting = SATA[4,8]
	V_{DETLOW}	75		170	mV	Setting = 1
	V_{DETLOW}	95		185	mV	Setting = 2
	V_{DETLOW}	100		190	mV	Setting = 3
	V_{DETLOW}	140		210	mV	Setting = 4
	V_{DETLOW}	155		240	mV	Setting = 5
	V_{DETLOW}	165		245	mV	Setting = 6
	V_{DETLOW}	170		250	mV	Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5 Gbps – 12.7 Gbps [5, 10]

Table 55 • PCI Express Gen2

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.35	UI
Receiver jitter tolerance	5.0 Gbps	0.4		UI

Note: With add-in card as specified in PCI Express CEM Rev 2.0.

7.5.2 Interlaken

The following table describes Interlaken.

Table 56 • Interlaken

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	6.375 Gbps		0.3	UI
	10.3125 Gbps		0.3	UI
	12.7 Gbps[1]			UI
Receiver jitter tolerance	6.375 Gbps	0.6		UI
	10.3125 Gbps	0.65		UI
	12.7 Gbps[1]			UI

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

Table 57 • 10GbE (10GBASE-R)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps		0.28	UI
Receiver jitter tolerance	10.3125 Gbps	0.7		UI

The following table describes 10GbE (10GBASE-KR).

Table 58 • 10GbE (10GBASE-KR)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (XAUI).

Table 59 • 10GbE (XAUI)

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter (near end)	3.125 Gbps		0.35	UI
Total transmit jitter (far end)			0.55	UI
Receiver jitter tolerance	3.125 Gbps	0.65		UI

The following table describes 10GbE (RXAUI).

Table 60 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

7.5.4 1GbE (1000BASE-T)

The following table describes 1GbE (1000BASE-T).

Table 61 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 62 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

7.5.5 SGMII and QSGMII

The following table describes SGMII.

Table 63 • SGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps		0.24	UI
Receiver jitter tolerance	1.25 Gbps	0.749		UI

The following table describes QSGMII.

Table 64 • QSGMII

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps		0.3	UI
Receiver jitter tolerance	5.0 Gbps	0.65		UI

7.5.6 SDI

The following table describes SDI.

Table 65 • SDI

Parameter	Data Rate	Min	Max	Unit
Total transmit jitter				UI
Receiver jitter tolerance				UI

7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 68 • FPGA Programming Cycles vs Retention Characteristics

Programming T_J	Programming Cycles, Max	Retention Years	Retention Years at T_J
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 69 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	17	25	s
		MPF300T, TL, TS, TLS	26	32	s
		MPF500T, TL, TS, TLS			s

Table 70 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	41[1]		s
		MPF300T, TL, TS, TLS	50[1]	60	s
		MPF500T, TL, TS, TLS			s

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

Table 71 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS		56	s
		MPF300T, TL, TS, TLS[1]		95	s
		MPF500T, TL, TS, TLS			s

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data PNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 79 • Zeroization Times for MPF300T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non- recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 80 • Zeroization Times for MPF500T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing

Parameter	Typ	Max	Unit	Conditions
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			s	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			s	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			s	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1]			s	Full scrubbing
Time to verify[5]			s	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 81 • Standalone Fabric Verify Times

Parameter	Devices	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	53[1]	s
	MPF300T, TL, TS, TLS	90[1]	s
	MPF500T, TL, TS, TLS		s
Standalone verification over SPI	MPF100T, TL, TS, TLS		s
	MPF200T, TL, TS, TLS	37[2]	s
	MPF300T, TL, TS, TLS	55[2]	s
	MPF500T, TL, TS, TLS		s

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

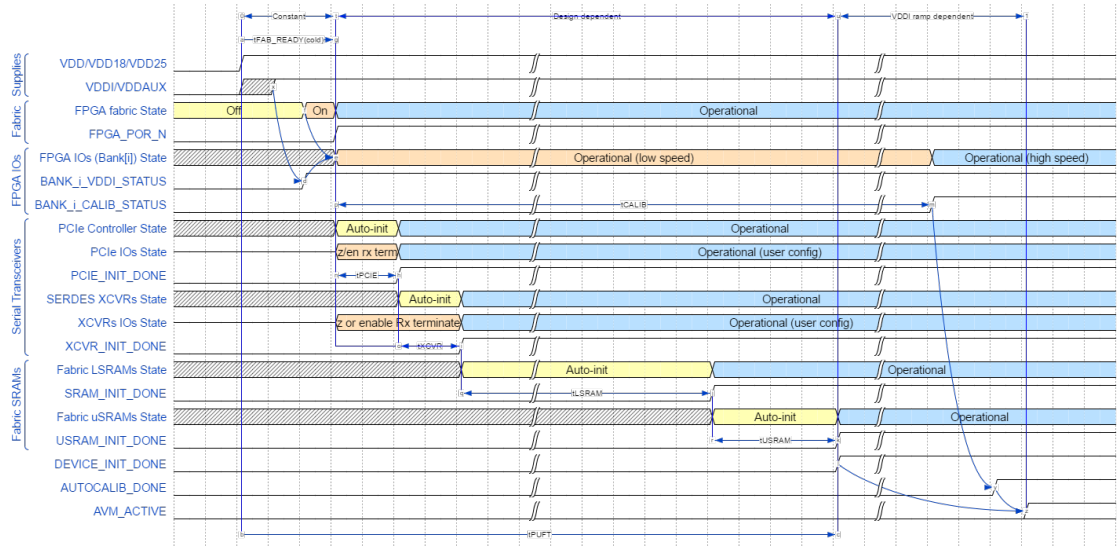
Notes:

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

Table 82 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor	Units
MPF100T, TL, TS, TLS						
MPF200T, TL, TS, TLS	9	67	53			s
MPF300T, TL, TS, TLS	14	95	90			s

Figure 5 • Cold Reset Timing



Notes:

- The previous diagram showsthe case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
  - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
  - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
  - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

7.9.2 Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

1. With DPA counter measures.

Table 115 • HMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
HMAC-SHA-256[1], 256-bit key	512	7477	2361
	64K	88367	2099
HMAC-SHA-384[1], 384-bit key	1024	13049	2257
	64K	106103	2153

1. With DPA counter measures.

Table 116 • CMAC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
AES-CMAC-256[1] (message is only authenticated)	128	446	9058
	64K	45494	111053

1. With DPA counter measures.

Table 117 • KEY TREE

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
128-bit nonce + 8-bit optype		102457	2751
256-bit nonce + 8-bit optype		103218	2089

Table 118 • SHA

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
SHA-1[1]	512	2386	1579
	64K	77576	990
SHA-256[1]	512	2516	884
	64K	84752	938
SHA-384[1]	1024	4154	884
	64K	100222	938
SHA-512[1]	1024	4154	881
	64K	100222	935

1. With DPA counter measures.

Table 119 • ECC

Modes	Message Size (bits)	Athena TeraFire Crypto Core Clock-Cycles	CAL Delay In CPU Clock-Cycles
ECDSA SigGen, P-384/SHA-384[1]	1024	12528912	6944
	8K	12540448	5643
ECDSA SigGen, P-384/SHA-384	1024	5502928	6155