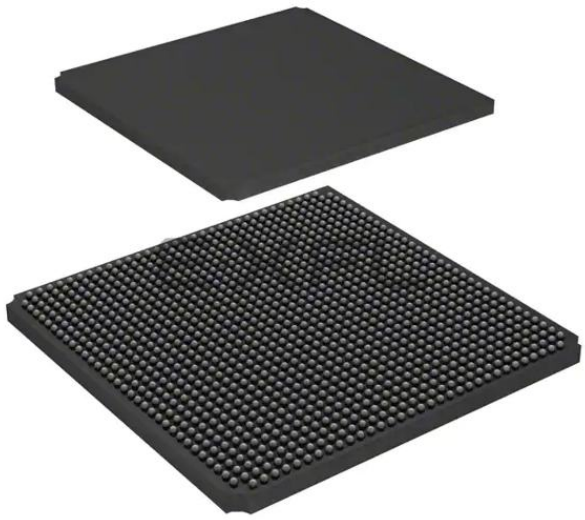

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 481000 |
| Total RAM Bits | 33792000 |
| Number of I/O | 584 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.08V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/mpf500tl-fcg1152e |

# Contents

# 3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$[1] Max (V) |
|---|---|---|---|---|---|---|---|
| SSTL135I | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| SSTL135II | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| HSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| HSTL135I | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL135II | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| HSTL12II | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| HSUL18I | 1.71 | 1.8 | 1.89 | –0.3 | 0.3 × $V_{DDI}$ | 0.7 × $V_{DDI}$ | 1.89 |
| HSUL18II | 1.71 | 1.8 | 1.89 | –0.3 | 0.3 × $V_{DDI}$ | 0.7 × $V_{DDI}$ | 1.89 |
| HSUL12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| POD12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | 1.26 |
| POD12II | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | 1.26 |

1. GPIO $V_{IH}$ max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. For external stub-series resistance. This resistance is on-die for GPIO.

**Note:** 3.3 V and 2.5 V are only supported in GPIO banks.

**Table 17 • Complementary Differential DC Output Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Min (V) | $V_{OL}$ Max (V) | $V_{OH}$[1,3] Min (V) | $I_{OL}$[2] Min (mA) | $I_{OH}$[2] Min (mA) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | 8.1 |
| SSTL25II | 2.375 | 2.5 | 2.625 | | $V_{TT}$ – 0.810 | $V_{TT}$ + 0.810 | 16.2 | 16.2 |
| SSTL18I | 1.71 | 1.8 | 1.89 | | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | 6.7 |
| SSTL18II | 1.71 | 1.8 | 1.89 | | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| HSTL15I | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI}$ – 0.4 | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI}$ – 0.4 | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/55 | ($V_{DDI}$ – $V_{OH}$)/55 |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| POD12I[3,4] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | $V_{OL}$/48 | ($V_{DDI}$ – $V_{OH}$)/48 |
| POD12II[3,4] | 1.14 | 1.2 | 1.26 | | 0.5 × $V_{DDI}$ | | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |

1. $V_{OH}$ is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers
3. $V_{OH\_MAX}$ based on external pull-up termination (pseudo-open drain).
4. $I_{OL}$/$I_{OH}$ units for impedance standards in amps (not mA).

### 6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

**Table 18 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V/1.35 V/1.2 V |
| –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |

| Parameter | Description | Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|---|---|
| Single-ended termination to $V_{SS}$[4, 5] | Internal parallel termination to $V_{SS}$ | –20 | 120 | 20 | Ω | $V_{DDI}$ = 2.5 V/1.8 V/1.5 V/1.2 V |
| | | –20 | 240 | 20 | Ω | $V_{DDI}$ = 2.5 V/1.8 V/1.5 V/1.2 V |

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of $V_{DDI}$.
5. Supported terminations vary with the IO type regardless of $V_{DDI}$ nominal voltage. Refer to Libero for available combinations.

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSUL18I | HSUL 1.8 V Class I | $V_{REF}$ – 0.54 | $V_{REF}$ + 0.54 | | | $V_{REF}$ | 0.90 | V |
| HSUL18II | HSUL 1.8 V Class II | $V_{REF}$ – 0.54 | $V_{REF}$ + 0.54 | | | $V_{REF}$ | 0.90 | V |
| HSUL12 | HSUL 1.2 V | $V_{REF}$ – .22 | $V_{REF}$ + .22 | | | $V_{REF}$ | 0.60 | V |
| POD12I | Pseudo open drain (POD) logic 1.2 V Class I | $V_{REF}$ – .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| POD12II | POD 1.2 V Class II | $V_{REF}$ – .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| LVDS33 | Low-voltage differential signaling (LVDS) 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS25 | LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS18 | LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| RSDS33 | RSDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS25 | RSDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS18 | RSDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS33 | Mini-LVDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS25 | Mini-LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS18 | Mini-LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| SUBLVDS33 | Sub-LVDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS25 | Sub-LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS18 | Sub-LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| PPDS33 | Point-to-point differential signaling 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS25 | PPDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS18 | PPDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| SLVS33 | Scalable low-voltage signaling 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | | V |

**Figure 1 • Output Delay Measurement—Single-Ended Test Setup**

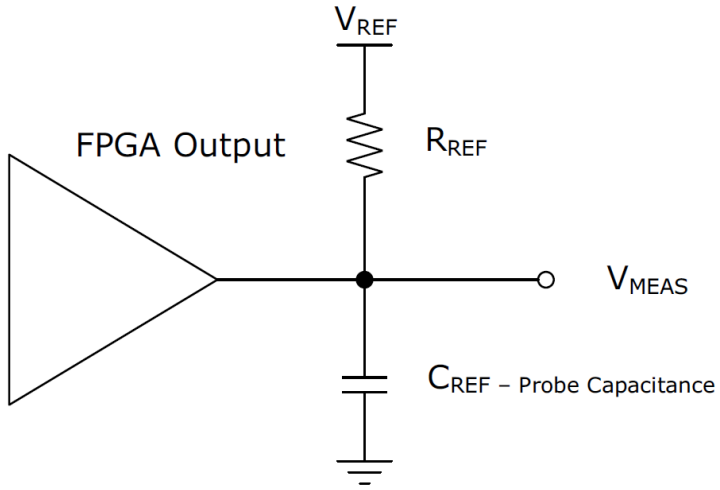
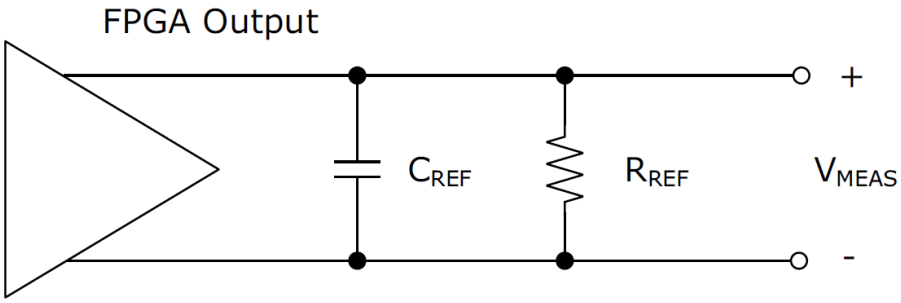



**Figure 2 • Output Delay Measurement—Differential Test Setup**




### 7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

**Table 24 • HSIO Maximum Input Buffer Speed**

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS18 | 1250 | 1250 | Mbps |
| RSDS18 | 800 | 800 | Mbps |
| MINILVDS18 | 800 | 800 | Mbps |
| SUBLVDS18 | 800 | 800 | Mbps |
| PPDS18 | 800 | 800 | Mbps |
| SLVS18 | 800 | 800 | Mbps |
| SSTL18I | 800 | 1066 | Mbps |
| SSTL18II | 800 | 1066 | Mbps |
| SSTL15I | 1066 | 1333 | Mbps |
| SSTL15II | 1066 | 1333 | Mbps |
| SSTL135I | 1066 | 1333 | Mbps |
| SSTL135II | 1066 | 1333 | Mbps |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|---|---|
| Output $F_{MAX}$ 2:1 | TX_DDRX_B_C | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered with PLL |
| Output $F_{MAX}$ 4:1 | TX_DDRX_B_C | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered with PLL |
| Output $F_{MAX}$ 8:1 | TX_DDRX_B_C | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered with PLL |
| In delay, out delay, DLL delay step sizes | | | 12.7 | 30 | 35 | 12.7 | 25 | 29.5 | ps | |

**Table 34 • I/O CDR Switching Characteristics**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Data rate | 266 | 1250 | Mbps |
| Receiver Sinusoidal jitter tolerance[1] | 0.2 | | UI |

1. Jitter values based on bit error ratio (BER) of 10–12, 80 MHz sinusoidal jitter injected to Rx data.

**Note:** See the LVDS output buffer specifications for transmit characteristics.

## 7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

### 7.2.1 Clocking

The following table provides clocking specifications.

**Table 35 • Global and Regional Clock Characteristics (–40 °C to 100 °C)**

| Parameter | Symbol | $V_{DD}$ = 1.0 V STD | $V_{DD}$ = 1.0 V –1 | $V_{DD}$ = 1.05 V STD | $V_{DD}$ = 1.05 V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Global clock $F_{MAX}$ | $F_{MAXG}$ | 500 | 500 | 500 | 500 | MHz | |
| Regional clock $F_{MAX}$ | $F_{MAXR}$ | 375 | 375 | 375 | 375 | MHz | Transceiver interfaces only |
| | $F_{MAXR}$ | 250 | 250 | 250 | 250 | MHz | All other interfaces |
| Global clock duty cycle distortion | $T_{DCDG}$ | 190 | 190 | 190 | 190 | ps | At 500 MHz |

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Secondary output clock frequency[2] | $F_{OUTSF}$ | 33.3 | | 800 | MHz |
| Input clock cycle-to-cycle jitter | $F_{INJ}$ | | | 200 | ps |
| Output clock period cycle-to-cycle jitter (w/clean input) | $T_{OUTJITTERP}$ | | | 300 | ps |
| Output clock-to-clock skew between two outputs with the same phase settings | $T_{SKEW}$ | | | ±200 | ps |
| DLL lock time | $T_{LOCK}$ | 16 | | 16K | Reference clock cycles |
| Minimum reset pulse width | $T_{MRPW}$ | 3 | | | ns |
| Minimum input pulse width[3] | $T_{MIPW}$ | 20 | | | ns |
| Minimum input clock pulse width high | $T_{MPWH}$ | 400 | | | ps |
| Minimum input clock pulse width low | $T_{MPWL}$ | 400 | | | ps |
| Delay step size | $T_{DEL}$ | 12.7 | 30 | 35 | ps |
| Maximum delay block delay[4] | $T_{DELMAX}$ | 1.8 | | 4.8 | ns |
| Output clock duty cycle (with 50% duty cycle input)[5] | $T_{DUTY}$ | 40 | | 60 | % |
| Output clock duty cycle (in phase reference mode)[5] | $T_{DUTY50}$ | 45 | | 55 | % |

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.

### 7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

**Table 39 • 2 MHz RC Oscillator Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency | $RC_{2FREQ}$ | | 2 | | MHz |
| Accuracy | $RC_{2FACC}$ | –4 | | 4 | % |
| Duty cycle | $RC_{2DC}$ | 46 | | 54 | % |
| Peak-to-peak output period jitter | $RC_{2PJIT}$ | | 5 | 10 | ns |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{2CJIT}$ | | 5 | 10 | ns |
| Operating current ($V_{DD25}$) | $RC_{2IVPPA}$ | | | 60 | µA |
| Operating current ($V_{DD}$) | $RC_{2IVDD}$ | | | 2.6 | µA |

**Table 40 • 160 MHz RC Oscillator Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency | $RC_{SCFREQ}$ | | 160 | | MHz |
| Accuracy | $RC_{SCFACC}$ | –4 | | 4 | % |
| Duty cycle | $RC_{SCDC}$ | 47 | | 52 | % |
| Peak-to-peak output period jitter | $RC_{SCPJIT}$ | | | 600 | ps |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{SCCJIT}$ | | | 172 | ps |
| Operating current ($V_{DD25}$) | $RC_{SCVPPA}$ | | | 599 | µA |

| Parameter | Modes [1] | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|---|
| Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks) | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 4.8 Gbps | | 300 | | 300 | MHz |
| | 20-bit, max data rate = 6.0 Gbps | | 300 | | 300 | MHz |
| | 32-bit, max data rate = 10.3125 Gbps | | 325 | | 325 | MHz |
| | 40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 260 | | 320 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 130 | | 160 | MHz |
| | Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | | 150 | | 150 | MHz |
| Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1) | | 225 | | 266 | MHz |
| | 20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1) | | 225 | | 266 | MHz |
| | 32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1) | | 225 | | 266 | MHz |
| | 40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1] | | 225 | | 266 | Mhz |
| | 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 130 | | 160 | MHz |
| Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1) | | 225 | | 266 | MHz |
| | 20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1) | | 225 | | 266 | MHz |
| | 32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1) | | 225 | | 266 | MHz |
| | 40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1] | | 225 | | 266 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 130 | | 160 | MHz |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

**Note**: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher $V_{CO}$ rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
   FTxRefClk = 75 MHz with typical settings.
   For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6). (see page 6)

### 7.4.6 Receiver Performance

The following table describes performance of the receiver.

**Table 53 • PolarFire Transceiver Receiver Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{IN}$ | 0 | | $V_{DDA}$ + 0.3 | V | |
| Differential peak-to-peak amplitude | $V_{IDPP}$ | 140 | | 1250 | mV | |
| Differential termination | $V_{ITERM}$ | | 85 | | Ω | |
| | $V_{ITERM}$ | | 100 | | Ω | |
| | $V_{ITERM}$ | | 150 | | Ω | |
| Common mode voltage | $V_{ICMDC}$ [1] | 0.7 × $V_{DDA}$ | | 0.9 × $V_{DDA}$ | V | DC coupled |
| Exit electrical idle detection time | $T_{EIDET}$ | | 50 | 100 | ns | |
| Run length of consecutive identical digits (CID) | $C_{ID}$ | | | 200 | UI | |
| CDR PPM tolerance[2] | $C_{DRPPM}$ | | | 1.15 | % UI | |
| CDR lock-to-data time | $T_{LTD}$ | | | | $CDR_{REFCLK}$ UI | |
| CDR lock-to-ref time | $T_{LTF}$ | | | | $CDR_{REFCLK}$ UI | |
| Loss-of-signal detect (Peak Detect Range setting = high)[9] | $V_{DETLHIGH}$ | | | | mV | Setting = 1 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 2 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 3 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 4 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 5 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 6 |
| | $V_{DETLHIGH}$ | | | | mV | Setting = 7 |
| Loss-of-signal detect (Peak Detect Range setting = low)[9] | $V_{DETLOW}$ | 65 | | 175 | mV | Setting = PCIe[3,7] |
| | $V_{DETLOW}$ | 95 | | 190 | mV | Setting = SATA[4,8] |
| | $V_{DETLOW}$ | 75 | | 170 | mV | Setting = 1 |
| | $V_{DETLOW}$ | 95 | | 185 | mV | Setting = 2 |
| | $V_{DETLOW}$ | 100 | | 190 | mV | Setting = 3 |
| | $V_{DETLOW}$ | 140 | | 210 | mV | Setting = 4 |
| | $V_{DETLOW}$ | 155 | | 240 | mV | Setting = 5 |
| | $V_{DETLOW}$ | 165 | | 245 | mV | Setting = 6 |
| | $V_{DETLOW}$ | 170 | | 250 | mV | Setting = 7 |
| Sinusoidal jitter tolerance | $T_{SJTOL}$ | | | | UI | >8.5 Gbps – 12.7 Gbps [5, 10] |

### 7.5.7 CPRI

The following table describes CPRI.

**Table 66 • CPRI**

| | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 0.6144 Gbps | | | UI |
| | 1.2288 Gbps | | | UI |
| | 2.4576 Gbps | | | UI |
| | 3.0720 Gbps | | | UI |
| | 4.9152 Gbps | | | UI |
| | 6.1440 Gbps | | | UI |
| | 9.8304 Gbps | | | UI |
| | 10.1376 Gbps | | | UI |
| | 12.16512 Gbps [1] | | | UI |
| Receive jitter tolerance | 0.6144 Gbps | | | UI |
| | 1.2288 Gbps | | | UI |
| | 2.4576 Gbps | | | UI |
| | 3.0720 Gbps | | | UI |
| | 4.9152 Gbps | | | UI |
| | 6.1440 Gbps | | | UI |
| | 9.8304 Gbps | | | UI |
| | 10.1376 Gbps | | | UI |
| | 12.16512 Gbps [1] | | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

### 7.5.8 JESD204B

The following table describes JESD204B.

**Table 67 • JESD204B**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 3.125 Gbps | | 0.35 | UI |
| | 6.25 Gbps | | 0.3 | UI |
| | 12.5 Gbps[1] | | | UI |
| Receive jitter tolerance | 3.125 Gbps | 0.56 | | UI |
| | 6.25 Gbps | 0.6 | | UI |
| | 12.5 Gbps[1] | | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

## 7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

### 7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

**Table 68 • FPGA Programming Cycles vs Retention Characteristics**

| Programming $T_J$ | Programming Cycles, Max | Retention Years | Retention Years at $T_J$ |
|---|---|---|---|
| 0 °C to 85 °C | 1000 | 20 | 85 °C |
| 0 °C to 100 °C | 500 | 20 | 100 °C |
| –20 °C to 100 °C | 500 | 20 | 100 °C |
| –40 °C to 100 °C | 500 | 20 | 100 °C |
| –40 °C to 85 °C | 1000 | 16 | 100 °C |
| –40 °C to 55 °C | 2000 | 12 | 100 °C |

**Note:** Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

### 7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

**Table 69 • Master SPI Programming Time (IAP)**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF100T, TL, TS, TLS | | | s |
| | | MPF200T, TL, TS, TLS | 17 | 25 | s |
| | | MPF300T, TL, TS, TLS | 26 | 32 | s |
| | | MPF500T, TL, TS, TLS | | | s |

**Table 70 • Slave SPI Programming Time**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF100T, TL, TS, TLS | | | s |
| | | MPF200T, TL, TS, TLS | 41[1] | | s |
| | | MPF300T, TL, TS, TLS | 50[1] | 60 | s |
| | | MPF500T, TL, TS, TLS | | | s |

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

**Table 71 • JTAG Programming Time**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF100T, TL, TS, TLS | | | s |
| | | MPF200T, TL, TS, TLS | | 56 | s |
| | | MPF300T, TL, TS, TLS[1] | | 95 | s |
| | | MPF500T, TL, TS, TLS | | | s |

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

### 7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

**Table 72 • Initialization Client Sizes**

| Device | Plaintext | Ciphertext |
|---|---|---|
| MPF100T, TL, TS, TLS | | |
| MPF200T, TL, TS, TLS | 2916 KB | 3006 KB |
| MPF300T, TL, TS, TLS | 4265 KB | 4403 KB |
| MPF500T, TL, TS, TLS | | |

**Note:** Worst case initializing all fabric LSRAM, USRAM, and UPROM.

**Table 73 • Bitstream Sizes**

| File | Devices | FPGA | Security | SNVM (all pages) | FPGA+ SNVM | FPGA+ Sec | SNVM+ Sec | FPGA+ SNVM+ Sec |
|---|---|---|---|---|---|---|---|---|
| SPI | MPF100T, TL, TS, TLS | | | | | | | |
| DAT | MPF100T, TL, TS, TLS | | | | | | | |
| SPI | MPF200T, TL, TS, TLS | 5.9 MB | 3.4 KB | 59.7 KB | 5.9 MB | 5.9 MB | 62.2 KB | 6.0 MB |
| DAT | MPF200T, TL, TS, TLS | 5.9 MB | 7.3 KB | 61.2 KB | 6.0 MB | 5.9 MB | 66.3 KB | 6.0 MB |
| SPI | MPF300T, TL, TS, TLS | 9.3 MB | 3.5 KB | 59.7 KB | 9.6 MB | 9.5 MB | 62.2 KB | 9.6 MB |
| DAT | MPF300T, TL, TS, TLS | 9.3 MB | 7.6 KB | 61.2 KB | 9.6 MB | 9.5 MB | 66.3 KB | 9.6 MB |
| SPI | MPF500T, TL, TS, TLS | | | | | | | |
| DAT | MPF500T, TL, TS, TLS | | | | | | | |

### 7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

**Table 74 • Maximum Number of Digest Cycles**

| | | Retention Since Programmed (N = Number Digests During that Time)[1] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Digest $T_J$ | Storage and Operating $T_J$ | N ≤300 | N = 500 | N = 1000 | N = 1500 | N = 2000 | N = 4000 | N = 6000 | Unit | Retention |
| –40 to 100 | –40 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| –40 to 100 | 0 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| –40 to 85 | –40 to 85 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 16 × LF | 8 × LF | 4 × LF | °C | Years |
| –40 to 55 | –40 to 55 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | °C | Years |

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | | | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | | | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | | | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | | | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1] | | | s | Full scrubbing |
| Time to verify[5] | | | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

## 7.6.7 Verify Time

The following tables describe verify time.

**Table 81 • Standalone Fabric Verify Times**

| Parameter | Devices | Max | Unit |
|---|---|---|---|
| Standalone verification over JTAG | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 53[1] | s |
| | MPF300T, TL, TS, TLS | 90[1] | s |
| | MPF500T, TL, TS, TLS | | s |
| Standalone verification over SPI | MPF100T, TL, TS, TLS | | s |
| | MPF200T, TL, TS, TLS | 37[2] | s |
| | MPF300T, TL, TS, TLS | 55[2] | s |
| | MPF500T, TL, TS, TLS | | s |

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.
2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. DirectC version 4.1.

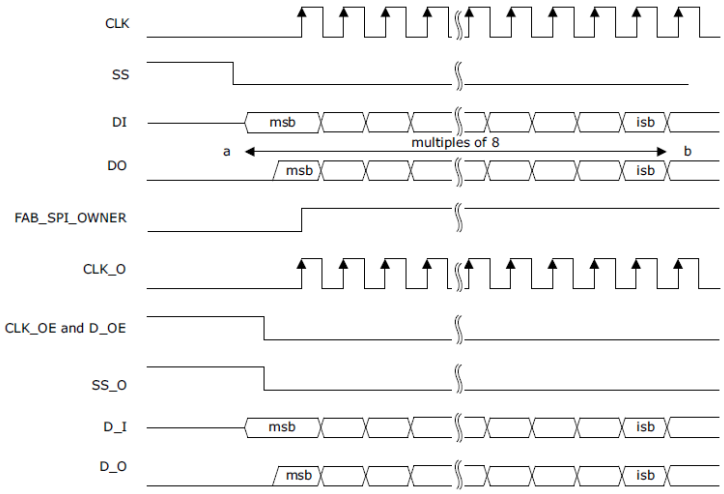
**Notes:**

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

**Table 82 • Verify Time by Programming Hardware**

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF100T, TL, TS, TLS | | | | | | |
| MPF200T, TL, TS, TLS | 9 | 67 | 53 | | | s |
| MPF300T, TL, TS, TLS | 14 | 95 | 90 | | | s |

**Figure 4 • USPI Switching Characteristics**




## 7.8.4 Tamper Detectors

The following section describes tamper detectors.

**Table 91 • ADC Conversion Rate**

| Parameter | Description | Min | Typ[1] | Max |
|---|---|---|---|---|
| $T_{CONV1}$ | Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0. | 420 µs | | 470 µs |
| $T_{CONVN}$ | Time between subsequent channel conversions. | | 480 µs | |
| $T_{SETUP}$ | Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs. | 0 ns | | |
| $T_{VALID}$[2] | Width of the valid pulse. | 1.625 µs | | 2 µs |
| $T_{RATE}$ | Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter. | 480 µs | Rate × 32 µs | 8128 µs |

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

**Note:** Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

**Table 92 • Temperature and Voltage Sensor Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Temperature sensing range | –40 | | 125 | °C | |
| Temperature sensing accuracy | –10 | | 10 | °C | |

**Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{MSCK}$ | | | 40 | MHz | |

**Table 108 • SPI Slave Mode (PolarFire Slave)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{SSCK}$ | | | 80 | MHz | |

### 7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

**Table 109 • SmartDebug Probe Performance Characteristics**

| Parameter | Symbol | $V_{DD}$ = 1.0 V STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|
| Maximum frequency of probe signal | $F_{MAX}$ | 100 | 100 | 100 | 100 | MHz |
| Minimum delay of probe signal | $T_{Min\_delay}$ | 13 | 12 | 13 | 12 | ns |
| Maximum delay of probe signal | $T_{Max\_delay}$ | 13 | 12 | 13 | 12 | ns |

### 7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

**Table 110 • DEVRST_N Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| DEVRST_N ramp rate | $DR_{RAMP}$ | | 10 | | µs | It must be a normal clean digital signal, with typical rise and fall times |
| DEVRST_N assert time | $DR_{ASSERT}$ | 1 | | | µs | The minimum time for DEVRST_N assertion to be recognized |
| DEVRST_N de-assert time | $DR_{DEASSERT}$ | 2.75 | | | ms | The minimum time DEVRST_N needs to be de-asserted before assertion |

### 7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

**Table 111 • FF_EXIT Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| FF_EXIT_N ramp rate | $FF_{RAMP}$ | | 10 | | µs | |
| Minimum FF_EXIT_N assert time | $FF_{ASSERT}$ | 1 | | | µs | The minimum time for FF_EXIT_N to be recognized |
| Minimum FF_EXIT_N de-assert time | $FF_{DEASSERT}$ | 170 | | | µs | The minimum time FF_EXIT_N needs to be de-asserted before assertion |

## 7.11 User Crypto

The following section describes user crypto.

### 7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

**Table 112 • TeraFire F5200B Switching Characteristics**

| Parameter | Symbol | VDD = 1.0 V STD | VDD = 1.0 V – 1 | VDD = 1.05 V STD | VDD = 1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Operating frequency | $F_{MAX}$ | 189 | | 189 | | MHz | –40 °C to 100 °C |

### 7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

**Note:** Throughput cycle count collected with Athena TeraFire Core and RISCV running at 100 MHz.

**Table 113 • AES**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-ECB-128 encrypt[1] | 128 | 515 | 1095 |
| | 64K | 50157 | 933 |
| AES-ECB-128 decrypt[1] | 128 | 557 | 1760 |
| | 64K | 48385 | 1524 |
| AES-ECB-256 encrypt[1] | 128 | 531 | 1203 |
| | 64K | 58349 | 1203 |
| AES-ECB-256 decrypt[1] | 128 | 589 | 1676 |
| | 64K | 56673 | 1671 |
| AES-CBC-256 encrypt[1] | 128 | 576 | 1169 |
| | 64K | 52547 | 1169 |
| AES-CBC-256 decrypt[1] | 128 | 585 | 1744 |
| | 64K | 48565 | 1652 |
| AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1925 | 2740 |
| | 64K | 60070 | 2158 |
| AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1973 | 2268 |
| | 64K | 60102 | 2151 |

1. With DPA counter measures.

**Table 114 • GMAC**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-GCM-256[1], 128-bit tag, (message is only authenticated) | 128 | 1863 | 2211 |
| | 64K | 49707 | 2128 |

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