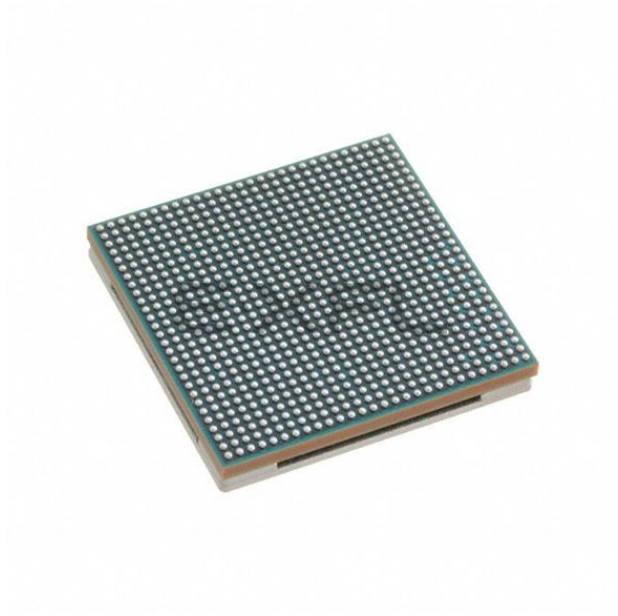

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 481000 |
| Total RAM Bits | 33792000 |
| Number of I/O | 388 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.08V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 784-BBGA, FCBGA |
| Supplier Device Package | 784-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/mpf500tl-fcg784e |

# Contents

# 2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (–40 °C to 100 °C $T_J$) and extended commercial temperature range (0 °C to 100 °C $T_J$). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply $V_{DD}$ can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply $V_{DDA}$ can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

# 5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

**Table 2 • PolarFire FPGA Silicon Status**

| Device | Silicon Status |
|---|---|
| MPF100T, TL, TS, TLS | Preliminary |
| MPF200T, TL, TS, TLS | Preliminary |
| MPF300T, TL, TS, TLS | Preliminary |
| MPF500T, TL, TS, TLS | Preliminary |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transceiver TX and RX lanes supply at 1.05 V mode (when any lane rate is greater than 10.3125 Gbps)[1] | $V_{DDA}$ | 1.02 | 1.05 | 1.08 | V |
| Programming and HSIO receiver supply | $V_{DD18}$ | 1.71 | 1.80 | 1.89 | V |
| FPGA core and FPGA PLL high-voltage supply | $V_{DD25}$ | 2.425 | 2.50 | 2.575 | V |
| Transceiver PLL high-voltage supply | $V_{DDA25}$ | 2.425 | 2.50 | 2.575 | V |
| Transceiver reference clock supply –3.3 V nominal | $V_{DD\_XCVR\_CLK}$ | 3.135 | 3.3 | 3.465 | V |
| Transceiver reference clock supply –2.5 V nominal | $V_{DD\_XCVR\_CLK}$ | 2.375 | 2.5 | 2.625 | V |
| Global $V_{REF}$ for transceiver reference clocks[3] | $XCVR_{VREF}$ | Ground | | $V_{DD\_XCVR\_CLK}$ | V |
| HSIO DC I/O supply. Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V[4] | $V_{DDIx}$ | 1.14 | Various | 1.89 | V |
| GPIO DC I/O supply. Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V[2,4] | $V_{DDIx}$ | 1.14 | Various | 3.465 | V |
| Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3). Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V | $V_{DDI3}$ | 1.71 | Various | 3.465 | V |
| GPIO auxiliary supply for I/O bank x with $V_{DDIx}$ = 3.3 V nominal[2,4] | $V_{DDAUXx}$ | 3.135 | 3.3 | 3.465 | V |
| GPIO auxiliary supply for I/O bank x with $V_{DDIx}$ = 2.5 V nominal or lower[2,4] | $V_{DDAUXx}$ | 2.375 | 2.5 | 2.625 | V |
| Extended commercial temperature range | $T_J$ | 0 | | 100 | °C |
| Industrial temperature range | $T_J$ | –40 | | 100 | °C |
| Extended commercial programming temperature range | $T_{PRG}$ | 0 | | 100 | °C |
| Industrial programming temperature range | $T_{PRG}$ | –40 | | 100 | °C |

1. $V_{DD}$ and $V_{DDA}$ can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if $V_{DDIx}$ is 2.5 V nominal or 3.3 V nominal, $V_{DDAUXx}$ must be connected to the $V_{DDIx}$ supply for that bank. If $V_{DDIx}$ for a given GPIO bank is <2.5 V nominal, $V_{DDAUXx}$ per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}$/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage ($V_{IN}$) overshoot duration for HSIO.

**Table 6 • Maximum Overshoot During Transitions for HSIO**

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 1.8 |
| 100 | 1.85 |
| 100 | 1.9 |
| 100 | 1.95 |
| 100 | 2 |
| 100 | 2.05 |
| 100 | 2.1 |
| 100 | 2.15 |
| 100 | 2.2 |
| 90 | 2.25 |
| 30 | 2.3 |
| 7.5 | 2.35 |
| 1.9 | 2.4 |

**Note:** Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage ($V_{IN}$) undershoot duration for HSIO.

**Table 7 • Maximum Undershoot During Transitions for HSIO**

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | –0.05 |
| 100 | –0.1 |
| 100 | –0.15 |
| 100 | –0.2 |
| 100 | –0.25 |
| 100 | –0.3 |
| 100 | –0.35 |
| 100 | –0.4 |
| 44 | –0.45 |
| 14 | –0.5 |
| 4.8 | –0.55 |
| 1.6 | –0.6 |

The following table shows the maximum AC input voltage ($V_{IN}$) overshoot duration for GPIO.

**Note**: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N. Weak pull-up (as specified in GPIO) is always enabled.

## 6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

### 6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

**Table 12 • DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$[1] Max (V) |
|---|---|---|---|---|---|---|---|
| PCI | 3.15 | 3.3 | 3.45 | –0.3 | 0.3 × $V_{DDI}$ | 0.5 × $V_{DDI}$ | 3.45 |
| LVTTL | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 2.625 |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.89 |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.575 |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.26 |
| SSTL25I[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL25II[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL18I[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL18II[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| SSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

**Table 19 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 34 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 48 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 80 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 80% of $V_{DDI}$.

**Table 20 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 50% of $V_{DDI}$.

### 6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

**Table 21 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank**

| Parameter | Description | Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination[1] | Internal differential termination | –20 | 100 | 20 | Ω | $V_{ICM}$ < 0.8 V |
| | | –20 | 100 | 40 | Ω | 0.6 V < $V_{ICM}$ < 1.65 V |
| | | –20 | 100 | 80 | Ω | 1.4 V < $V_{ICM}$ |
| Single-ended thevenin termination[2, 3] | Internal parallel thevenin termination | –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| | | –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V |

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSUL18I | HSUL 1.8 V Class I | $V_{REF}$ – 0.54 | $V_{REF}$ + 0.54 | | | $V_{REF}$ | 0.90 | V |
| HSUL18II | HSUL 1.8 V Class II | $V_{REF}$ – 0.54 | $V_{REF}$ + 0.54 | | | $V_{REF}$ | 0.90 | V |
| HSUL12 | HSUL 1.2 V | $V_{REF}$ – .22 | $V_{REF}$ + .22 | | | $V_{REF}$ | 0.60 | V |
| POD12I | Pseudo open drain (POD) logic 1.2 V Class I | $V_{REF}$ – .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| POD12II | POD 1.2 V Class II | $V_{REF}$ – .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| LVDS33 | Low-voltage differential signaling (LVDS) 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS25 | LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS18 | LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| RSDS33 | RSDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS25 | RSDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS18 | RSDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS33 | Mini-LVDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS25 | Mini-LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS18 | Mini-LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| SUBLVDS33 | Sub-LVDS 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS25 | Sub-LVDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS18 | Sub-LVDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| PPDS33 | Point-to-point differential signaling 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS25 | PPDS 2.5 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS18 | PPDS 1.8 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| SLVS33 | Scalable low-voltage signaling 3.3 V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | | V |

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL18I | SSTL 1.8 V Class I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL18II | SSTL 1.8 V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL15I | SSTL 1.5 V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL15II | SSTL 1.5 V Class II | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL135I | SSTL 1.35 V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL135II | SSTL 1.35 V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL15I | High-speed transceiver logic (HSTL) 1.5 V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL15II | HSTL 1.5 V Class II | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL135I | HSTL 1.35 V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL135II | HSTL 1.35 V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL12 | HSTL 1.2 V | 50 | 0 | $V_{REF}$ | 0.6 |
| HSUL18I | High-speed unterminated logic 1.8 V Class I | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL18II | HSUL 1.8 V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL12 | HSUL 1.2 V | 50 | 0 | $V_{REF}$ | 0.6 |
| POD12I | Pseudo open drain (POD) logic 1.2 V Class I | 50 | 0 | $V_{REF}$ | 0.84 |
| POD12II | POD 1.2 V Class II | 50 | 0 | $V_{REF}$ | 0.84 |
| LVDS33 | LVDS 3.3 V | 100 | 0 | 0[1] | 0 |
| LVDS25 | LVDS 2.5 V | 100 | 0 | 0[1] | 0 |
| LVDS18 | LVDS 1.8 V | 100 | 0 | 0[1] | 0 |
| RSDS33 | Reduced swing differential signaling 3.3 V | 100 | 0 | 0[1] | 0 |
| RSDS25 | RSDS 2.5 V | 100 | 0 | 0[1] | 0 |
| RSDS18 | RSDS 1.8 V | 100 | 0 | 0[1] | 0 |
| MINILVDS33 | Mini-LVDS 3.3 V | 100 | 0 | 0[1] | 0 |
| MINILVDS25 | Mini-LVDS 2.5 V | 100 | 0 | 0[1] | 0 |
| SUBLVDS33 | Sub-LVDS 3.3 V | 100 | 0 | 0[1] | 0 |
| SUBLVDS25 | Sub-LVDS 2.5 V | 100 | 0 | 0[1] | 0 |
| PPDS33 | Point-to-point differential signaling 3.3 V | 100 | 0 | 0[1] | 0 |
| PPDS25 | PPDS 2.5 V | 100 | 0 | 0[1] | 0 |
| BUSLVDSE25 | Bus LVDS | 100 | 0 | 0[1] | 0 |
| MLVDSE25 | Multipoint LVDS 2.5 V | 100 | 0 | 0[1] | 0 |
| LVPECLE33 | Low-voltage positive emitter-coupled logic | 100 | 0 | 0[1] | 0 |
| MIPIE25 | Mobile industry processor interface 2.5 V | 100 | 0 | 0[1] | 0 |

1. The value given is the differential output voltage.

| Standard | STD | –1 | Unit |
|---|---|---|---|
| HSTL15I | 900 | 1100 | Mbps |
| HSTL15II | 900 | 1100 | Mbps |
| HSTL135I | 1066 | 1066 | Mbps |
| HSTL135II | 1066 | 1066 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL12 | 1066 | 1333 | Mbps |
| HSTL12 | 1066 | 1266 | Mbps |
| POD12I | 1333 | 1600 | Mbps |
| POD12II | 1333 | 1600 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 300 | 300 | Mbps |

1. Performance is achieved with $V_{ID}$ ≥200 mV.

### Table 25 • GPIO Maximum Input Buffer Speed

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS25/LVDS33/LCMDS25/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25/RSDS33 | 800 | 800 | Mbps |
| MINILVDS25/MINILVDS33 | 800 | 800 | Mbps |
| SUBLVDS25/SUBLVDS33 | 800 | 800 | Mbps |
| PPDS25/PPDS33 | 800 | 800 | Mbps |
| SLVS25/SLVS33 | 800 | 800 | Mbps |
| SLVSE15 | 800 | 800 | Mbps |
| HCSL25/HCSL33 | 800 | 800 | Mbps |
| BUSLVDSE25 | 800 | 800 | Mbps |
| MLVDSE25 | 800 | 800 | Mbps |
| LVPECL33 | 800 | 800 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| HSTL15I | 800 | 900 | Mbps |
| HSTL15II | 800 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS25 (16 mA) | 500 | 500 | Mbps |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|---|---|
| FMAX 4:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_B_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 8:1 | RX_DDRX_B_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 2:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 4:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 8:1 | RX_DDRX_BL_A | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| FMAX 2:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |
| FMAX 4:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|---|---|
| FMAX 8:1 | RX_DDRX_BL_C | Rx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, centered |

**Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|---|---|
| Output FMAX | TX_SDR_G_A | Tx SDR | | | | | | | MHz | From a global clock source, aligned[1] |
| | TX_SDR_G_C | Tx SDR | | | | | | | MHz | From a global clock source, centered[1] |

1. A centered clock-to-data interface can be created with a negedge launch of the data.

**Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|---|---|
| Output FMAX | TX_DDR_G_A | Tx DDR | | | 335 | | | 335 | MHz | From a global clock source, aligned |
| | TX_DDR_G_C | Tx DDR | | | 335 | | | 335 | MHz | From a global clock source, centered |
| | TX_DDR_L_A | Tx DDR | | | 250 | | | 250 | MHz | From a lane clock source, aligned |
| | TX_DDR_L_C | Tx DDR | | | 250 | | | 250 | MHz | From a lane clock source, centered |
| Output FMAX 2:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| Output FMAX 4:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |
| Output FMAX 8:1 | TX_DDRX_B_A | Tx DDR digital mode | | | | | | | MHz | From a HS_IO_CLK clock source, aligned |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Maximum input period clock jitter (reference and feedback clocks)[2] | $F_{MAXINJ}$ | | 120 | 1000 | ps |
| PLL VCO frequency | $F_{VCO}$ | 800 | | 5000 | MHz |
| Loop bandwidth (Int)[3] | $F_{BW}$ | $F_{PHDET}$/55 | $F_{PHDET}$/44 | $F_{PHDET}$/30 | MHz |
| Loop bandwidth (FRAC)[3] | $F_{BW}$ | $F_{PHDET}$/91 | $F_{PHDET}$/77 | $F_{PHDET}$/56 | MHz |
| Static phase offset of the PLL outputs[4] | $T_{SPO}$ | | | Max (±60 ps, ±0.5 degrees) | ps |
| | $T_{OUTJITTER}$ | | | | ps |
| PLL output duty cycle precision | $T_{OUTDUTY}$ | 48 | | 54 | % |
| PLL lock time[5] | $T_{LOCK}$ | | | Max (6.0 µs, 625 PFD cycles) | µs |
| PLL unlock time[6] | $T_{UNLOCK}$ | 2 | | 8 | PFD cycles |
| PLL output frequency | $F_{OUT}$ | 0.050 | | 1250 | MHz |
| Minimum reset pulse width | $T_{MRPW}$ | | | | µs |
| Maximum delay in the feedback path[7] | $F_{MAXDFB}$ | | | 1.5 | PFD cycles |
| Spread spectrum modulation spread[8] | Mod_Spread | 0.1 | | 3.1 | % |
| Spread spectrum modulation frequency[9] | Mod_Freq | $F_{PHDETF}$/(128x63) | 32 | $F_{PHDETF}$/(128) | KHz |

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/$F_{REF}$. For example, $F_{REF}$ = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

**Note**: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

### 7.2.3 DLL

The following table provides information about DLL.

**Table 38 • DLL Electrical Characteristics**

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input reference clock frequency | $F_{INF}$ | 133 | | 800 | MHz |
| Input feedback clock frequency | $F_{INFDBF}$ | 133 | | 800 | MHz |
| Primary output clock frequency | $F_{OUTPF}$ | 133 | | 800 | MHz |

## 7.3 Fabric Specifications

The following section describes specifications for the fabric.

### 7.3.1 Math Blocks

The following tables describe math block performance.

**Table 41 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)**

| Parameter | Symbol | Modes | $V_{DD}$ = 1.0 V – STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V – STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|---|
| Maximum operating frequency | $F_{MAX}$ | 18 × 18 multiplication | 370 | 470 | 440 | 500 | MHz |
| | | 18 × 18 multiplication summed with 48-bit input | 370 | 470 | 440 | 500 | MHz |
| | | 18 × 19 multiplier pre-adder ROM mode | 365 | 465 | 435 | 500 | MHz |
| | | Two 9 × 9 multiplication | 370 | 470 | 440 | 500 | MHz |
| | | 9 × 9 dot product (DOTP) | 370 | 470 | 440 | 500 | MHz |
| | | Complex 18 × 19 multiplication | 360 | 455 | 430 | 500 | MHz |

**Table 42 • Math Block Performance Industrial Range (–40 °C to 100 °C)**

| Parameter | Symbol | Modes | $V_{DD}$ = 1.0 V – STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V – STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|---|
| Maximum operating frequency | $F_{MAX}$ | 18 × 18 multiplication | 365 | 465 | 435 | 500 | MHz |
| | | 18 × 18 multiplication summed with 48-bit input | 365 | 465 | 435 | 500 | MHz |
| | | 18 × 19 multiplier pre-adder ROM mode | 355 | 460 | 430 | 500 | MHz |
| | | Two 9 × 9 multiplication | 365 | 465 | 435 | 500 | MHz |
| | | 9 × 9 DOTP | 365 | 465 | 435 | 500 | MHz |
| | | Complex 18 × 19 multiplication | 350 | 450 | 425 | 500 | MHz |

### 7.5.7 CPRI

The following table describes CPRI.

**Table 66 • CPRI**

| | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 0.6144 Gbps | | | UI |
| | 1.2288 Gbps | | | UI |
| | 2.4576 Gbps | | | UI |
| | 3.0720 Gbps | | | UI |
| | 4.9152 Gbps | | | UI |
| | 6.1440 Gbps | | | UI |
| | 9.8304 Gbps | | | UI |
| | 10.1376 Gbps | | | UI |
| | 12.16512 Gbps [1] | | | UI |
| Receive jitter tolerance | 0.6144 Gbps | | | UI |
| | 1.2288 Gbps | | | UI |
| | 2.4576 Gbps | | | UI |
| | 3.0720 Gbps | | | UI |
| | 4.9152 Gbps | | | UI |
| | 6.1440 Gbps | | | UI |
| | 9.8304 Gbps | | | UI |
| | 10.1376 Gbps | | | UI |
| | 12.16512 Gbps [1] | | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

### 7.5.8 JESD204B

The following table describes JESD204B.

**Table 67 • JESD204B**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 3.125 Gbps | | 0.35 | UI |
| | 6.25 Gbps | | 0.3 | UI |
| | 12.5 Gbps[1] | | | UI |
| Receive jitter tolerance | 3.125 Gbps | 0.56 | | UI |
| | 6.25 Gbps | 0.6 | | UI |
| | 12.5 Gbps[1] | | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

## 7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

**Table 75 • FPGA Programming Cycles Lifetime Factor**

| Programming $T_J$ | Programming Cycles | LF |
|---|---|---|
| –40 °C to 100 °C | 500 | 1 |
| –40 °C to 85 °C | 1000 | 0.8 |
| –40 °C to 55 °C | 2000 | 0.6 |

**Notes:**

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures ($T_J$).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C $T_J$. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

### 7.6.5 Digest Time

The following table describes digest time.

**Table 76 • Digest Times**

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| Setup time | All | 2 | | µs |
| Fabric digest run time | MPF100T, TL, TS, TLS | | | ms |
| | MPF200T, TL, TS, TLS | 1005 | 1072 | ms |
| | MPF300T, TL, TS, TLS | 1503.9 | 1582 | ms |
| | MPF500T, TL, TS, TLS | | | ms |
| UFS CC digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 33.2 | 35 | µs |
| | MPF300T, TL, TS, TLS | 33.2 | 35 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| sNVM digest run time[1] | MPF100T, TL, TS, TLS | | | ms |
| | MPF200T, TL, TS, TLS | 4.4 | 4.8 | ms |
| | MPF300T, TL, TS, TLS | 4.4 | 4.8 | ms |
| | MPF500T, TL, TS, TLS | | | ms |
| UFS UL digest run time | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 46.6 | 48.8 | µs |
| | MPF300T, TL, TS, TLS | 46.6 | 48.8 | µs |
| | MPF500T, TL, TS, TLS | | | µs |
| User key digest run time[2] | MPF100T, TL, TS, TLS | | | µs |
| | MPF200T, TL, TS, TLS | 525.4 | 543.3 | µs |
| | MPF300T, TL, TS, TLS | 525.4 | 543.3 | µs |
| | MPF500T, TL, TS, TLS | | | µs |

**Table 104 • Flash*Freeze**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| The time from Flash*Freeze entry command to the Flash*Freeze state | $T_{FF\_ENTRY}$ | | 59 | | µs | |
| The time from Flash*Freeze exit pin assertion to fabric operational state | $T_{FF\_FABRIC\_UP}$ | | 133 | | µs | |
| The time from Flash*Freeze exit pin assertion to I/Os operational | $T_{FF\_IO\_ACTIVE}$ | | 143 | | µs | |

## 7.10 Dedicated Pins

The following section describes the dedicated pins.

### 7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

**Table 105 • JTAG Electrical Characteristics**

| Symbol | Description | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $T_{DISU}$ | TDI input setup time | 0.0 | | | ns | |
| $T_{DIHD}$ | TDI input hold time | 2.0 | | | ns | |
| $T_{TMSSU}$ | TMS input setup time | 1.5 | | | ns | |
| $T_{TMSHD}$ | TMS input hold time | 1.5 | | | ns | |
| $F_{TCK}$ | TCK frequency | | | 25 | MHz | |
| $T_{TCKDC}$ | TCK duty cycle | 40 | | 60 | % | |
| $T_{TDOCQ}$ | TDO clock to Q out | | | 8.4 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBCQ}$ | TRSTB clock to Q out | | | 23.5 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBPW}$ | TRSTB min pulse width | 50 | | | ns | |
| $T_{RSTBREM}$ | TRSTB removal time | 0.0 | | | ns | |
| $T_{RSTBREC}$ | TRSTB recovery time | 12.0 | | | ns | |
| $CIN_{TDI}$ | TDI input pin capacitance | | | 5.3 | pf | |
| $CIN_{TMS}$ | TMS input pin capacitance | | | 5.3 | pf | |
| $CIN_{TCK}$ | TCK input pin capacitance | | | 5.3 | pf | |
| $CIN_{TRSTB}$ | TRSTB input pin capacitance | | | 5.3 | pf | |

### 7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

**Table 106 • SPI Master Mode (PolarFire Master) During Programming**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{MSCK}$ | | | 20 | MHz | |

**Table 107 • SPI Master Mode (PolarFire Master) During Device Initialization**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{MSCK}$ | | | 40 | MHz | |

**Table 108 • SPI Slave Mode (PolarFire Slave)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{SSCK}$ | | | 80 | MHz | |

### 7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

**Table 109 • SmartDebug Probe Performance Characteristics**

| Parameter | Symbol | $V_{DD}$ = 1.0 V STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|
| Maximum frequency of probe signal | $F_{MAX}$ | 100 | 100 | 100 | 100 | MHz |
| Minimum delay of probe signal | $T_{Min\_delay}$ | 13 | 12 | 13 | 12 | ns |
| Maximum delay of probe signal | $T_{Max\_delay}$ | 13 | 12 | 13 | 12 | ns |

### 7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

**Table 110 • DEVRST_N Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| DEVRST_N ramp rate | $DR_{RAMP}$ | | 10 | | µs | It must be a normal clean digital signal, with typical rise and fall times |
| DEVRST_N assert time | $DR_{ASSERT}$ | 1 | | | µs | The minimum time for DEVRST_N assertion to be recognized |
| DEVRST_N de-assert time | $DR_{DEASSERT}$ | 2.75 | | | ms | The minimum time DEVRST_N needs to be de-asserted before assertion |

### 7.10.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

**Table 111 • FF_EXIT Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| FF_EXIT_N ramp rate | $FF_{RAMP}$ | | 10 | | µs | |
| Minimum FF_EXIT_N assert time | $FF_{ASSERT}$ | 1 | | | µs | The minimum time for FF_EXIT_N to be recognized |
| Minimum FF_EXIT_N de-assert time | $FF_{DEASSERT}$ | 170 | | | µs | The minimum time FF_EXIT_N needs to be de-asserted before assertion |

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