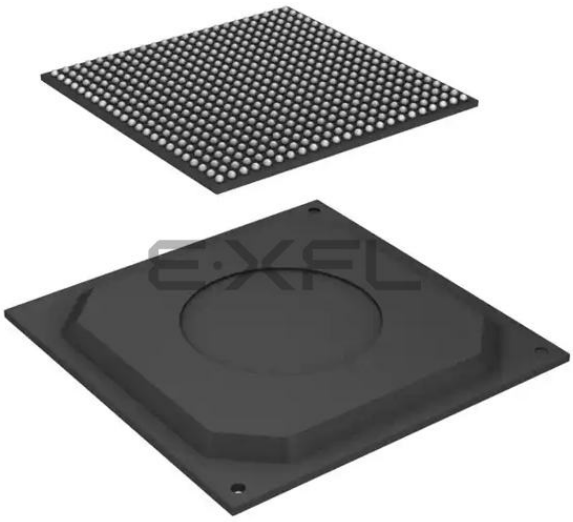

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx534avv8b

1.1 Functional Part Differences and Ordering Information

Table 1shows the functional differences between the different parts in the i.MX53 family.

Table 1. i.MX53 Parts Functional Differences

Feature	i.MX534	i.MX536
Example Applications	Clusters	Video and Navigation
Core	800 MHz ARM Cortex™-A8	ARM 800 MHz Cortex™-A8
Memory	2 GB, x32 LPDDR2/DDR2/DDR3	2 GB, x32 LPDDR2/DDR2/DDR3
Video Decode	no HW acceleration	Hardware (1080p30)
Video Encode	no HW acceleration	Hardware (720p30)
3D GPU	OpenGL/ES 2.0	OpenGL/ES 2.0
	33 Mtri/s, 200 Mpix/s	33 Mtri/s, 200 Mpix/s
2D GPU	OpenVG 1.1, 200 Mpix/s	OpenVG 1.1, 200 Mpix/s
LCD IF	Parallel, LVDS	Parallel, LVDS
Video Out	VGA HD1080p60	VGA HD1080p60
Camera I/F	2x 20-bit Parallel	2x 20-bit Parallel
Ethernet	10/100, IEEE1588	10/100, IEEE1588
SATA	S-ATA II 1.5 Gbps	S-ATA II 1.5 Gbps
CAN	2 x FlexCAN	2 x FlexCAN
MLB	MLB50	MLB50
USB	Four HS USB2.0: 1xHS OTG + PHY 1xHost + PHY 2xHost + ULPI/IC-USB	Four HS USB2.0: 1xHS OTG + PHY 1xHost + PHY 2xHost + ULPI/IC-USB
SDIO I/F	3x SD/MMC 4.3 1x SD/MMC 4.4	3x SD/MMC 4.3 1x SD/MMC 4.4
SPI I/F	3x SPI	3x SPI
I2C I/F	3x I2C	3x I2C
Other	5x UART, P-ATA, 3x I2S, S/PDIF Tx/Rx, ESAI	5x UART, P-ATA, 3x I2S, S/PDIF Tx/Rx, ESAI
Package	19x19 0.8P TE-BGA	19x19 0.8P TE-BGA
Qual.	Automotive AEC-Q100	Automotive AEC-Q100

  - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4).
- USB
  - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high-speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Automotive environment interfaces:
  - Two controller area network (FlexCAN) interfaces, 1 Mbps each
  - Media local bus or MediaLB (MLB) provides interface to most networks (50 Mbps)
  - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
  - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
  - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
  - Three I^2C ports, supporting 400 kbps
  - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
  - Sony Phillips Digital Interface (SPDIF), Rx and Tx
  - Key pad port (KPP)
  - Two pulse-width modulators (PWM)
  - GPIO with interrupt capabilities

The system supports efficient and smart power control and clocking:

- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware/features:

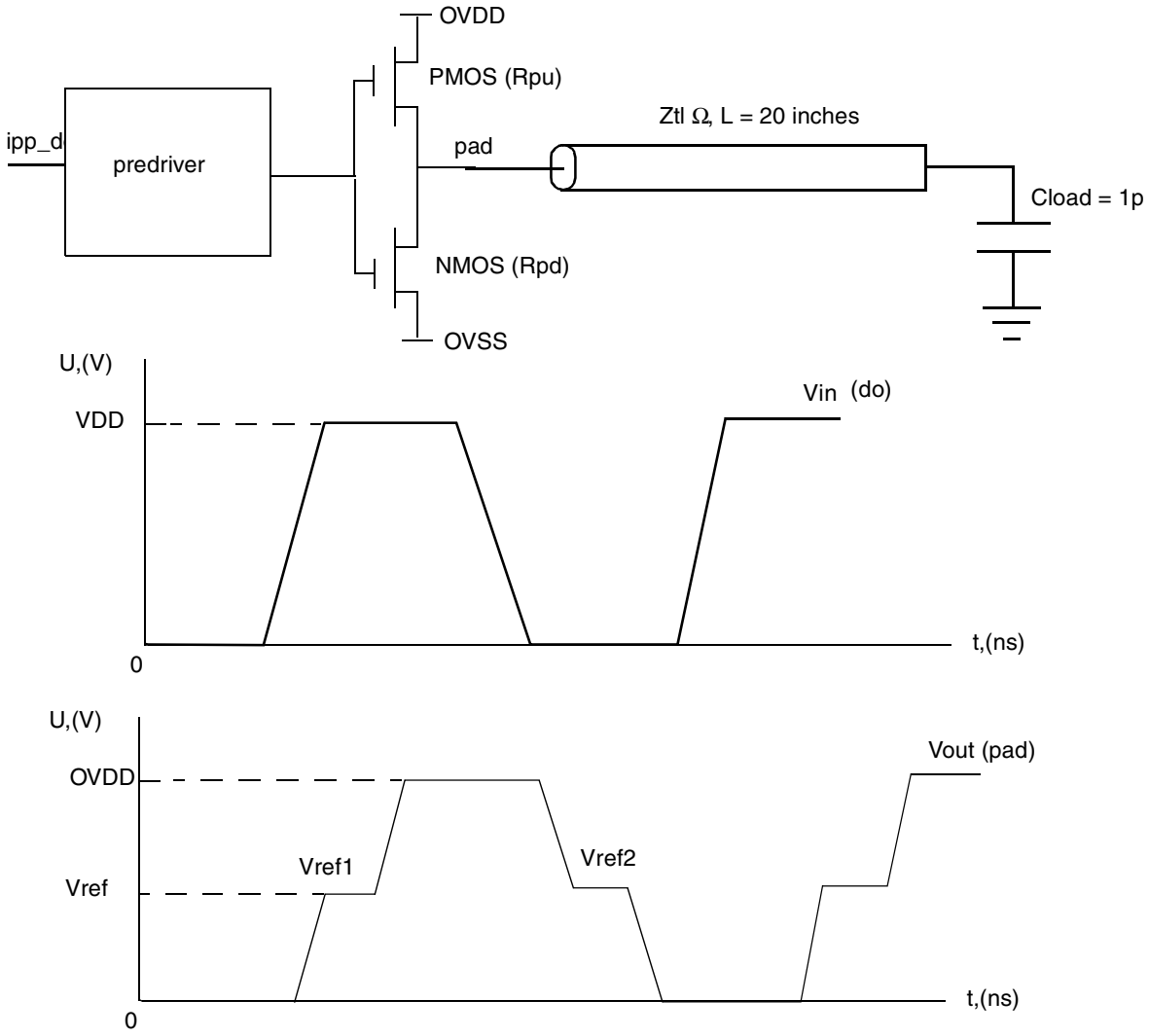
- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches

3 Modules List

The i.MX53xA processor contains a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX53xA Digital and Analog Blocks

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Cortex™ A8 platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Multiplexer	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1 CAMP-2	Clock Amplifier	Clocks, Resets, and Power Control	Clock amplifier
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs.
CSPI ECSPI-1 ECSPI-2	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals.
CSU	Central Security Unit	Security	The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53xA platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing.



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 4. Impedance Matching Load for Measurement

Table 25. LPDDR2 I/O DDR3 mode AC Characteristics[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate	tsr	At 25 Ω to Vref	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 266 MHz clk = 400 MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 x OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

4.5.3 LVIO I/O AC Electrical Characteristics

AC electrical characteristics for LVIO I/O in slow and fast modes are presented in the Table 26 and Table 27, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 26. LVIO I/O AC Parameters in Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 33 shows the electrical parameters of CAMP.

Table 33. CAMP Electrical Parameters (CKIH1, CKIH2)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)[1]	NVCC_CKIH - 0.25	—	NVCC_CKIH	V
Sinusoidal input amplitude	0.4	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 NVCC_CKIH is the supply voltage of CAMP.

4.6.4 DPLL Electrical Parameters

Table 34 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 34. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	-67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output Duty Cycle	—	48.5	50	51.5	%
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz at avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz at avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 33.

2 The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user. Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15. Therefore, if the MFI value is 15, MFN value must be zero.

4.6.6.3 General EIM Timing-Synchronous Mode

Figure 16, Figure 17, and Table 39 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

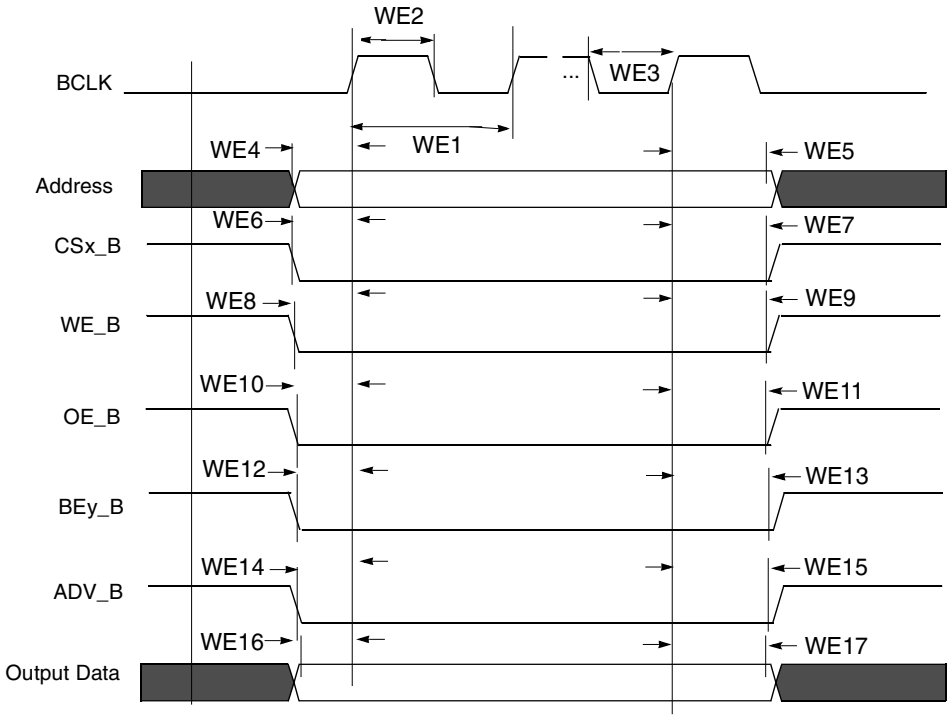


Figure 16. EIM Outputs Timing Diagram

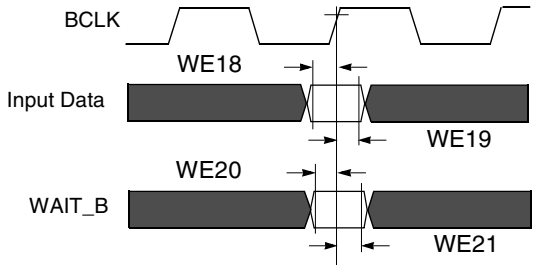


Figure 17. EIM Inputs Timing Diagram

Table 39. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t		2 x t		3 x t		4 x t	
WE2	BCLK Low Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	

4.7.2.3 ECSPI Master Mode Timing

Figure 32 depicts the timing of ECSPI in master mode. Table 47 lists the ECSPI master mode timing characteristics.

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time—Read SCLK Cycle Time—Write	t_{clk}	30 15	—	ns
CS2	SCLK High or Low Time—Read SCLK High or Low Time—Write	t_{SW}	14 7	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2.5	ns
CS8	MISO Setup Time	t_{Smiso}	8.5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, “I/O AC Parameters”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.4 ECSPI Slave Mode Timing

Figure 33 depicts the timing of ECSPI in slave mode. Table 48 lists the ECSPI slave mode timing characteristics.

Table 48. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	15 40	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	7 20	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

Table 49. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
80	SCKT rising edge to FST out (wr) high[6]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [77]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 VCORE_VDD= 1.00 ± 0.10V
Tj = -40 °C to 125 °C
CL= 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

Table 51. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD3	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	eSDHC Input Hold Time	t_{IH}	2.5	—	ns

4.7.5 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the MII pins), for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see the i.MX53 Reference Manual.

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.7.5.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 52 lists the MII receive channel signal timing parameters and Figure 38 shows MII receive signal timings.

Table 52. MII Receive Signal Timing

No.	Characteristics[1] [2]	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

1 FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

2 Test conditions: 25pF on each output signal.

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.7.8.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 58 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 58. Camera Input Signal Cross Reference, Format and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] CSIx stands for CSI1 or CSI2.

Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(\text{floor}\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

ATA Interface Signals

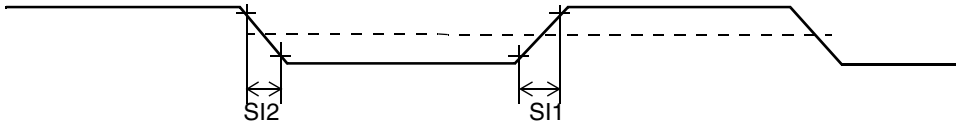


Figure 65. PATA Interface Signals Timing Diagram

Table 72. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface[1]	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15—40 pF where all signals have the same capacitive load value.

The user must use level shifters for 5.0 V compatibility on the ATA interface. The i.MX53xA PATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX53xA PATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 73 shows ATA timing parameters.

Table 76. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 68 (Read), Figure 69 (Write)	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = time_jn x T - (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T - tskew1 toff = time_off × T - tskew1	—

1 tk1 in the MDMA figures (**Figure 68** and **Figure 69**) equals (tk - 2 x T).

2 tk1 in the MDMA figures equals (tk – 2 x T).

4.7.13.2 Ultra DMA (UDMA) Input Timing

Figure 70 shows timing when the UDMA in transfer starts, Figure 71 shows timing when the UDMA in host terminates transfer, Figure 72 shows timing when the UDMA in device terminates transfer, and Table 77 lists the timing parameters for UDMA in burst.

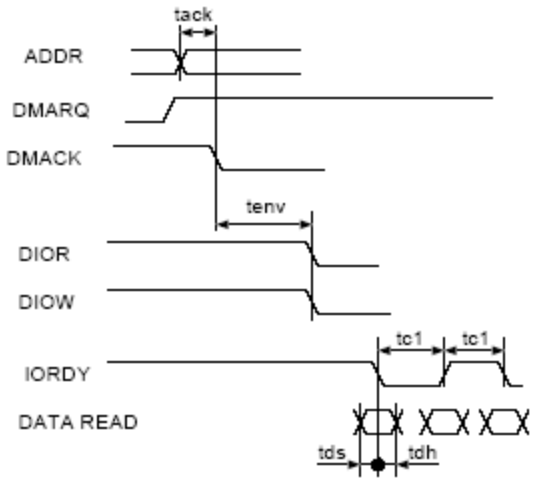


Figure 70. UDMA in Transfer Starts Timing Diagram

4.7.17.4 SSI Receiver Timing with External Clock

Figure 86 depicts the SSI receiver external clock timing and Table 88 lists the timing parameters for the receiver timing with the external clock.

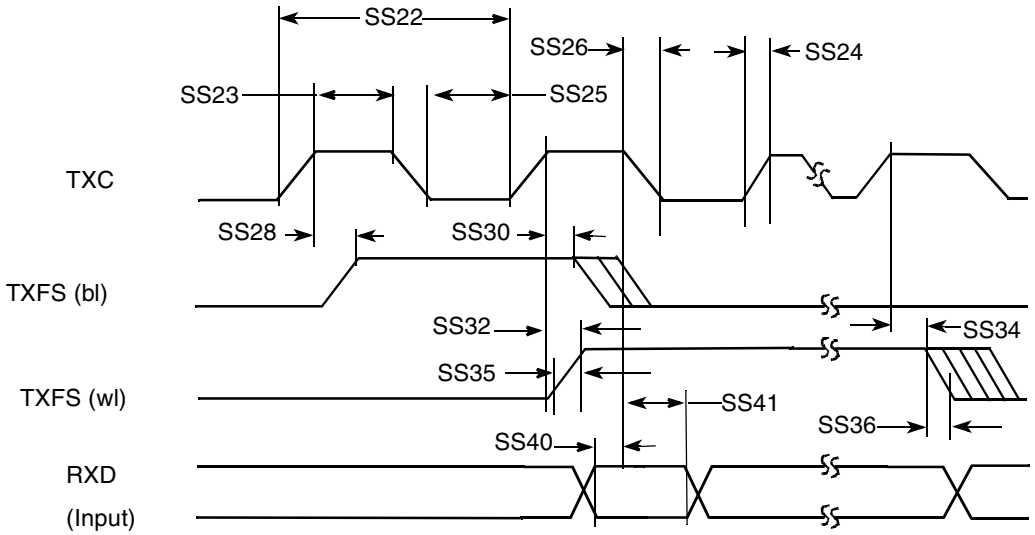


Figure 86. SSI Receiver External Clock Timing Diagram

Table 88. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	-10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

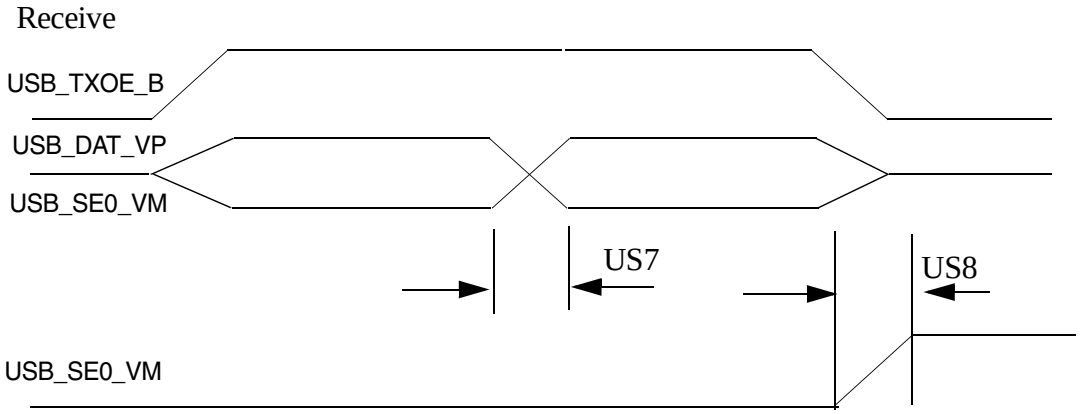


Figure 92. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 95. Definitions of USB Waveform in DAT_SE0 Bi — Directional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions / Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_WAIT	AB9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_WAIT	Output	—
EXTAL	AB11	NVCC_XTAL	ANALOG	—	EXTALOSC	EXTAL	—	—
FASTR_ANA	E18	NVCC_CKIH	ANALOG	—	—	(reserved, tie to ground)	—	—
FASTR_DIG	E17	NVCC_CKIH	ANALOG	—	—	(reserved, tie to ground)	—	—
FEC_CRS_DV	D11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[25]	Input	100 KΩ PU
FEC_MDC	E10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[31]	Input	100 KΩ PU
FEC_MDIO	D12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[22]	Input	100 KΩ PU
FEC_REF_CLK	E12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[23]	Input	100 KΩ PU
FEC_RX_ER	F12	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[24]	Input	100 KΩ PU
FEC_RXD0	C11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[27]	Input	100 KΩ PU
FEC_RXD1	E11	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[26]	Input	100 KΩ PU
FEC_TX_EN	C10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[28]	Input	360 KΩ PD
FEC_TXD0	F10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[30]	Input	100 KΩ PU
FEC_TXD1	D10	NVCC_FEC	UHVIO	ALT1	GPIO-1	gpio1_GPIO[29]	Input	100 KΩ PU
GPIO_0	C8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[0]	Input	360 KΩ PD
GPIO_1	B7	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[1]	Input	360 KΩ PD
GPIO_10	W16	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[0]	Input	100 KΩ PU
GPIO_11	V17	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[1]	Input	100 KΩ PU
GPIO_12	W17	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[2]	Input	100 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
GPIO_13	AA18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[3]	Input	100 KΩ PU
GPIO_14	W18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[4]	Input	100 KΩ PU
GPIO_16	C6	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[11]	Input	360 KΩ PD
GPIO_17	A3	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[12]	Input	360 KΩ PD
GPIO_18	D7	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[13]	Input	360 KΩ PD
GPIO_19	B4	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[5]	Input[3]	100 KΩ PU
GPIO_2	C7	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[2]	Input	360 KΩ PD
GPIO_3	A6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[3]	Input	360 KΩ PD
GPIO_4	D8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[4]	Input	100 KΩ PU
GPIO_5	A5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[5]	Input	360 KΩ PD
GPIO_6	B6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[6]	Input	360 KΩ PD
GPIO_7	A4	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[7]	Input	360 KΩ PD
GPIO_8	B5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[8]	Input	360 KΩ PD
GPIO_9	E8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[9]	Input	100 KΩ PU
JTAG_MOD	C9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_MOD	Input	100 KΩ PU
JTAG_TCK	D9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TCK	Input	100 KΩ PD
JTAG_TDI	B8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDI	Input	47 KΩ PU
JTAG_TDO	A7	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDO	Input	Keeper
JTAG_TMS	A8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TMS	Input	47 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
LVDS1_TX0_N	AC14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[31]	Input	Floating
LVDS1_TX0_P	AB14	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[30]	Input	Floating
LVDS1_TX1_N	AC13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[29]	Input	Floating
LVDS1_TX1_P	AB13	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[28]	Input	Floating
LVDS1_TX2_N	AC12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[25]	Input	Floating
LVDS1_TX2_P	AB12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[24]	Input	Floating
LVDS1_TX3_N	AA12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[23]	Input	Floating
LVDS1_TX3_P	Y12	NVCC_LVDS	LVDS	ALT0	GPIO-6	gpio6_GPI[22]	Input	Floating
NANDF_ALE	Y11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[8]	Input	100 KΩ PU
NANDF_CLE	AA10	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[7]	Input	100 KΩ PU
NANDF_CS0	W12	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[11]	Input	100 KΩ PU
NANDF_CS1	V13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[14]	Input	100 KΩ PU
NANDF_CS2	V14	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[15]	Input	100 KΩ PU
NANDF_CS3	W13	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[16]	Input	100 KΩ PU
NANDF_RB0	U11	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[10]	Input	100 KΩ PU
NANDF_RE_B	AC8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[13]	Input	100 KΩ PU
NANDF_WE_B	AB8	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-6	gpio6_GPIO[12]	Input	100 KΩ PU
NANDF_WP_B	AC9	NVCC_NANDF	UHVIO	ALT1	GPIO-6	gpio6_GPIO[9]	Input	100 KΩ PU
PATA_BUFFER_EN	K4	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[1]	Input	100 KΩ PU
PATA_CS_0	L5	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[9]	Input	100 KΩ PU
PATA_CS_1	L2	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[10]	Input	100 KΩ PU
PATA_DA_0	K6	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[6]	Input	100 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
SD1_DATA2	F17	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[19]	Input	100 KΩ PU
SD1_DATA3	F16	NVCC_SD1	UHVIO	ALT1	GPIO-1	gpio1_GPIO[21]	Input	100 KΩ PU
SD2_CLK	E14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[10]	Input	100 KΩ PU
SD2_CMD	C15	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[11]	Input	100 KΩ PU
SD2_DATA0	D13	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[15]	Input	100 KΩ PU
SD2_DATA1	C14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[14]	Input	100 KΩ PU
SD2_DATA2	D14	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[13]	Input	100 KΩ PU
SD2_DATA3	E13	NVCC_SD2	UHVIO	ALT1	GPIO-1	gpio1_GPIO[12]	Input	100 KΩ PU
TEST_MODE	D17	NVCC_RESET	LVIO	ALT0		tcu_TEST_MODE	Input	100 KΩ PD
TVCDC_IOB_BACK	AB19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOB_BACK	—	—
TVCDC_IOG_BACK	AC20	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOG_BACK	—	—
TVCDC_IOR_BACK	AB21	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVCDC_IOR_BACK	—	—
TVDAC_COMP	AA19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_COMP	—	—
TVDAC_IOB	AC19	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOB	—	—
TVDAC_IOG	AB20	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOG	—	—
TVDAC_IOR	AC21	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_IOR	—	—
TVDAC_VREF	Y18	TVDAC_AHVDDRGB	ANALOG	—	TVE	TVDAC_VREF	—	—
USB_H1_DN	B17	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_DN	—	—
USB_H1_DP	A17	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_DP	—	—