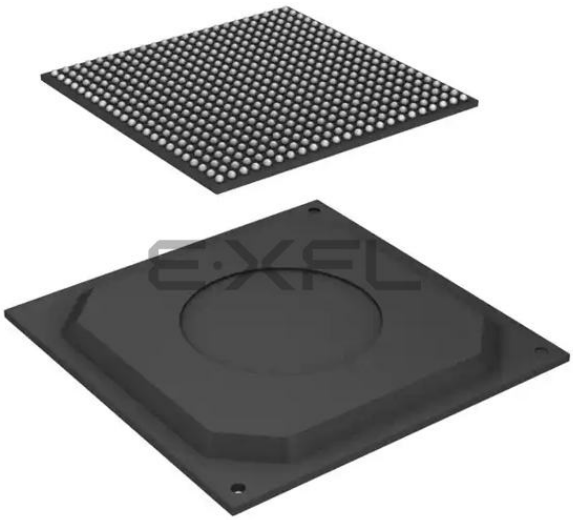

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx534avv8c

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX53xA processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX53xA processor system.

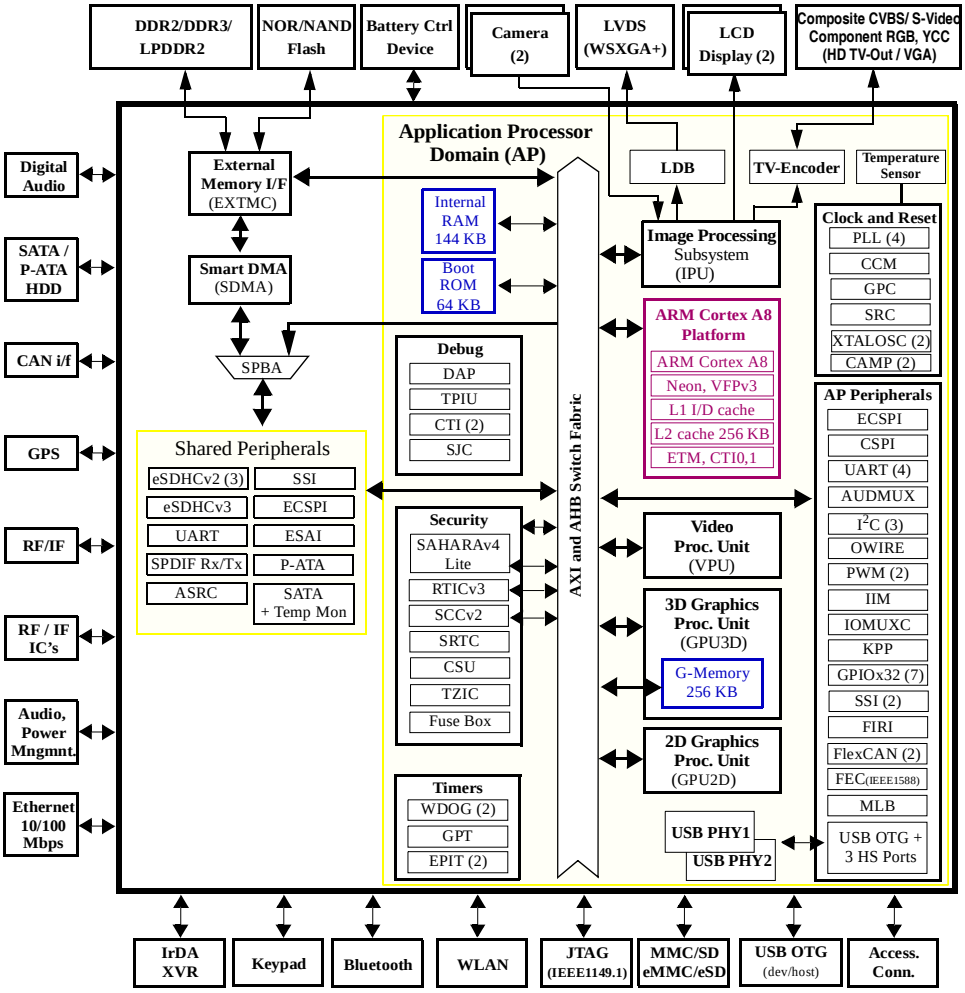

Figure 1. i.MX53xA System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

Table 3. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
BOOTROM	Boot ROM	Internal Memory	Supports secure and regular boot modes. The ROM controller supports ROM patching.
RTIC	Run-Time Integrity Checker	Security	Protecting read only data from modification is one of the basic elements in trusted platforms. The run-time integrity checker, version 3 (RTIC) block is a data-monitoring device responsible for ensuring that the memory content is not corrupted during program execution. The RTIC mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The purpose of the RTIC is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement and assist with boot authentication.
SAHARA	SAHARA Security Accelerator	Security	SAHARA (symmetric/asymmetric hashing and random accelerator), version 4, is a security coprocessor. It implements symmetric encryption algorithms, (AES, DES, 3DES, RC4 and C2), public key algorithms (RSA and ECC), hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256), and a hardware true random number generator. It has a slave IP Bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SATA	Serial ATA	Connectivity Peripherals	SATA HDD interface, includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity.
SCCv2	Security Controller, ver. 2	Security	The security controller is a security assurance hardware module designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords and biometrics reference data. The SCCv2 monitors the system's alert signal to determine if the data paths to and from it are secure, that is, it cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCCv2 also features a key encryption module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.

4.3.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 17 shows the Low Voltage Differential Signaling (LVDS) DC electrical characteristics. The parameters in Table 17 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 17. LVDS DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	V_{OD}	Rload = 100Ω between padP and padN	250	350	450	mV
Output High Voltage	V_{OH}		1.25	1.375	1.6	V
Output Low Voltage	V_{OL}		0.9	1.025	1.25	
Offset Voltage	V_{OS}		1.125	1.2	1.375	

4.4 Output Buffer Impedance Characteristics

This section defines the I/O Impedance parameters of the i.MX53xA processor for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2, and DDR3 modes
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

Output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission lime. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 4).

[4] T_{dpdref} is the time period of the reference clock after predivider. According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

[5] Tdck is the time period of the output clock, dpdck_2.

4.6.5 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among various signals of NFC at the module level, in each operational mode.

Timing parameters in Figure 10, Figure 11, Figure 12, Figure 13, Figure 15, and Table 36 show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B.

Timing parameters in Figure 10, Figure 11, Figure 12, Figure 14, Figure 15, and Table 36 show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16— 40 pF) and there is maximum drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock (“enfc_clk” at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider.

Figure 35 demonstrates several examples of clock frequency settings.

Table 35. NFC Clock Settings Examples

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T-Clock Period (ns)
100 (Boot mode)	7[1]	14.29	70
	3[2]	33.33	30
133	4	33.33	30
	3	44.33[3]	22.5
	2	66[3]	15

[1] Boot value NFC_FREQ_SEL Fuse High (burned)

[2] Boot value NFC_FREQ_SEL Fuse Low

[3] For RBB_MODE=1, using NANDF_RB0 signal for ready/busy indication. This mode require setting the delay line. See the Reference Manual for details.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low, the data bus capturing might occur after the specified t_{rhoh} (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (that is, T = 39 ns) guaranties a proper operation for devices having t_{rhoh} > 15 ns. It is also recommended that the NFC_FREQ_SEL Fuse be set accordingly to initiate the boot with 33.33 MHz clock.

[4] NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

[5] NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^3 - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.6 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.6.6.1 EIM Signal Cross Reference

Table 37 is a guide intended to help the user identify signals in the External Interface Module Chapter of the Reference Manual which are identical to those mentioned in this data sheet.

Table 37. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.6.2 EIM Interface Pads Allocation

EIM supports16-bit and 8-bit devices operating in address/data separate or multiplexed modes. In some of the modes the EIM and the NAND FLASH have shared data bus. Table 38 provides EIM interface pads allocation in different modes.

Table 39. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—

4.7 External Peripheral Interfaces Parameters

The following subsections provide information on external peripheral interfaces.

4.7.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.7.2 CSPI and ECSPI Timing Parameters

This section describes the timing parameters of the CSPI and ECSPI blocks. The CSPI and ECSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI / ECSPI modules and the respective routing of these signals is shown in Table 45.

Table 45. CSPI Nomenclature and Routing

Block Instance	I/O Access
ECSPI-1	GPIO, KPP, DISP0_DAT, CSI0_DAT and EIM_D through IOMUXC
ECSPI-2	DISP0_DAT, CSI0_DAT and EIM through IOMUXC
CSPI	DISP0_DAT, EIM_A/D, SD1 and SD2 through IOMUXC

4.7.2.1 CSPI Master Mode Timing

Figure 32 depicts the timing of CSPI in master mode. Table 46 lists the CSPI master mode timing characteristics.

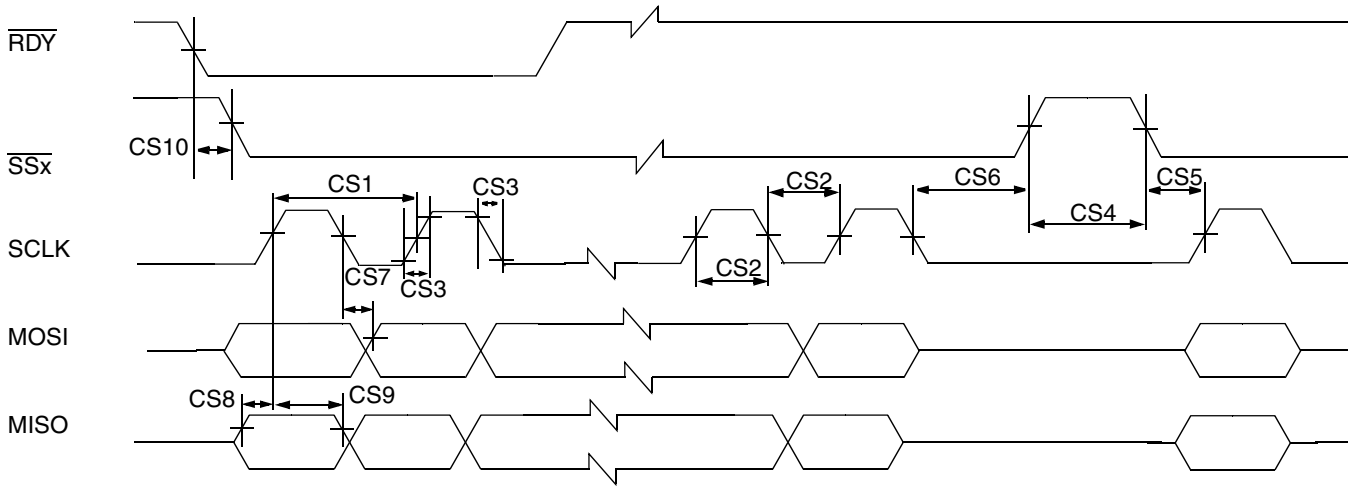

Figure 32. CSPI/ECSPI Master Mode Timing Diagram

Table 49. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
80	SCKT rising edge to FST out (wr) high[6]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [77]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 VCORE_VDD= 1.00 ± 0.10V
Tj = -40 °C to 125 °C
CL= 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

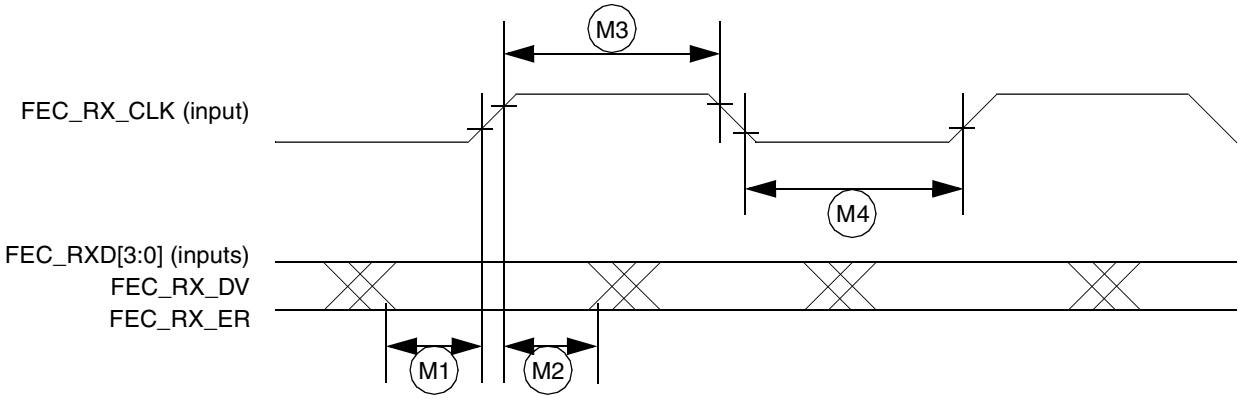

Figure 38. MII Receive Signal Timing Diagram

4.7.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 53 lists MII transmit channel timing parameters. Figure 39 shows MII transmit signal timing diagram for the values listed in Table 53.

Table 53. MII Transmit Signal Timing

Num	Characteristic[1] [2]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

[2] Test conditions: 25pF on each output signal.

Table 60. Video Signal Cross-Reference

i.MX53xA	LCD								Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

NOTE

Table 60 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.7.8.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.7.8.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the i.MX53 Reference Manual.

4.7.8.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

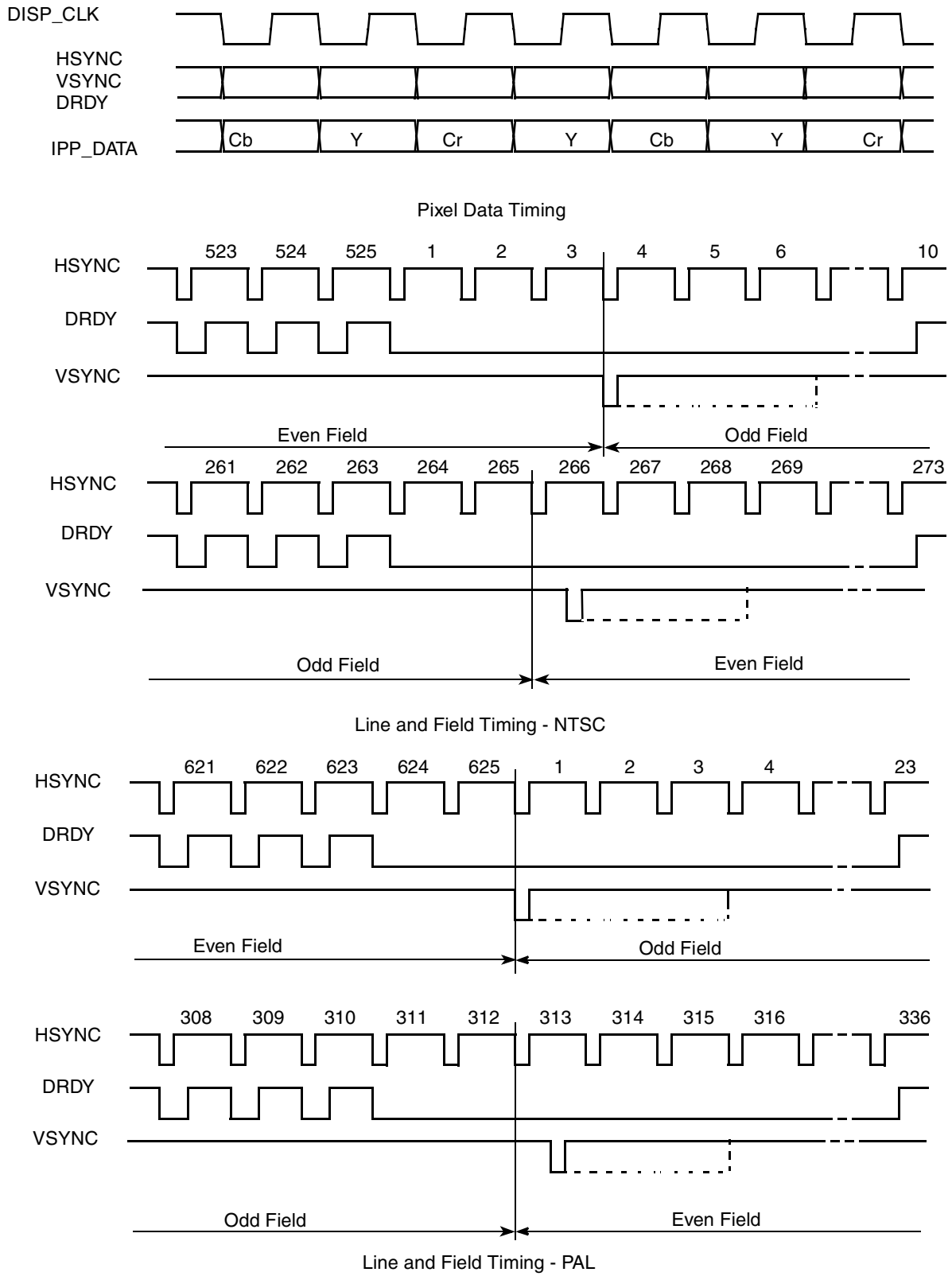

Figure 51. TV Encoder Interface Timing Diagram

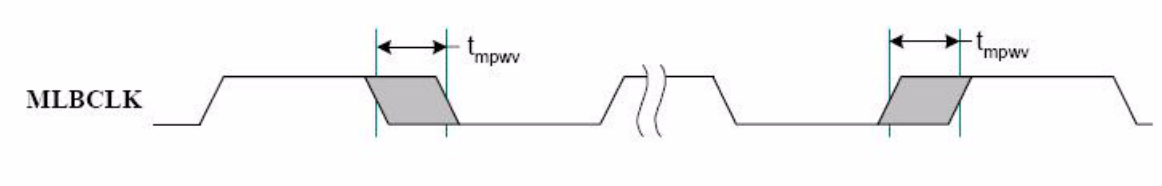

Figure 59. MediaLB Pulse Width Variation Timing

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 66. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256*fs at 44.0 kHz Typ: 256*fs at 48.0 kHz Typ: 512*fs at 48.0 kHz Max: 512*fs at 48.1 kHz Max: 512*fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	256*Fs 512*Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512*Fs 512*Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	256*Fs 256*Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512*Fs 512*Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	2	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	2.5	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	4	—	10	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note[3]
MLBSIG/MLBDAT output valid from MLBCLK high	t_{delay}	—	—	11	ns	—

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

Table 77. UDMA in Burst Timing Parameters (continued)

ATA Parameter	Parameter from Figure 70, Figure 71, and Figure 72	Description	Controlling Variable
tcyc	tc1	(tcyc - tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T - (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) - (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) - (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) - (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T - tskew1 toff = time_off × T - tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

4.7.13.3 UDMA Output Timing

Figure 73 shows timing when the UDMA out transfer starts, Figure 74 shows timing when the UDMA out host terminates transfer, Figure 75 shows timing when the UDMA out device terminates transfer, and Table 78 lists the timing parameters for UDMA out burst.

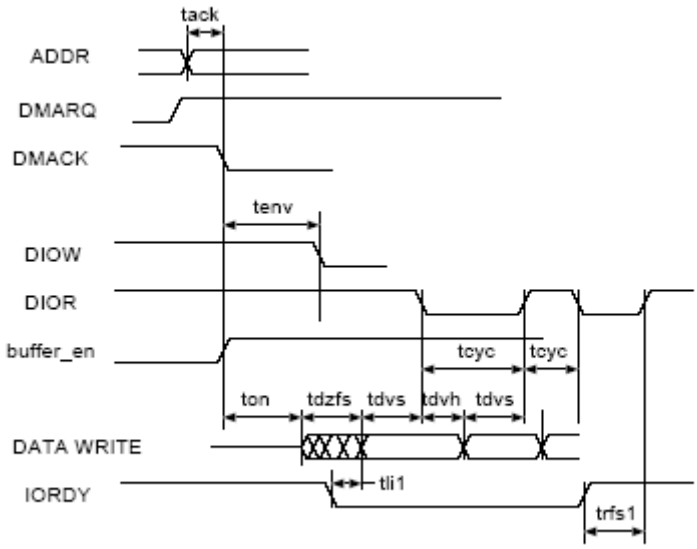

Figure 73. UDMA Out Transfer Starts Timing Diagram

Table 82. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{TRST}$ assert time	100	—	ns
SJ13	$\overline{TRST}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.7.16 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 83 and Figures , show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 83. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Units
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

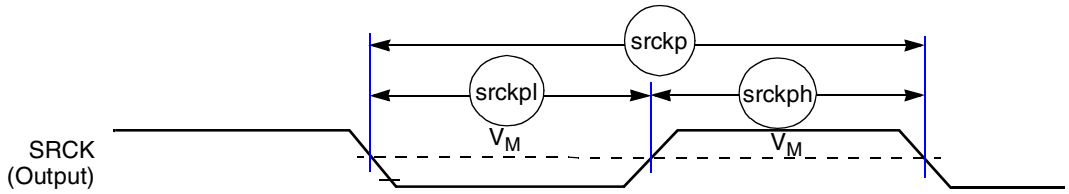

Figure 81. SPDIF Timing Diagram

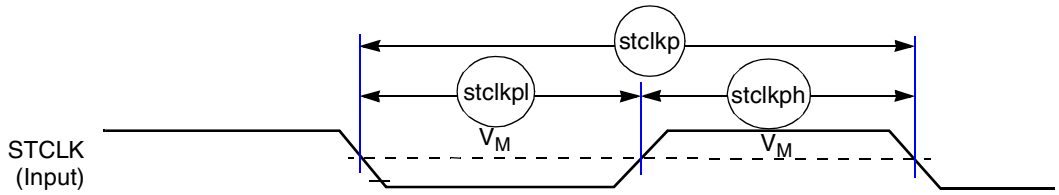

Figure 82. STCLK Timing

4.7.17 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 84.

Table 84. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External— AUD3 I/O
AUDMUX port 4	AUD4	External— EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External— EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External— EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX53 Reference Manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

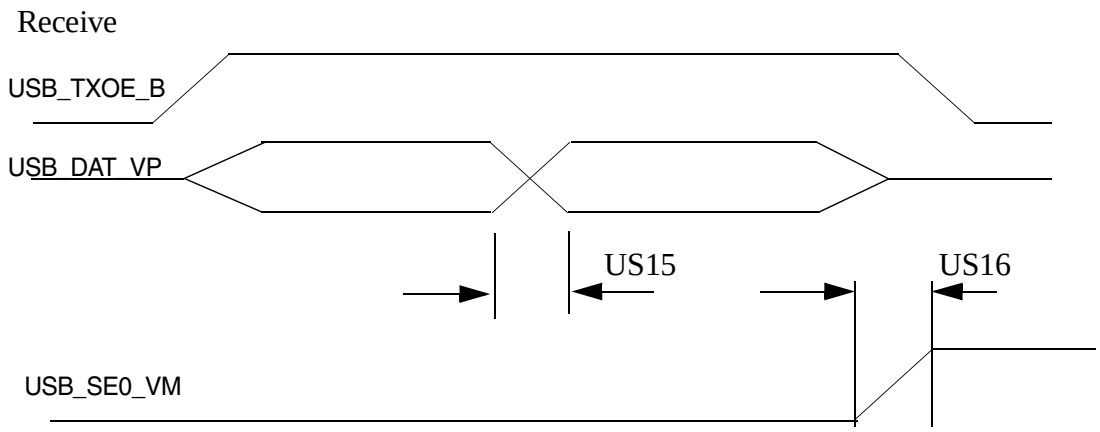

Figure 94. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 97. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition / Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF

Table 104. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
tfall	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	—	—	10 1 0.2	ns

4.7.20.2 USB PHY Additional Electrical Parameters

Table 105 lists the parameters for additional electrical characteristics for USB PHY.

Table 105. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	< 160 MHz	-50	0	50	mV
Power supply ripple noise (analog 2.5 V)	< 1.2 MHz > 1.2 MHz	-10 -50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2 V)	All conditions	-50	0	50	mV

4.7.20.3 USB PHY System Clocking (SYSCLK)

Table 106 lists the USB PHY system clocking parameters.

Table 106. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	Reference Clock frequency 24 MHz	-150	—	150	ppm
Rise/fall time	—	—	—	200	ps
Jitter (peak-peak)	< 1.2 MHz	0	—	50	ps
Jitter (peak-peak)	> 1.2 MHz	0	—	100	ps
Duty-cycle	Reference Clock frequency 24 MHz	40	—	60	%

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DISP0_DAT20	F4	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[14]	Input	100 KΩ PU
DISP0_DAT21	C1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[15]	Input	100 KΩ PU
DISP0_DAT22	E3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[16]	Input	100 KΩ PU
DISP0_DAT23	C3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[17]	Input	100 KΩ PU
DISP0_DAT3	F1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[24]	Input	100 KΩ PD
DISP0_DAT4	G2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[25]	Input	100 KΩ PD
DISP0_DAT5	H3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[26]	Input	100 KΩ PD
DISP0_DAT6	G1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[27]	Input	100 KΩ PD
DISP0_DAT7	H6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[28]	Input	100 KΩ PD
DISP0_DAT8	G6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[29]	Input	100 KΩ PU
DISP0_DAT9	E2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[30]	Input	100 KΩ PU
DRAM_A0	M19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[0]	Output	Low
DRAM_A1	L21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[1]	Output	Low
DRAM_A10	K19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[10]	Output	Low
DRAM_A11	L22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[11]	Output	Low
DRAM_A12	L20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[12]	Output	Low
DRAM_A13	L23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[13]	Output	Low
DRAM_A14	N18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[14]	Output	Low
DRAM_A15	M18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[15]	Output	Low
DRAM_A2	M20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[2]	Output	Low

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_CS0	W8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[0]	Output	—
EIM_CS1	Y7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[1]	Output	—
EIM_D16	U6	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[16]	Input	100 KΩ PU
EIM_D17	U5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[17]	Input	100 KΩ PU
EIM_D18	V1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[18]	Input	100 KΩ PU
EIM_D19	V2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[19]	Input	100 KΩ PU
EIM_D20	W1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[20]	Input	100 KΩ PU
EIM_D21	V3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[21]	Input	100 KΩ PU
EIM_D22	W2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[22]	Input	360 KΩ PD
EIM_D23	Y1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[23]	Input	100 KΩ PU
EIM_D24	Y2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[24]	Input	100 KΩ PU
EIM_D25	W3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[25]	Input	100 KΩ PU
EIM_D26	V5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[26]	Input	100 KΩ PU
EIM_D27	V4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[27]	Input	100 KΩ PU
EIM_D28	AA1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[28]	Input	100 KΩ PU
EIM_D29	AA2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[29]	Input	100 KΩ PU
EIM_D30	W4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[30]	Input	100 KΩ PU
EIM_D31	W5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[31]	Input	360 KΩ PD
EIM_DA0	Y8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[0]	Input[2]	100 KΩ PU
EIM_DA1	AC4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[1]	Input[2]	100 KΩ PU