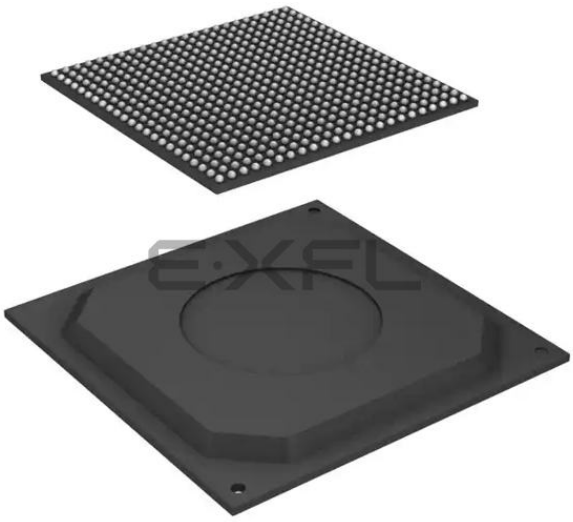

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx534avv8cr2

- Real-time integrity checker, version 3 (RTICv3)—RTIC type1, enhanced with SHA-256 engine
- SAHARAv4 Lite—Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2)—Improved SCC with AES engine, secure/non-secure RAM and support for multiple keys as well as TZ/non-TZ separation
- Central security unit (CSU)—Enhancement for the IIM (IC Identification Module). CSU is configured during boot by eFUSEs, and determines the security level operation mode as well as the TrustZone (TZ) policy
- Advanced High Assurance Boot (A-HAB)—HAB with the following embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization
- Tamper detection mechanism—Provides evidence of any physical attempt to remove the device cover. Upon detection of such an attack, sensitive information can immediately be erased.

Table 3. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESDHCV3-3	Ultra-High-Speed eMMC / SD Host Controller	Connectivity Peripherals	Ultra high-speed eMMC / SD host controller, enhanced to support eMMC 4.4 standard specification, for 832 MBps. • Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port). ESDHCV3 is backward compatible to ESDHCV2 and supports all the features of ESDHCV2 as described below.
ESDHCV2-1 ESDHCV2-2 ESDHCv2-4	Enhanced Multi-Media Card / Secure Digital Host Controller		Enhanced multimedia card / secure digital host controller • Ports 1, 2, and 4 are compatible with the “MMC System Specification” version 4.3, full support and supporting 1, 4 or 8-bit data. The generic features of the eSDHCv2 module, when serving as SD / MMC host, include the following: • Can be configured either as SD / MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to SD Host Controller Standard Specification, version 2.0, full support. • Compatible with the SD Memory Card Specification, version 1.1 • Compatible with the SDIO Card Specification, version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/high speed mode. • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using 4 parallel data lines • Up to 416 Mbps data transfer for MMC cards using 8 parallel data lines
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet media access controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX53xA also consists of HW assist for IEEE1588™ standard. See, TSU and CE_RTC (IEEE1588) section for more details.
FIRI	Fast Infrared Interface	Connectivity Peripherals	Fast infrared interface
FLEXCAN-1 FLEXCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The controller area network (CAN) protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus. Meets the following specific requirements of this application: real-time processing, reliable operation in the EXTMC environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN is a full implementation of the CAN protocol specification, Version 2.0 B (ISO 11898), which supports both standard and extended message frames at 1 Mbps.

4.1.2 Thermal Resistance

4.1.2.1 TEPBGA-2 Package Thermal Resistance

Table 6 provides the TEPBGA-2 package thermal resistance data.

Table 6. TEPBGA-2 Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	21	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	6	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	4	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	4	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.2 Power-Down Sequence

Power-down sequence should follow one of the following two options:

- Option 1: Switch all supplies down simultaneously with further free discharge. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
- Option 2: Switch down supplies, in any order, keeping the following rules:
  - NVCC_CKIH must be powered down at the same time or after the UHVIO I/O cell supplies (for full supply list, see Table 7, Ultra High voltage I/O (UHVIO) supplies). A deviation of few microseconds of actual power-down of the different power rails is acceptable.
  - VDD_REG must be powered down at the same time or after NVCC_EMI_DRAM supply. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
  - If all of the following conditions are met:
    – VDD_REG is powered down to 0V (Not Hi-Z)
    – VDD_DIG_PLL and VDD_ANA_PLL are provided externally,
    – VDD_REG is powered down before VDD_DIG_PLL and VDD_ANA_PLL
    Then the following rule should be kept: VDD_REG output impedance must be higher than 1 kW, when inactive.

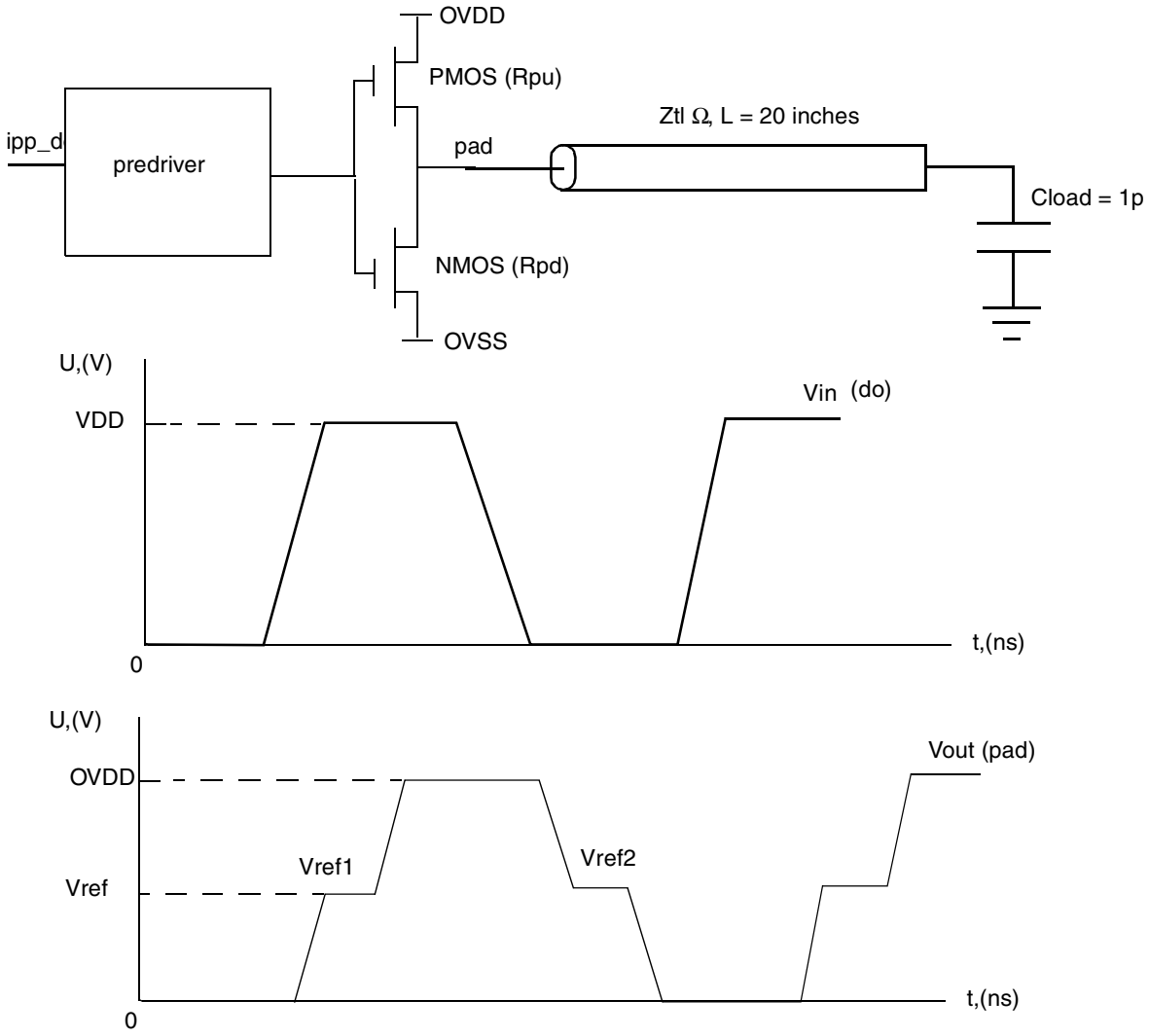
4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is off. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”
- If not using SATA interface and the embedded thermal sensor, the VP and VPH should be grounded. In particular, keeping VPH turned OFF while the VP is powered ON is not recommended and might lead to excessive power consumption.
- When internal clock source is used for SATA temperature monitor the USB_PHY supplies and PLL need to be active because they are providing the clock.
- If not using the TVE module, the TVDAC_DHVDD and TVDAC_AHVDDRGB can be kept floating or tied to GND—the recommendation is to float. If only the GPIO pads in TVDAC_AHVDDRGB domain are in use, the supplies can be set to GPIO pad voltage range (1.65 V to 3.1 V).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 4. Impedance Matching Load for Measurement

Table 19 shows DDR output driver average impedance of the i.MX53xA processor.

Table 19. DDR Output Driver Average Impedance[1]

Parameter	Symbol	Test Conditions	Drive strength (DSE)								Unit
			000	001	010	011	100	101	110	111	
Output Driver Impedance	Rdrv[2]	LPDDR1/DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 00 Calibration resistance = 300 Ω[3]	Hi-Z	300	150	100	75	60	50	43	Ω
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 01 Calibration resistance = 180 Ω[3]	Hi-Z	180	90	60	45	36	30	26	
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 10 Calibration resistance = 200 Ω[3]	Hi-Z	200	100	66	50	40	33	28	
		DDR2 mode NVCC_DRAM= 1.8 V DDR_SEL = 11 Calibration resistance = 140 Ω[3]	Hi-Z	140	70	46	35	28	23	20	
		LPDDR2 mode NVCC_DRAM= 1.2 V DDR_SEL = 01[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 10 Calibration resistance = 240 Ω[3]	Hi-Z	240	120	80	60	48	40	34	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 11[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		DDR3 mode NVCC_DRAM = 1.5 V DDR_SEL = 00 Calibration resistance = 200 Ω[3]	Hi-Z	240	120	80	60	48	48	34	

1 Output driver impedance is controlled across PVTs (process, voltages, and temperatures) using calibration procedure and pu_*cal, pd_*cal input pins.

2 Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3 Calibration is done against external reference resistor. Value of the resistor should be varied depending on DDR mode and DDR_SEL setting.

4 If DDR_SEL = ‘01’ or DDR_SEL = ‘11’ are selected with NVCC_DRAM = 1.2 V for LPDDR2 operation, the external reference resistor value must be 160 Ω for a correct ZQ calibration. In any case, reference resistors attached to the DDR memory devices should be kept to 240 Ω per the JEDEC standard.

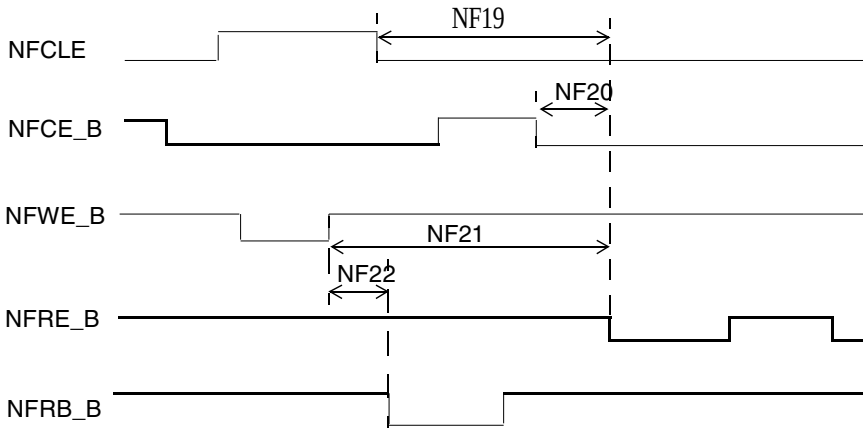


Figure 15. Other Timing Parameters

[4] NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

[5] NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^{3} - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including I/O pad delay, and t_{Dpd} is Data propogation delay from I/O pad to EXTMC including I/O pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.6 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.6.6.1 EIM Signal Cross Reference

Table 37 is a guide intended to help the user identify signals in the External Interface Module Chapter of the Reference Manual which are identical to those mentioned in this data sheet.

Table 37. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.6.2 EIM Interface Pads Allocation

EIM supports16-bit and 8-bit devices operating in address/data separate or multiplexed modes. In some of the modes the EIM and the NAND FLASH have shared data bus. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode	
	8 Bit			16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]
A[25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [24:16][1]	EIM_A [25:16]	NANDF_D [8:0][1]
D[7:0], EIM_EB0	NANDF_D [7:0][2]	—	—	NANDF_D [7:0][2]	—	NANDF_D [7:0]	EIM_DA [7:0]	EIM_DA [7:0]
D[15:8], EIM_EB1	—	NANDF_D [15:8][3]	—	NANDF_D [15:8][3]	—	NANDF_D [15:8]	EIM_DA [15:8]	EIM_DA [15:8]
D[23:16], EIM_EB2	—	—	—	—	EIM_D [23:16]	EIM_D [23:16]	—	NANDF_D [7:0]
D[31:24], EIM_EB3	—	—	EIM_D [31:24]	—	EIM_D [31:24]	EIM_D [31:24]	—	NANDF_D [15:8]

1 For 32-bit mode, the address range is A[24:0], due to address space allocation in memory map.

2 NANDF_D[7:0] multiplexed on ALT3 mode of PATA_DATA[7:0]

3 NANDF_D[15:8] multiplexed on ALT3 mode of PATA_DATA[15:8]

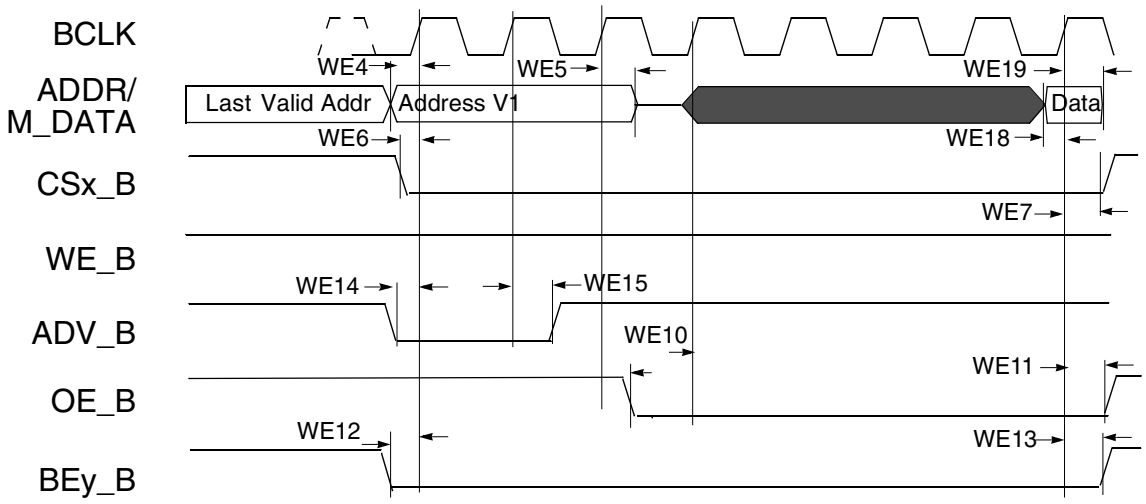


Figure 21. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, and OEA=0

4.6.6.5 General EIM Timing-Asynchronous Mode

Figure 22 through Figure 27, and Table 40 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 22 through Figure 25 as RWSC, OEN, and CSN is configured differently. See i.MX53 reference manual for the EIM programming model.

NOTE

Table 60 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.7.8.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.7.8.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the i.MX53 Reference Manual.

4.7.8.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

Figure 64 depicts the timing of the PWM, and Table 71 lists the PWM timing parameters.

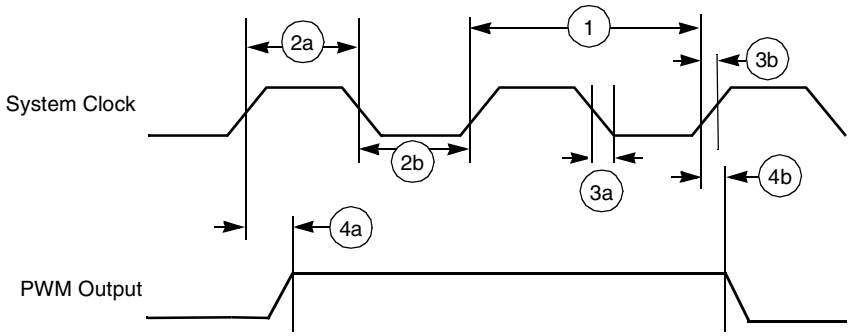


Figure 64. PWM Timing

Table 71. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.13 PATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-6 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100MB/s. Parallel ATA module interface consist of a total of 29 pins. Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Table 72 and Figure 65 define the AC characteristics of all the PATA interface signals in all data transfer modes.

Figure 67 shows timing for PIO write. Table 75 lists the timing parameters for PIO write.

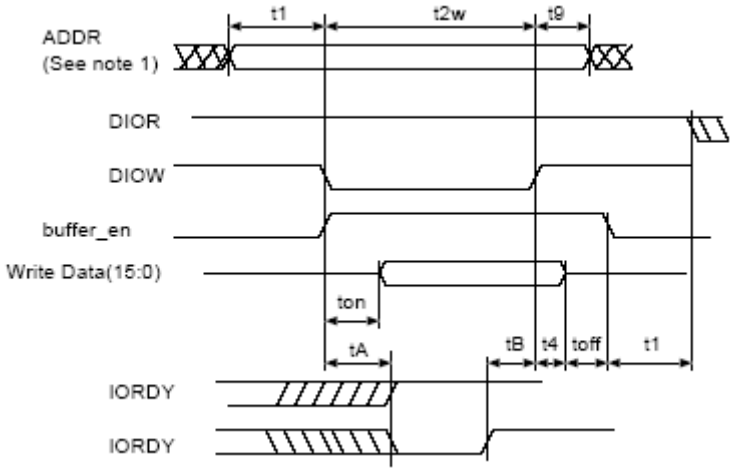


Figure 67. Multi-word DMA (MDMA) Timing

Table 75. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 67	Value	Controlling Variable
t1	t1	t1(min) = time_1 x T - (tskew1 + tskew2 + tskew5)	time_1
t2 (write)	t2w	t2(min) = time_2w x T - (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9(min) = time_9 x T - (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3(min) = (time_2w - time_on) x T - (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4(min) = time_4 x T - tskew1	time_4
tA	tA	tA = (1.5 + time_ax) x T - (tco + tsui + tcable2 + tcable2 + 2 x tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) x T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

Table 76. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 68 (Read), Figure 69 (Write)	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = time_jn x T - (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T - tskew1 toff = time_off × T - tskew1	—

1 tk1 in the MDMA figures (**Figure 68** and **Figure 69**) equals (tk - 2 x T).

2 tk1 in the MDMA figures equals (tk – 2 x T).

4.7.13.2 Ultra DMA (UDMA) Input Timing

Figure 70 shows timing when the UDMA in transfer starts, Figure 71 shows timing when the UDMA in host terminates transfer, Figure 72 shows timing when the UDMA in device terminates transfer, and Table 77 lists the timing parameters for UDMA in burst.

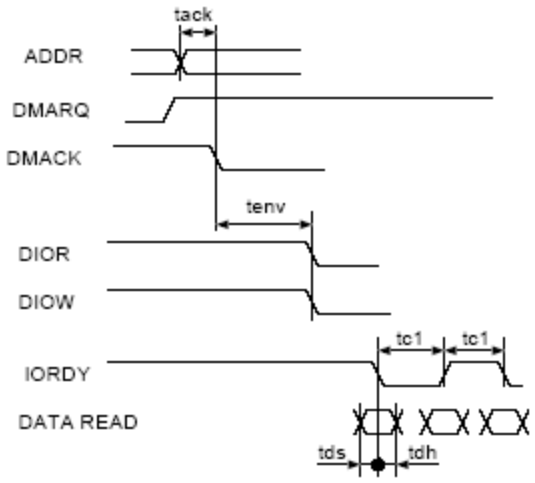


Figure 70. UDMA in Transfer Starts Timing Diagram

Table 104. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
tfall	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	—	—	10 1 0.2	ns

4.7.20.2 USB PHY Additional Electrical Parameters

Table 105 lists the parameters for additional electrical characteristics for USB PHY.

Table 105. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	< 160 MHz	-50	0	50	mV
Power supply ripple noise (analog 2.5 V)	< 1.2 MHz > 1.2 MHz	-10 -50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2 V)	All conditions	-50	0	50	mV

4.7.20.3 USB PHY System Clocking (SYSCLK)

Table 106 lists the USB PHY system clocking parameters.

Table 106. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	Reference Clock frequency 24 MHz	-150	—	150	ppm
Rise/fall time	—	—	—	200	ps
Jitter (peak-peak)	< 1.2 MHz	0	—	50	ps
Jitter (peak-peak)	> 1.2 MHz	0	—	100	ps
Duty-cycle	Reference Clock frequency 24 MHz	40	—	60	%

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
CSI0_VSYNC	P4	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[21]	Input	100 KΩ PU
DI0_DISP_CLK	H4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[16]	Input	100 KΩ PU
DI0_PIN15	E4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[17]	Input	100 KΩ PU
DI0_PIN2	D3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[18]	Input	100 KΩ PU
DI0_PIN3	C2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[19]	Input	100 KΩ PU
DI0_PIN4	D2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[20]	Input	100 KΩ PU
DISP0_DAT0	J5	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[21]	Input	100 KΩ PD
DISP0_DAT1	J4	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[22]	Input	100 KΩ PD
DISP0_DAT10	G3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[31]	Input	100 KΩ PU
DISP0_DAT11	H5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[5]	Input	100 KΩ PD
DISP0_DAT12	H1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[6]	Input	100 KΩ PU
DISP0_DAT13	E1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[7]	Input	100 KΩ PU
DISP0_DAT14	F2	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[8]	Input	100 KΩ PU
DISP0_DAT15	F3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[9]	Input	100 KΩ PU
DISP0_DAT16	D1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[10]	Input	100 KΩ PU
DISP0_DAT17	F5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[11]	Input	100 KΩ PU
DISP0_DAT18	G4	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[12]	Input	100 KΩ PU
DISP0_DAT19	G5	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[13]	Input	100 KΩ PU
DISP0_DAT2	H2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[23]	Input	100 KΩ PD

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_CS0	W8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[0]	Output	—
EIM_CS1	Y7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[1]	Output	—
EIM_D16	U6	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[16]	Input	100 KΩ PU
EIM_D17	U5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[17]	Input	100 KΩ PU
EIM_D18	V1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[18]	Input	100 KΩ PU
EIM_D19	V2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[19]	Input	100 KΩ PU
EIM_D20	W1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[20]	Input	100 KΩ PU
EIM_D21	V3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[21]	Input	100 KΩ PU
EIM_D22	W2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[22]	Input	360 KΩ PD
EIM_D23	Y1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[23]	Input	100 KΩ PU
EIM_D24	Y2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[24]	Input	100 KΩ PU
EIM_D25	W3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[25]	Input	100 KΩ PU
EIM_D26	V5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[26]	Input	100 KΩ PU
EIM_D27	V4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[27]	Input	100 KΩ PU
EIM_D28	AA1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[28]	Input	100 KΩ PU
EIM_D29	AA2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[29]	Input	100 KΩ PU
EIM_D30	W4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[30]	Input	100 KΩ PU
EIM_D31	W5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[31]	Input	360 KΩ PD
EIM_DA0	Y8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[0]	Input[2]	100 KΩ PU
EIM_DA1	AC4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[1]	Input[2]	100 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
GPIO_13	AA18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[3]	Input	100 KΩ PU
GPIO_14	W18	TVDAC_AHVDDRGB	GPIO	ALT0	GPIO-4	gpio4_GPIO[4]	Input	100 KΩ PU
GPIO_16	C6	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[11]	Input	360 KΩ PD
GPIO_17	A3	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[12]	Input	360 KΩ PD
GPIO_18	D7	NVCC_GPIO	UHVIO	ALT1	GPIO-7	gpio7_GPIO[13]	Input	360 KΩ PD
GPIO_19	B4	NVCC_KEYPAD	UHVIO	ALT1	GPIO-4	gpio4_GPIO[5]	Input[3]	100 KΩ PU
GPIO_2	C7	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[2]	Input	360 KΩ PD
GPIO_3	A6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[3]	Input	360 KΩ PD
GPIO_4	D8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[4]	Input	100 KΩ PU
GPIO_5	A5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[5]	Input	360 KΩ PD
GPIO_6	B6	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[6]	Input	360 KΩ PD
GPIO_7	A4	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[7]	Input	360 KΩ PD
GPIO_8	B5	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[8]	Input	360 KΩ PD
GPIO_9	E8	NVCC_GPIO	UHVIO	ALT1	GPIO-1	gpio1_GPIO[9]	Input	100 KΩ PU
JTAG_MOD	C9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_MOD	Input	100 KΩ PU
JTAG_TCK	D9	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TCK	Input	100 KΩ PD
JTAG_TDI	B8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDI	Input	47 KΩ PU
JTAG_TDO	A7	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TDO	Input	Keeper
JTAG_TMS	A8	NVCC_JTAG	GPIO	ALT0	SJC	sjc_TMS	Input	47 KΩ PU

6.1.4 19 x 19 mm, 0.8 mm Pitch Ball Map

Table 115 shows the 19 × 19 mm, 0.8 mm pitch ball map.

Table 115. 19 x 19 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	GPIO_17	GPIO_7	GPIO_5	GPIO_3	JTAG_TDO	JTAG_TMS	VPH	SATA_TXP	GND	SATA_RXM	GND	SATA_REFCLKM	VP	USB_H1_GPANAIO	USB_H1_DP	GND	USB_OTG_DN	SD1_DATA0	RESET_IN_B	GND	GND	A
B	GND	SVDDGP	KEY_ROW0	GPIO_19	GPIO_8	GPIO_6	GPIO_1	JTAG_TDI	VPH	SATA_TXM	GND	SATA_RXP	GND	SATA_REFCLKP	VP	USB_H1_RREFEXT	USB_H1_DN	GND	USB_OTG_DP	BOOT_MODE1	CKIH1	SVCC	GND	B
C	DISP0_DAT21	DI0_PIN3	DISP0_DAT23	KEY_COL2	KEY_COL0	GPIO_16	GPIO_2	GPIO_0	JTAG_MOD	FEC_TX_EN	FEC_RXD0	GND	SATA_REXT	SD2_DATA1	SD2_CMD	USB_OTG_ID	SD1_DATA1	BOOT_MODE0	POR_B	GND	GND	DRAM_D15	DRAM_D13	C
D	DISP0_DAT16	DI0_PIN4	DI0_PIN2	KEY_ROW3	KEY_ROW2	KEY_ROW1	GPIO_18	GPIO_4	JTAG_TCK	FEC_TXD1	FEC_CRS_DV	FEC_MDIO	SD2_DATA0	SD2_DATA2	USB_H1_VBUS	USB_OTG_RREFEXT	TEST_MODE	CKIH2	GND	DRAM_D11	DRAM_D9	DRAM_SDQS1_B	DRAM_SDQS1	D
E	DISP0_DAT13	DISP0_DAT9	DISP0_DAT22	DI0_PIN15	KEY_COL4	KEY_ROW4	KEY_COL1	GPIO_9	JTAG_TRSTB	FEC_MDC	FEC_RXD1	FEC_REF_CLK	SD2_DATA3	SD2_CLK	USB_OTG_VBUS	SD1_CLK	FASTR_DIG	FASTR_ANA	GND	DRAM_DQM1	DRAM_D8	DRAM_D10	DRAM_D12	E
F	DISP0_DAT3	DISP0_DAT14	DISP0_DAT15	DISP0_DAT20	DISP0_DAT17	KEY_COL3	NVCC_KEYPAD	NVCC_GPIO	VDDAL1	FEC_TXD0	NVCC_FEC	FEC_RX_ER	USB_H1_VDDA25	USB_OTG_VDDA25	USB_OTG_GPANAIO	SD1_DATA3	SD1_DATA2	SD1_CMD	GND	GND	GND	GND	DRAM_D14	F

7 Revision History

Table 116 provides a revision history for this data sheet.

Table 116. i.MX53xA Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	03/2013	In Table 2, “Ordering Information” removed MCIMX535DVV2C, as it no longer exists. In Table 7, “i.MX53xA Operating Ranges,” updated minimum values of LVDS interface supply (NVCC_LVDS) and LVDS band gap supply (NVCC_LVDS_BG) to 2.375 volts.
Rev. 5	09/2012	• In Table 2, "Ordering Information," on page 4,” renamed “Features” column as “CPU Frequency” and removed part number, PCIMX536AVV8C. • Added Table 1, "i.MX53 Parts Functional Differences," on page 3. • In Section 1.2, “Features:” —Changed “SATA I” to “SATA II” under Hard disk drives bullet —Added a new bullet item to mention support for tamper detection mechanism • Removed the note shown at the end of Section 1.2, “Features.” • In Table 3, "i.MX53xA Digital and Analog Blocks," on page 9, removed details of MPEG2 encoder, as this is not supported on i.MX53. • In Table 7, "i.MX53xA Operating Ranges," on page 21, updated footnote on TVDAC_DHVDD and TVDAC_AHVDDRGB. • In Table 9, "Maximal Supply Currents," on page 23: —Corrected power line name, MVCC_XTAL, to NVCC_XTAL —Added a footnote on NVCC_EMI_DRAM —Updated max current value and added a footnote for power line, NVCC_SRTC_POW —Removed duplicate entries for NVCC_EMI_DRAM and NVCC_XTAL • In Section 4.2.3, “Power Supplies Usage,” updated the fourth bullet item. • In Figure 25, "Asynchronous A/D Muxed Write Access," on page 61, renamed “WE41” as “WE41A” and shifted its position to left. • In Table 58, "Camera Input Signal Cross Reference, Format and Bits Per Cycle," on page 83, added a footnote on “YCbCr 8 bits 2 cycles” column header.
Rev. 4	11/2011	• In Section 1, “Introduction,” changed 1 GHz to 1.2 GHz in the second paragraph and updated the bulleted list after the second paragraph. • In Table 2, "Ordering Information," on page 4: —Removed part numbers “PCIMX535DVV1C” and “MCIMX538DZK1C” —Added a new part number “MCIMX535DVV2C” —Updated package information for part number “PCIMX538DZK1C” —Updated the second footnote • In Section 1.2, “Features,” changed “Target frequency” to “Maximum frequency” and 1 GHz to 1–1.2 GHz in the third bullet item of the first bulleted list. • In Table 3, "i.MX53xA Digital and Analog Blocks," on page 9, removed “Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate” from VPU brief description. • In Table 5, "Absolute Maximum Ratings," on page 19, changed the maximum voltage for VDDGP from 1.35V to 1.4V. • In Table 7, "i.MX53xA Operating Ranges," on page 21: —Added a row and a footnote for “ARM core supply voltage $f_{ARM} \leq$ 1200 MHz” parameter of VDDGP —Added a new footnote for “Peripheral supply voltage” parameter of VCC —Updated the footnote for “Junction temperature” parameter • In Section 1.2, “Features,” changed “Target frequency” to “Maximum frequency” in the third bullet item of the first bulleted list. • In Table 3, "i.MX53xA Digital and Analog Blocks," on page 9, removed “Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate” from VPU brief description. (continued on next page)