Renesas Electronics America Inc - R5F2LA64ADFP#30 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la64adfp-30

Table 1.12 Product List for R8C/LA8A Group **Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA84ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	N Version
R5F2LA84ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA8AANFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8AANFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA8CANFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8CANFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA84ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	D Version
R5F2LA84ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA8AADFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8AADFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA8CADFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8CADFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	

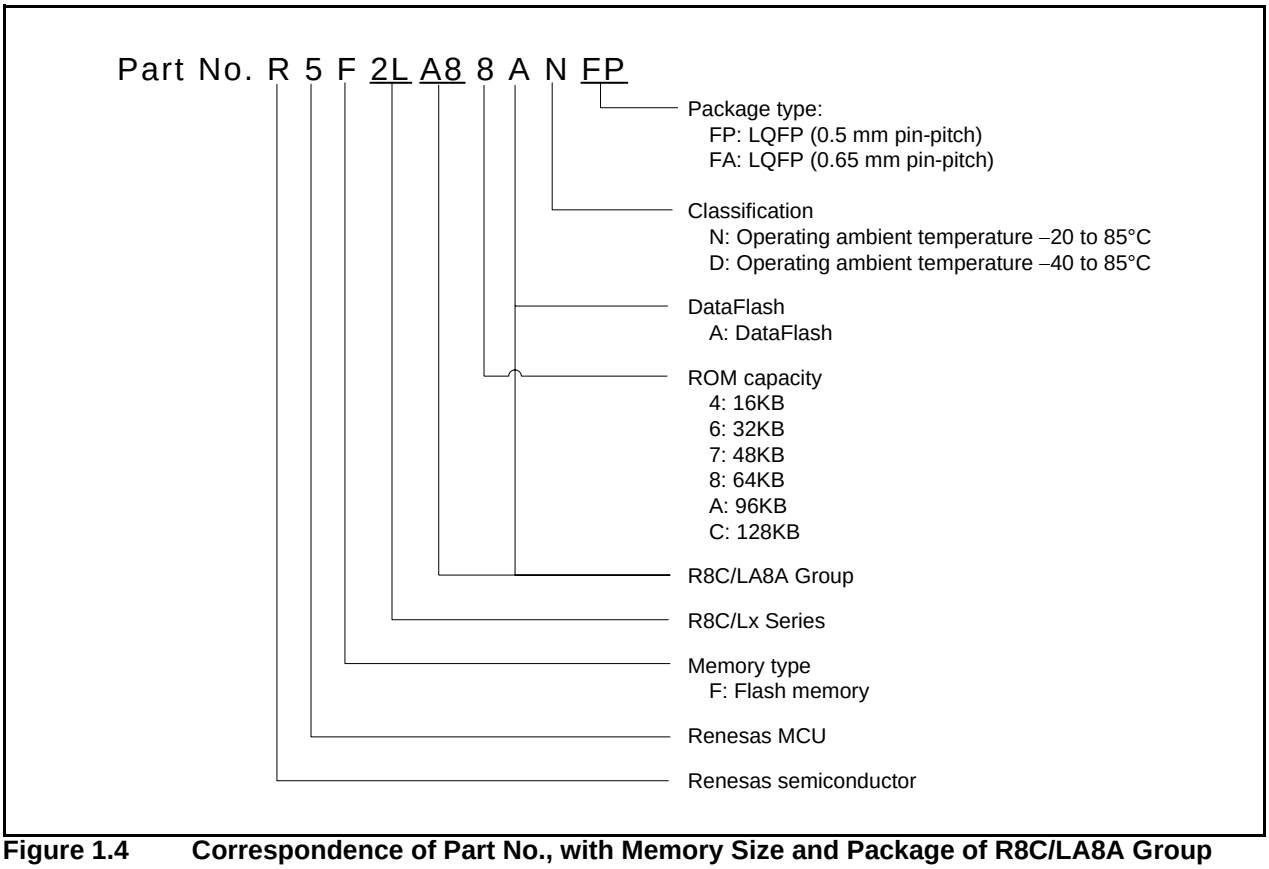


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/LA8A Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/LA3A Group. Figure 1.6 shows a Block Diagram of R8C/LA5A Group. Figure 1.7 shows a Block Diagram of R8C/LA6A Group. Figure 1.8 shows a Block Diagram of R8C/LA8A Group.

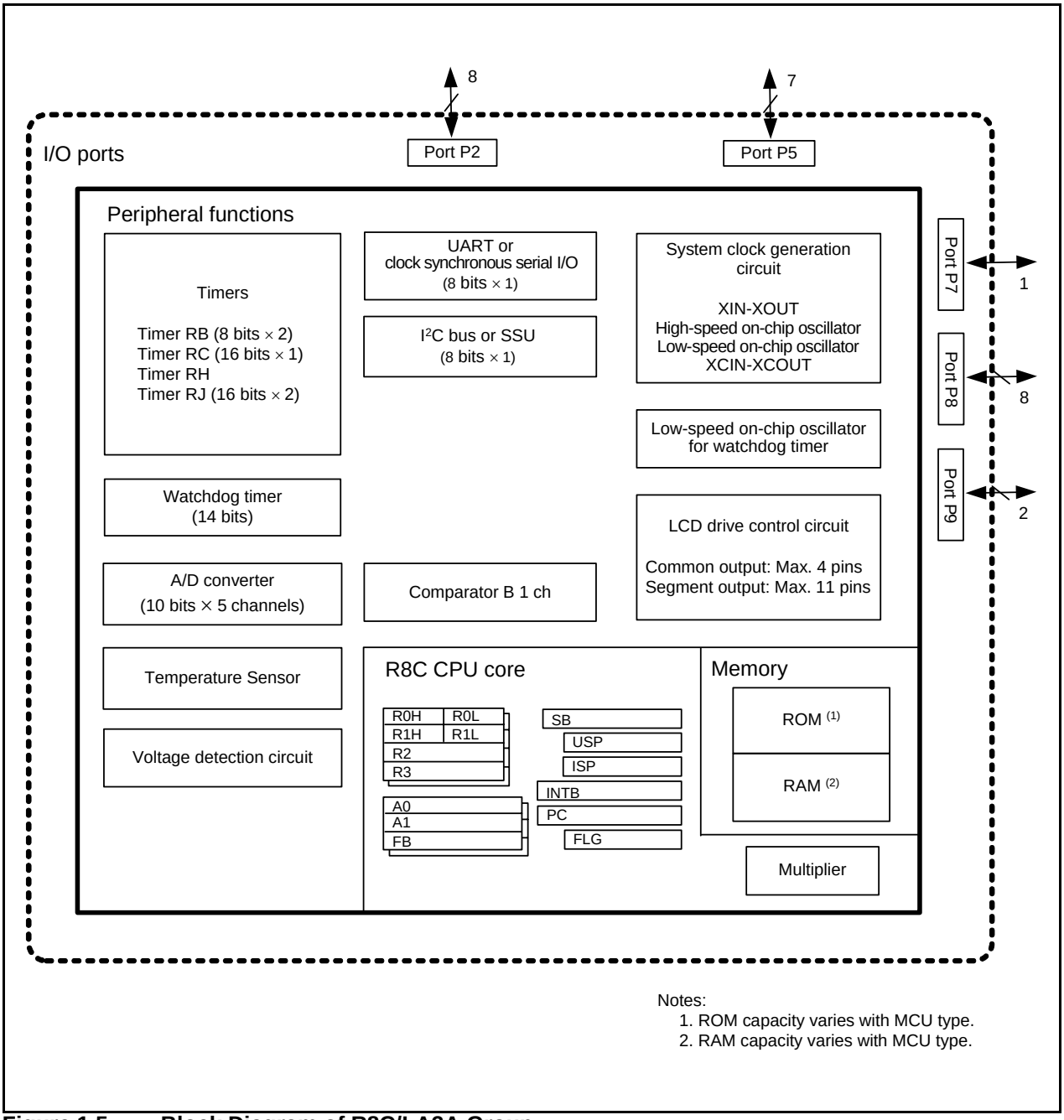
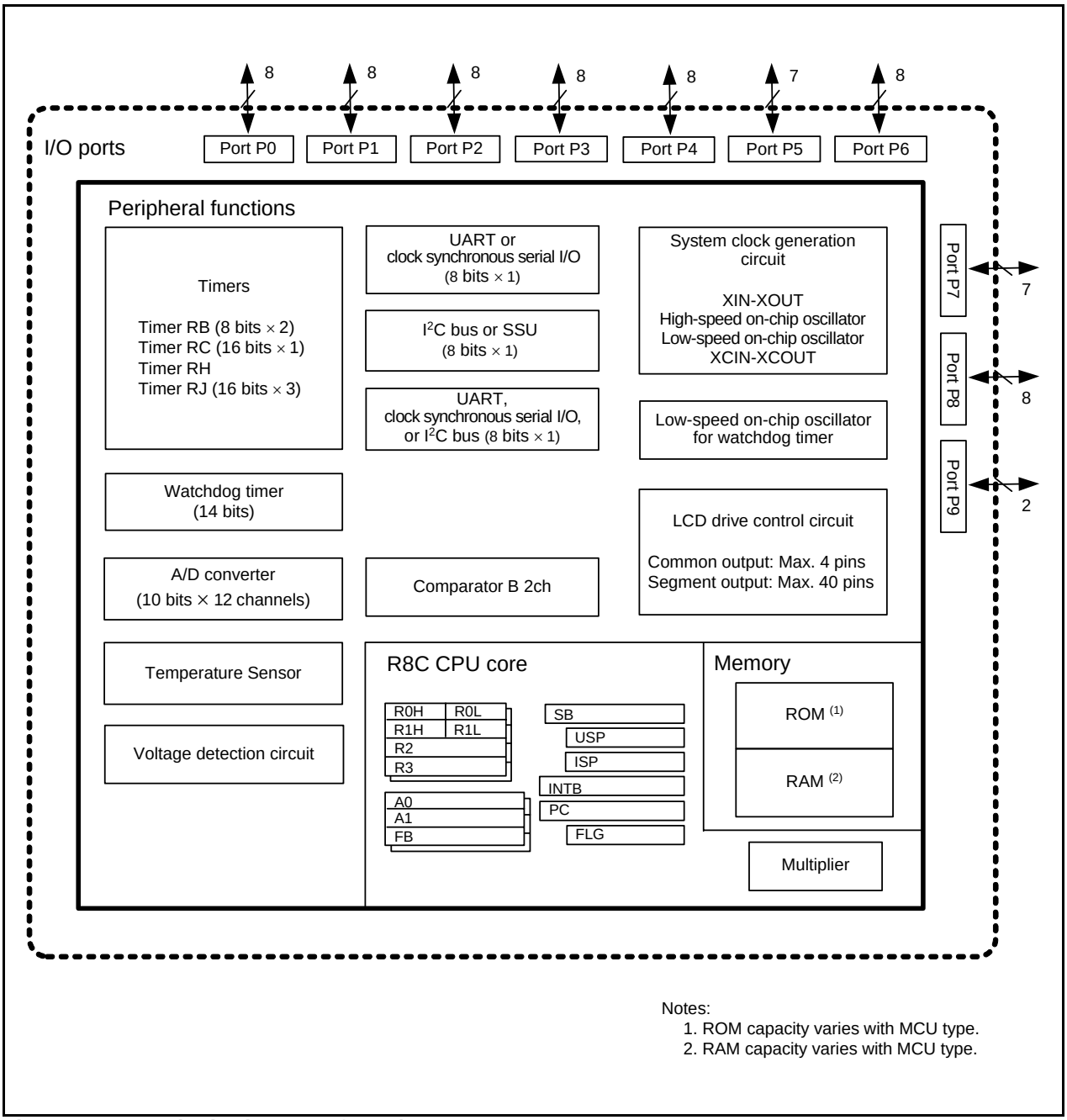


Figure 1.5 Block Diagram of R8C/LA3A Group

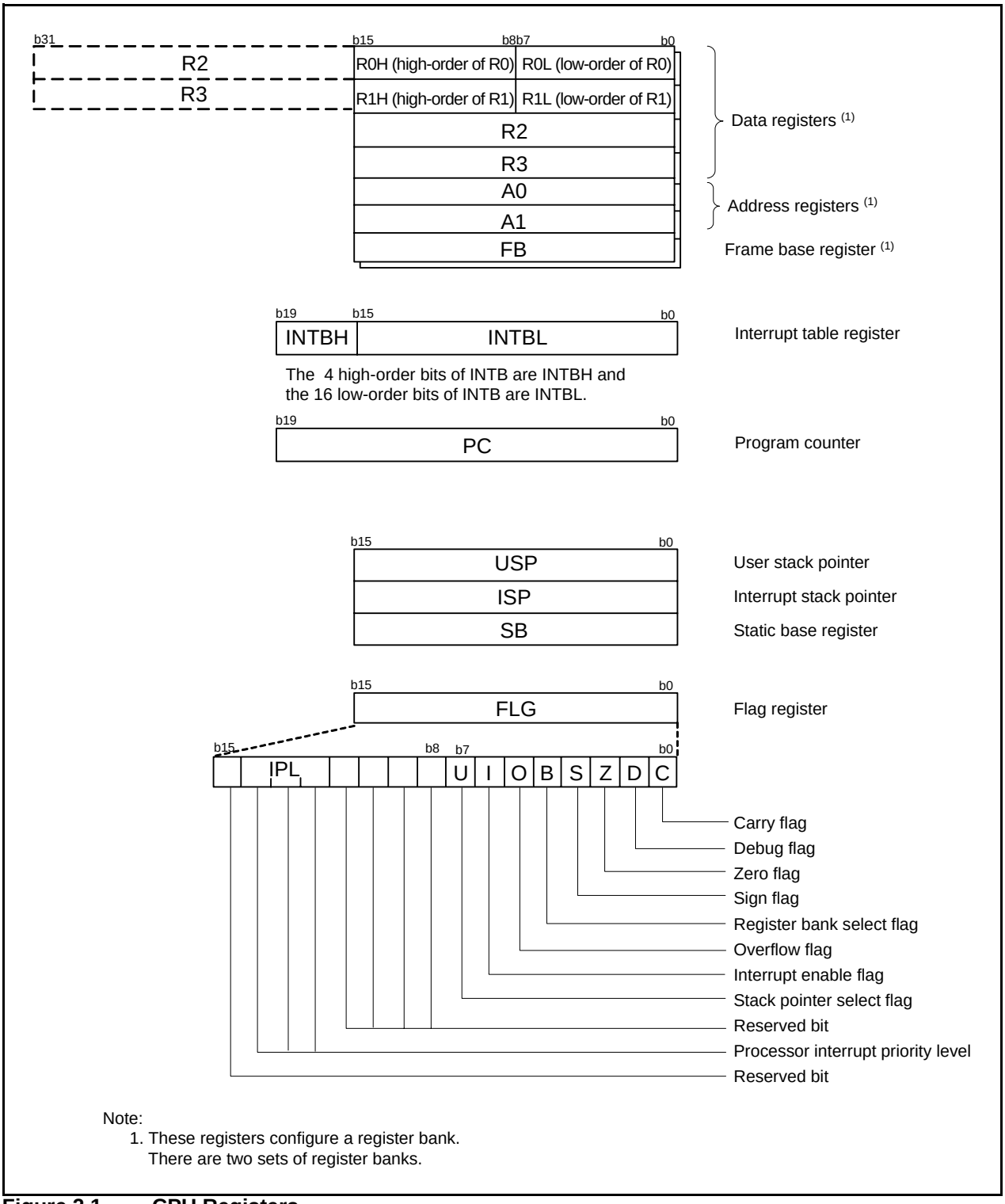


Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.8 Block Diagram of R8C/LA8A Group

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.



Note:
1. These registers configure a register bank.
There are two sets of register banks.

Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

5. Electrical Characteristics

5.1 Electrical Characteristics (R8C/LA3A Group and R8C/LA5A Group)

5.1.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG26		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40 °C ≤ T_{opr} ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

Table 5.11 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

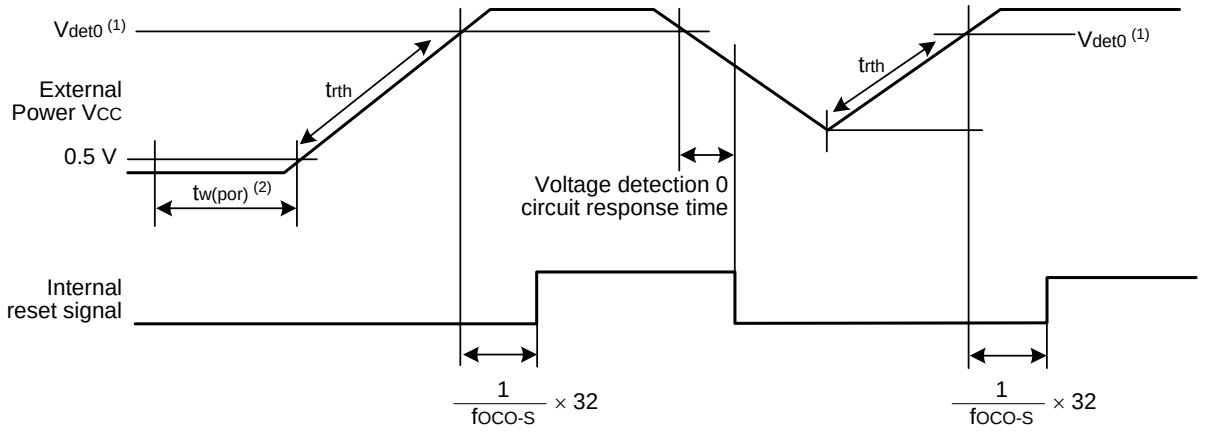
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (1)	At the falling of V_{CC}		3.70	4.0	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	200	500	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit Characteristics (1)
(T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		0	–	50000	mV/ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** in the User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Characteristics

Table 5.16 LCD Drive Control Circuit Characteristics
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL3	2.2	–	5.5	V
VL2	VL2 voltage		VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2 (2)	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(1)	–	µA

Notes:
1. Refer to Table 5.19 DC Characteristics (2), Table 5.21 DC Characteristics (4), and Table 5.23 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

Table 5.17 Power-Off Mode Characteristics
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		1.8	–	5.5	V

Table 5.19 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	63	220	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	60	220	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	46	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	4.6	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	2.4	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25 °C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85 °C	–	0.03	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C	–	1.8	6.4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C	–	2.7	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.22 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	I_{OL} = 2 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, $\overline{ADTRG}$, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V		85	220	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

5.1.5 AC Characteristics

Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

5.2.1 Absolute Maximum Ratings

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

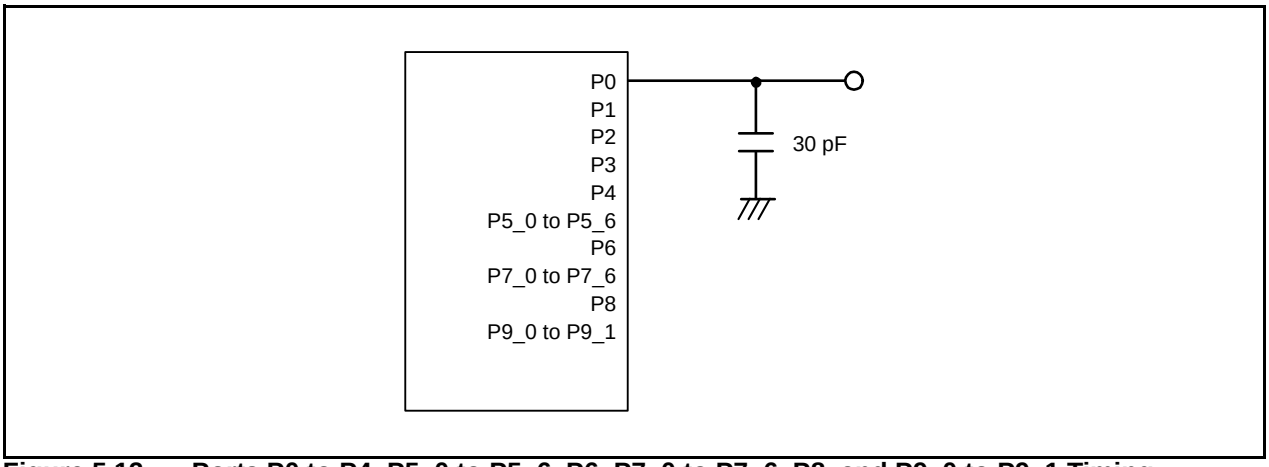


Figure 5.12 Ports P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, and P9_0 to P9_1 Timing Measurement Circuit

Table 5.37 Flash Memory (Data flash Block A and Block B) Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	µs
–	Block erase time (program/erase endurance ≤ 10,000 times)	Internal ROM Capacity: 1 KB × 2	–	0.05	1	s
		Internal ROM Capacity: 2 KB × 2	–	0.055	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		–20 (6)	–	85	°C
–	Data hold time (7)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. –40°C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

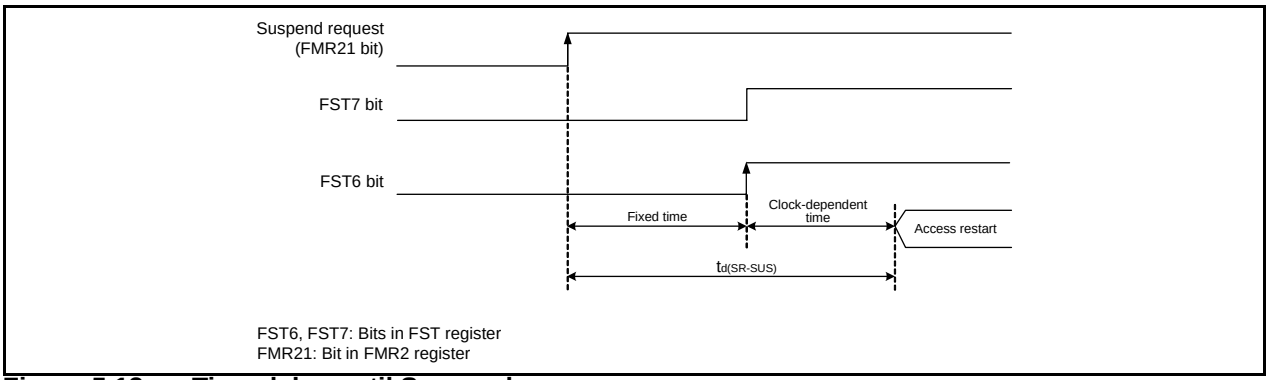


Figure 5.13 Time delay until Suspend

Table 5.40 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

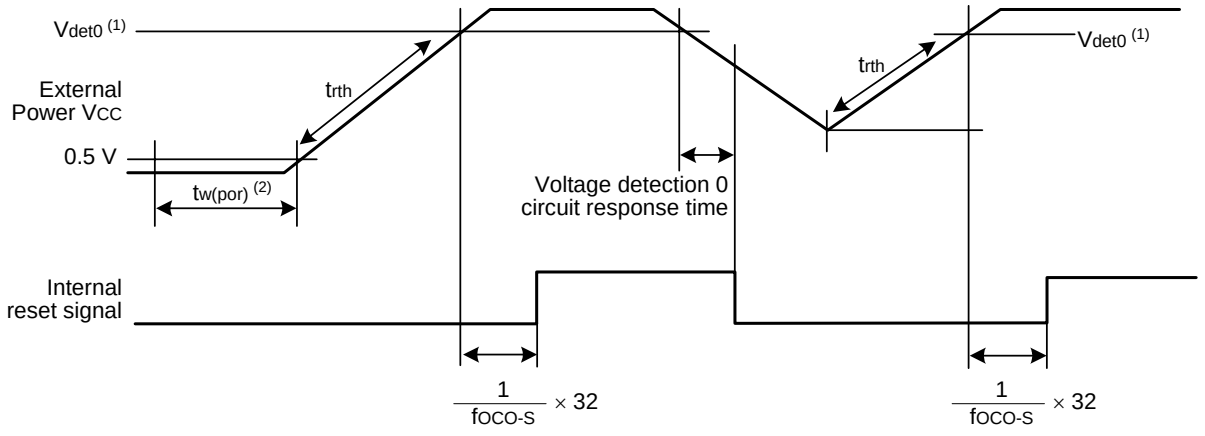
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (1)	At the falling of V_{CC}		3.70	4.0	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	200	500	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.41 Power-on Reset Circuit Characteristics (1)
(T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		0	–	50000	mV/ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** in the User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.14 Power-on Reset Circuit Characteristics

Table 5.45 LCD Drive Control Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL3	2.2	–	5.5	V
VL2	VL2 voltage		VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2 (2)	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(1)	–	µA

Notes:
1. Refer to Table 5.48 DC Characteristics (2), Table 5.50 DC Characteristics (4), and Table 5.52 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

Table 5.46 Power-Off Mode Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		1.8	–	5.5	V

Table 5.50 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	6	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	2.9	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	10 MHz	125 kHz	No division	–		–	2.9	–	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	–		–	1.5	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	3.1	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.3	4.5	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.2	–	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.52 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	–		–	2.1	–	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	–		–	0.9	–	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	–		–	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	–		–	1.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	2.4	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.2	4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2	–	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open.The standard value does not include the current that flows through external division resistors.

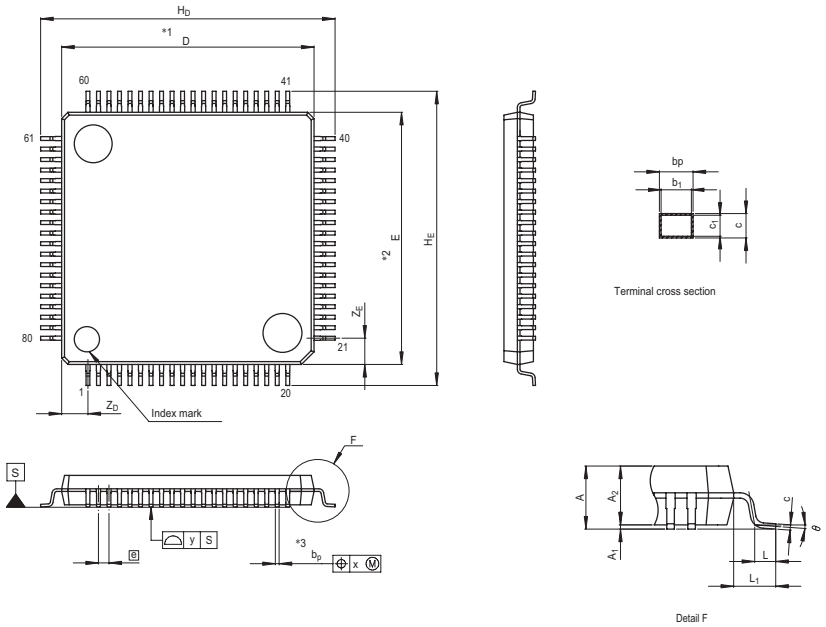
5.2.5 AC Characteristics

Table 5.53 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

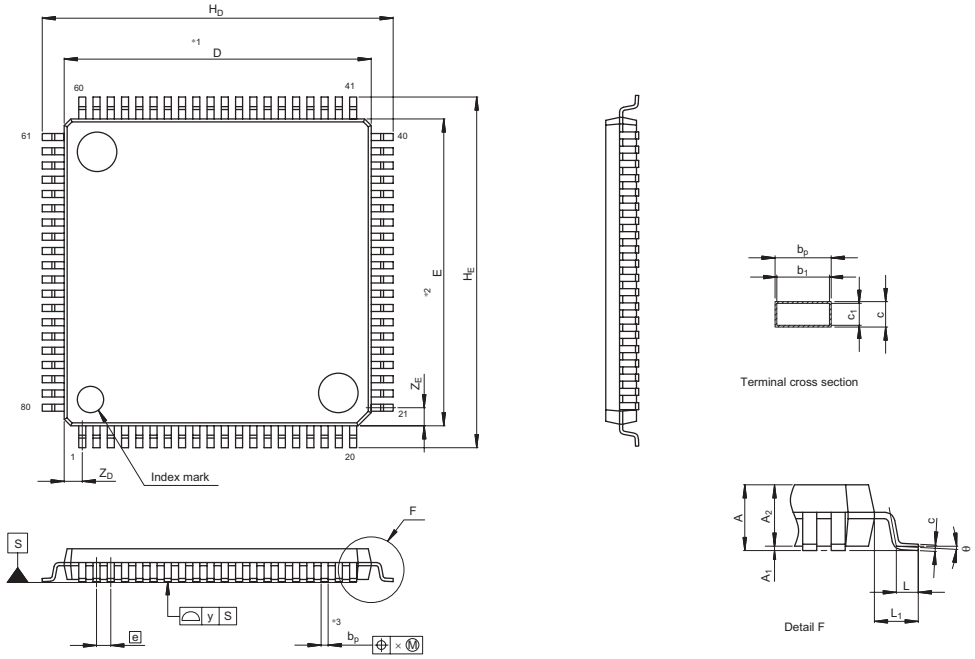
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—