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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la64anfa-u0

Table 1.2 Programmable I/O Ports Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Programmable I/O Port	R8C/LA3A Group Total: 26 I/O pins								R8C/LA5A Group Total: 44 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	✓	—	—	—	—	—	—	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.

Table 1.3 Programmable I/O Ports Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the P7DRR register. When read, the content is 0.

Table 1.7 Specifications (2)

Item	Function		Specification		
Timer	Timer RB0, Timer RB1		8 bits × 2 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode		
	Timer RC		16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)		
	Timer RH		Real-time clock mode (counting of seconds, minutes, hours, day of the week, date, month, year), output compare mode		
	Timer RJ0 Timer RJ1 Timer RJ2	R8C/LA3A Group	Timer RJ0, Timer RJ1	16 bits × 2	Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
		R8C/LA5A Group			
	R8C/LA6A Group				
	R8C/LA8A Group	Timer RJ0, Timer RJ1, Timer RJ2	16 bits × 3		
Serial Interface	UART0		1 channel Clock synchronous serial I/O/UART		
	UART2		1 channel Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function		
Synchronous Serial Communication Unit (SSU)			1 (shared with I ² C-bus)		
I ² C bus			1 (shared with SSU)		
A/D Converter	R8C/LA3A Group		10-bit resolution × 5 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA5A Group		10-bit resolution × 7 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA6A Group		10-bit resolution × 8 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA8A Group		10-bit resolution × 12 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
Comparator B	R8C/LA3A Group		1 circuit (comparator B1)		
	R8C/LA5A Group		2 circuits (comparator B1, comparator B3)		
	R8C/LA6A Group				
	R8C/LA8A Group				

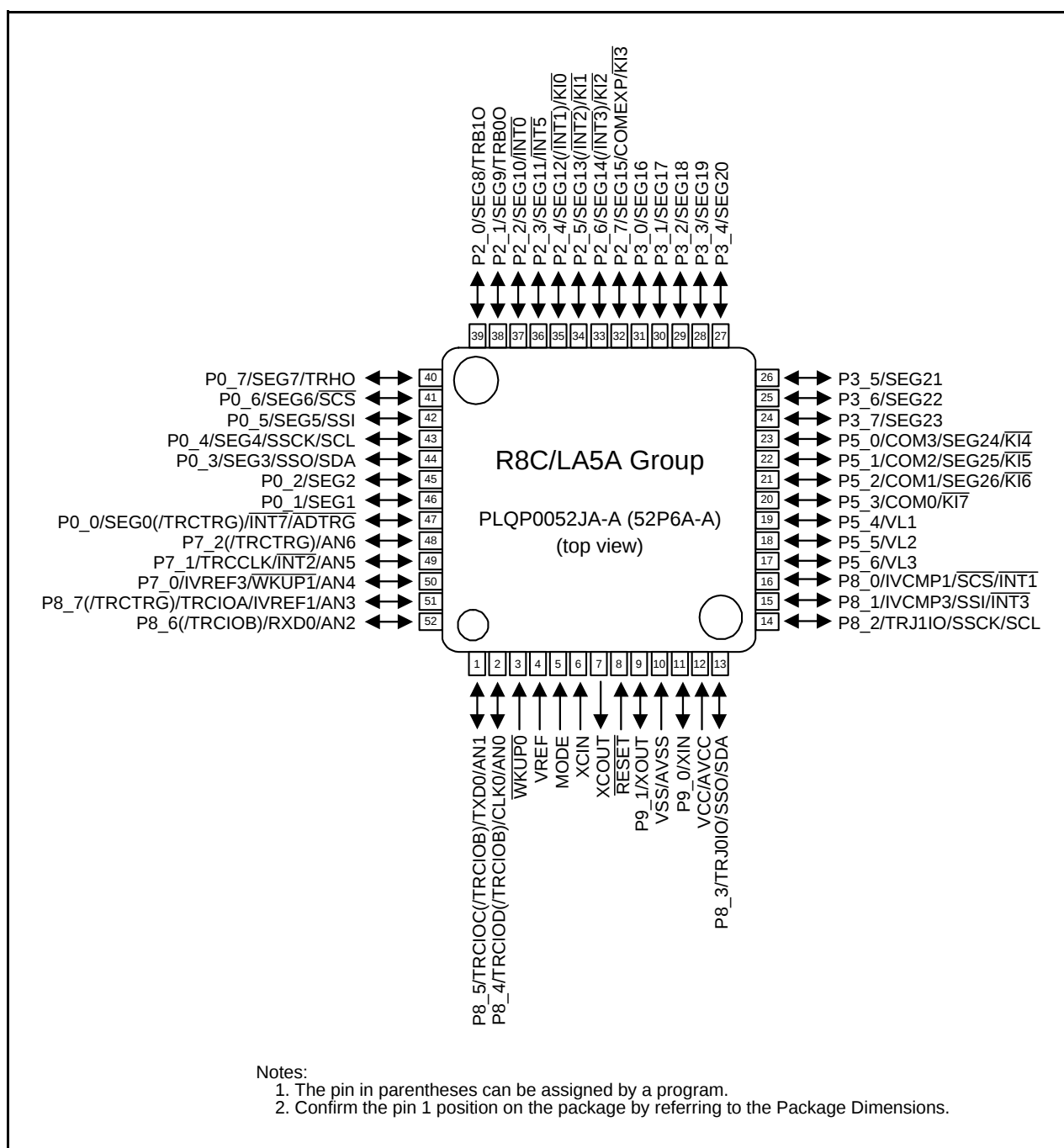


Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package

Table 1.14 Pin Name Information by Pin Number (R8C/LA3A Group, R8C/LA5A Group)(2)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA5A	LA3A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
31			P3_0							SEG16
32	19		P2_7	$\overline{KI3}$						SEG15/ COMEXP
33	20		P2_6	$\overline{(INT3)/KI2}$						SEG14
34	21		P2_5	$\overline{(INT2)/KI1}$						SEG13
35	22		P2_4	$\overline{(INT1)/KI0}$						SEG12
36	23		P2_3	$\overline{INT5}$						SEG11
37	24		P2_2	$\overline{INT0}$						SEG10
38	25		P2_1		TRB0O					SEG9
39	26		P2_0		TRB1O					SEG8
40			P0_7		TRHO					SEG7
41			P0_6				$\overline{SCS}$			SEG6
42			P0_5				SSI			SEG5
43			P0_4				SSCK	SCL		SEG4
44			P0_3				SSO	SDA		SEG3
45			P0_2							SEG2
46			P0_1							SEG1
47			P0_0	$\overline{INT7}$	(TRCTRG)				$\overline{ADTRG}$	SEG0
48			P7_2		(TRCTRG)				AN6	
49	27		P7_1	$\overline{INT2}$	TRCCLK				AN5	
50		$\overline{WKUP1}$	P7_0						AN4/IVREF3	
51	28		P8_7		TRCIOA/ (TRCTRG)				AN3/IVREF1	
52	29		P8_6		(TRCIOB)	RXD0			AN2	

Note:

1. The pin in parentheses can be assigned by a program.

Table 1.17 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(3)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
69	58		P6_6		(TRB00/ TRCIOB/ TRCIOB)				AN9/IVREF3	
70	59		P6_5		(TRB10/ TRCIOB/ TRCIOD)				AN8/IVREF1	
71	60		P6_4				(SSO)	(SDA)	AN7	
72	61		P6_3				(SSCK)	(SCL)	AN6	
73	62		P6_2		(TRJ0IO)		(SSI)		AN5	
74	63		P6_1		(TRJ1IO)		(SCS)		AN4	
75			P6_0		(TRJ2IO)				AN3	
76			P7_6		(TRB00)				AN2	
77			P7_5		TRB10				AN1	
78			P7_4						AN0	
79			P7_3			(CTS2/RTS2)				
80			P7_2		TRJ00	(RXD2/SCL2/ TXD2/SDA2)				

Note:

1. The pin in parentheses can be assigned by a program.

1.5 Pin Functions

Tables 1.18 and 1.19 list Pin Functions for R8C/LA5A Group, and Tables 1.20 and 1.21 list Pin Functions for R8C/LA8A Group.

Table 1.18 Pin Functions for R8C/LA5A Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	WKUP0	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$, $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RB	TRB0O, TRB1O	O	Timer RB output pins.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RH	TRHO	O	Timer RH output pin.
Timer RJ	TRJ0IO, TRJ1IO	I/O	Timer RJ I/O pins.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.20 Pin Functions for R8C/LA8A Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUNT. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUNT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RB	TRB0O, TRB1O	O	Timer RB output pins.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRIG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RH	TRHO	O	Timer RH output pin.
Timer RJ	TRJ0IO, TRJ1IO, TRJ2IO	I/O	Timer RJ I/O pins.
	TRJ0IO, TRJ1IO, TRJ2IO	O	Timer RJ output pins.
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pin.
	RXD0, RXD2	I	Serial data input pin.
	TXD0, TXD2	O	Serial data output pin.
	$\overline{\text{CTS2}}$	I	Transmission control input pin.
	$\overline{\text{RTS2}}$	O	Reception control output pin.
	SCL2	I/O	I ² C mode clock I/O pin.
	SDA2	I/O	I ² C mode data I/O pin.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 4.5 SFR Information for R8C/LA5A Group (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h ⁽²⁾
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h ⁽²⁾
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h ⁽²⁾
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h ⁽²⁾
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b ⁽²⁾
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b ⁽²⁾
0116h	Timer RH Year Data Register	TRHYR	XXh 00h ⁽²⁾
0117h	Timer RH Control Register	TRHCR	XX0000Xb 000XX1X0b ⁽²⁾
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb ⁽²⁾
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h ⁽²⁾
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b ⁽²⁾
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h ⁽²⁾
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h ⁽²⁾
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h ⁽²⁾
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h ⁽²⁾
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b ⁽²⁾
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h 00h
0127h			
0128h	Timer RC General Register A	TRCGRA	FFh FFh
0129h			
012Ah	Timer RC General Register B	TRCGRB	FFh FFh
012Bh			
012Ch	Timer RC General Register C	TRCGRC	FFh FFh
012Dh			
012Eh	Timer RC General Register D	TRCGRD	FFh FFh
012Fh			
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.11 SFR Information for R8C/LA8A Group (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch	Timer RJ2 Interrupt Control Register	TRJ2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.16 SFR Information for R8C/LA8A Group (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h	Timer RB Pin Select Register	TRBSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b ⁽³⁾
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.19 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FFEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.9 Voltage Detection 0 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	50	500	μs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	100	500	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (2)			—	—	100	μs

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽¹⁾	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽¹⁾	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽¹⁾	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽¹⁾	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽¹⁾	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽¹⁾	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽¹⁾	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽¹⁾	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽¹⁾	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽¹⁾	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽¹⁾	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽¹⁾	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽¹⁾	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽¹⁾	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽¹⁾	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽¹⁾	At the falling of Vcc		4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		—	0.07	—	V
		Vdet1_6 to Vdet1_F selected		—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽²⁾	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	μs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	250	500	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾			—	—	100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.22 DC Characteristics (5) [1.8 V ≤ V_{CC} < 2.7 V]
(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 ⁽¹⁾	I _{OH} = −2 mA	V _{CC} − 0.5	—	V _{CC}	V
			Other pins	I _{OH} = −1 mA	V _{CC} − 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 ⁽¹⁾	I _{OL} = 2 mA	—	—	0.5	V
			Other pins	I _{OL} = 1 mA	—	—	0.5	V
V _{T+} –V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	—	V
		RESET, WKUP0			0.1	0.8	—	V
I _{IH}	Input "H" current		V _I = 1.8 V, V _{CC} = 1.8 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 1.8 V		—	—	−4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 1.8 V		85	220	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	2.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

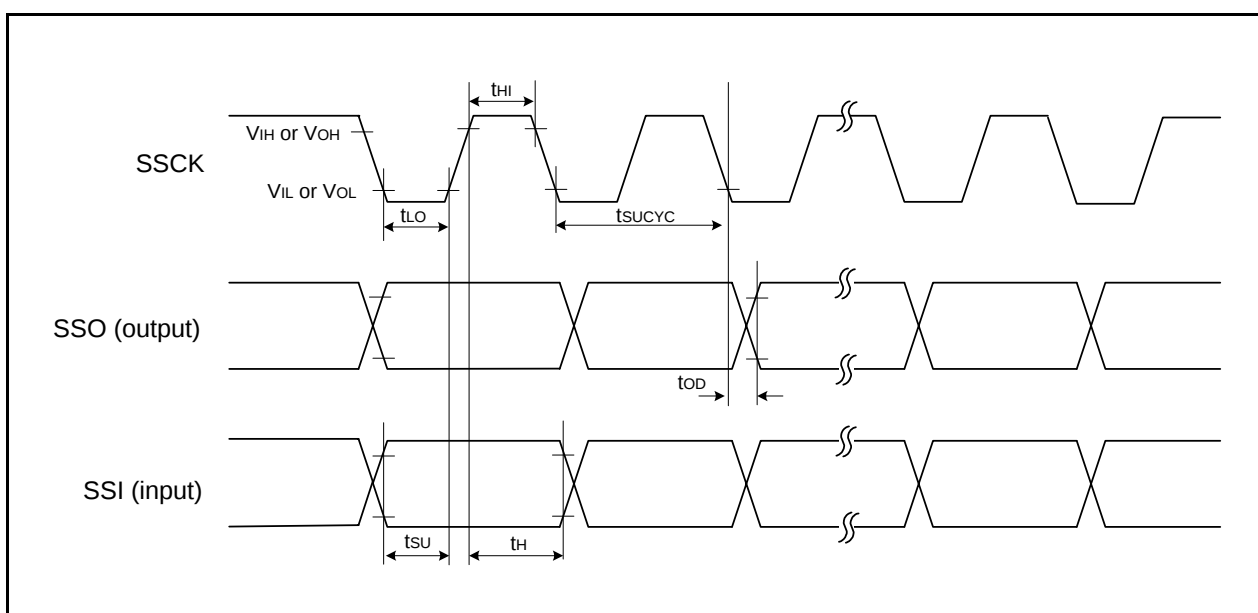


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

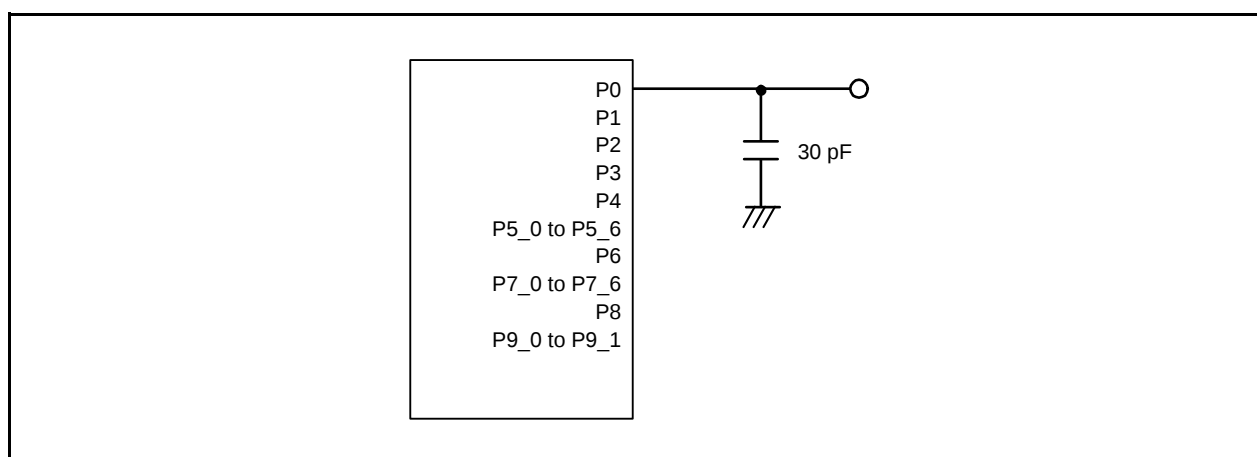


Figure 5.12 Ports P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, and P9_0 to P9_1 Timing Measurement Circuit

Table 5.49 DC Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.0\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output "H" voltage		Port P7_0, P7_1, P8 (1)	$I_{OH} = -5\text{ mA}$	$V_{CC} - 0.5$	–	V_{CC}
			Other pins	$I_{OH} = -1\text{ mA}$	$V_{CC} - 0.5$	–	V_{CC}
VOL	Output "L" voltage		Port P7_0, P7_1, P8 (1)	$I_{OL} = 5\text{ mA}$	–	–	0.5
			Other pins	$I_{OL} = 1\text{ mA}$	–	–	0.5
VT+·VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO		0.05	0.4	–	V
		RESET, WKUP0		0.1	0.8	–	V
I _{IH}	Input "H" current		$V_I = 3\text{ V}, V_{CC} = 3\text{ V}$		–	–	5.0
I _{IL}	Input "L" current		$V_I = 0\text{ V}, V_{CC} = 3\text{ V}$		–	–	–5.0
R _{PULLUP}	Pull-up resistance		$V_I = 0\text{ V}, V_{CC} = 3\text{ V}$		25	80	140
R _{FXIN}	Feedback resistance	XIN			–	2.0	–
R _{FXCIN}	Feedback resistance	XCIN			–	14	–
V _{RAM}	RAM hold voltage		During stop mode		1.8	–	–

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DDR and P8DDR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.50 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]
(T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit		
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)		Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed									
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	4.7	10	mA	
			10 MHz	Off	Off	125 kHz	No division	—			—	2.3	6	mA	
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled		—	2.9	—	mA	
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.8	—	mA	
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.0	—	mA	
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	5.0	11	mA	
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	2.1	—	mA	
			Off	Off	10 MHz	125 kHz	No division	—			—	2.9	—	mA	
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.5	—	mA	
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh			—	0.9	—	mA	
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0			—	106	300	μA	
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	54	200	μA	
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	54	200	μA	
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	36	—	μA	
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	9.0	50	μA	
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	2.5	31	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	3.1	—	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode		—	1.7	—	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM10 = 1	While a WAIT instruction is executed Peripheral clock off		—	0.5	2.2	μA	
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	0.5	2.2	μA	
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	1.2	—	μA	
		Power-off mode	Off	Off	Off	Off	—	—		Power-off 0 Topr = 25°C		—	0.01	0.1	μA
			Off	Off	Off	Off	—	—		Power-off 0 Topr = 85°C		—	0.02	—	μA
Off	32 kHz		Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C		—	1.3	4.5	μA			
Off	32 kHz		Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C		—	2.2	—	μA			

Notes:

1. V_{CC} = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V_{SS}.
2. XIN is set to square wave input.
3. V_{CC} = 3.0 V
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.51 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage		Port P7_0, P7_1, P8 (1)	IOH = −2 mA	Vcc − 0.5	−	Vcc	V
			Other pins	IOH = −1 mA	Vcc − 0.5	−	Vcc	V
VOL	Output “L” voltage		Port P7_0, P7_1, P8 (1)	IOL = 2 mA	−	−	0.5	V
			Other pins	IOL = 1 mA	−	−	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0			0.1	0.8	−	V
IIH	Input “H” current		VI = 1.8 V, Vcc = 1.8 V		−	−	4.0	μA
IIL	Input “L” current		VI = 0 V, Vcc = 1.8 V		−	−	−4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 1.8 V		85	220	500	kΩ
RfXIN	Feedback resistance	XIN			−	2.0	−	MΩ
RfXCIN	Feedback resistance	XCIN			−	14	−	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7D_{RR} and P8D_{RR}. When the drive capacity is set to Low, the value of any other pin applies.

5.2.5 AC Characteristics

Table 5.53 Timing Requirements of Synchronous Serial Communication Unit (SSU)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (1)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (1)
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	—	—	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1tcyc + 20	ns
tSA	SSI slave access time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	1.5tcyc + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5tcyc + 200	ns
tOR	SSI slave out open time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	1.5tcyc + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5tcyc + 200	ns

Note:

1. $1\text{tcyc} = 1/f_1(\text{s})$

Table 5.55 Timing Requirements of External Clock Input (XIN, XCIN)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tc(XIN)	XIN input cycle time	200	—	50	—	50	—	ns
tWH(XIN)	XIN input “H” width	90	—	24	—	24	—	ns
tWL(XIN)	XIN input “L” width	90	—	24	—	24	—	ns
tc(XCIN)	XCIN input cycle time	20	—	20	—	20	—	μs
tWH(XCIN)	XCIN input “H” width	10	—	10	—	10	—	μs
tWL(XCIN)	XCIN input “L” width	10	—	10	—	10	—	μs

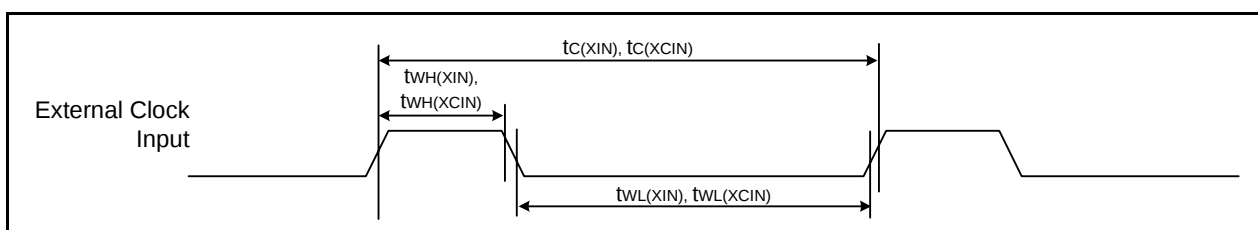


Figure 5.19 External Clock Input Timing

Table 5.56 Timing Requirements of TRJiIO (i = 0 to 2)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRJiO)	TRJiO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRJiO)	TRJiO input “H” width	200	—	120	—	40	—	ns
t _{WL} (TRJiO)	TRJiO input “L” width	200	—	120	—	40	—	ns

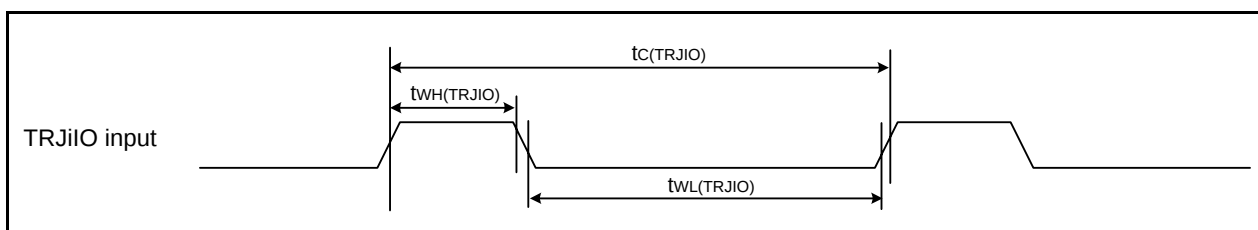


Figure 5.20 Input Timing of TRJiIO