# Renesas Electronics America Inc - R5F2LA66ANFP#30 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | LCD, POR, PWM, Voltage Detect, WDT |
| Number of I/O | 56 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la66anfp-30 |

### 1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.
Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

**Table 1.1 Differences between Groups**

| Item | Function | R8C/LA3A Group | R8C/LA5A Group | R8C/LA6A Group | R8C/LA8A Group |
|---|---|---|---|---|---|
| I/O Ports | Programmable I/O ports | 26 pins | 44 pins | 56 pins | 72 pins |
| | High current drive ports | 8 pins | 8 pins | 8 pins | 10 pins |
| Interrupts | $\overline{\text{INT}}$ interrupt pins | 5 pins | 6 pins | 8 pins | 8 pins |
| Timer RJ | Timer RJ0 output pin | None | None | None | 1 pin |
| | Timer RJ1 output pin | None | None | None | 1 pin |
| | Timer RJ2 I/O pin | None | None | None | 1 pin |
| | Timer RJ2 output pin | None | None | None | 1 pin |
| Timer RH | Timer RH output pin | None | 1 pin | 1 pin | 1 pin |
| Serial interface | UART2 | None | None | 1 pin | 1 pin |
| A/D Converter | Analog input pins | 5 pins | 7 pins | 8 pins | 12 pins |
| LCD Drive Control Circuit | Segment output pins | Max. 11 pins | Max. 27 pins | Max. 32 pins | Max. 40 pins |
| Comparator B | Analog input voltage | 1 pin | 2 pins | 2 pins | 2 pins |
| | Reference input voltage | 1 pin | 2 pins | 2 pins | 2 pins |
| Clock | XCIN pin | Shared with XIN pin | Dedicated pin | Dedicated pin | Dedicated pin |
| | XCOUT pin | Shared with XOUT pin | Dedicated pin | Dedicated pin | Dedicated pin |
| Packages | | 32-pin LQFP | 52-pin LQFP | 64-pin LQFP | 80-pin LQFP |

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

### 1.1.3 Specifications

Tables 1.6 to 1.8 list the specifications.

**Table 1.6 Specifications (1)**

| Item | Function | | Specification |
|---|---|---|---|
| CPU | Central processing unit | | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V)<br>125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM/RAM<br>Data flash | | Refer to Tables 1.9 to 1.12 Product Lists. |
| Power Supply Voltage Detection | Voltage detection circuit | | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | R8C/LA3A Group | • CMOS I/O ports: 26, selectable pull-up resistor (1)<br>• High current drive ports: 8 |
| | | R8C/LA5A Group | • CMOS I/O ports: 44, selectable pull-up resistor (1)<br>• High current drive ports: 8 |
| | | R8C/LA6A Group | • CMOS I/O ports: 56, selectable pull-up resistor (1)<br>• High current drive ports: 8 |
| | | R8C/LA8A Group | • CMOS I/O ports: 72, selectable pull-up resistor (1)<br>• High current drive ports: 10 |
| Clock | Clock generation circuits | | 4 circuits: XIN clock oscillation circuit<br>XCIN clock oscillation circuit (32 kHz)<br>High-speed on-chip oscillator (with frequency adjustment function)<br>Low-speed on-chip oscillator<br>• Oscillation stop detection:<br>XIN clock oscillation stop detection function<br>• Frequency divider circuit:<br>Division ratio selectable from 1, 2, 4, 8, and 16<br>• Low-power-consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode |
| | | | Real-time clock (timer RH) |
| Interrupts | | R8C/LA3A Group | • Number of interrupt vectors: 69<br>• External Interrupt: 13 ($\overline{\text{INT}}$ × 5, key input × 8)<br>• Priority levels: 7 levels |
| | | R8C/LA5A Group | • Number of interrupt vectors: 69<br>• External Interrupt: 14 ($\overline{\text{INT}}$ × 6, key input × 8)<br>• Priority levels: 7 levels |
| | | R8C/LA6A Group | • Number of interrupt vectors: 69<br>• External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8)<br>• Priority levels: 7 levels |
| | | R8C/LA8A Group | |
| Watchdog Timer | | | • 14 bits × 1 (with prescaler)<br>• Selectable reset start function<br>• Selectable low-speed on-chip oscillator for watchdog timer |

Note:
1. No pull-up resistor is provided in the pins P5_4 to P5_6.

**Table 1.11 Product List for R8C/LA6A Group** **Current of Oct 2011**

| Part No. | Internal ROM Capacity | | Internal RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data Flash | | | |
| R5F2LA64ANFP | 16 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064KB-A | N Version |
| R5F2LA64ANFA | 16 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064GA-A | |
| R5F2LA66ANFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064KB-A | |
| R5F2LA66ANFA | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064GA-A | |
| R5F2LA67ANFP | 48 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064KB-A | |
| R5F2LA67ANFA | 48 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064GA-A | |
| R5F2LA68ANFP | 64 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064KB-A | |
| R5F2LA68ANFA | 64 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064GA-A | |
| R5F2LA6AANFP | 96 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064KB-A | |
| R5F2LA6AANFA | 96 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064GA-A | |
| R5F2LA6CANFP | 128 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064KB-A | |
| R5F2LA6CANFA | 128 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064GA-A | |
| R5F2LA64ADFP | 16 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064KB-A | D Version |
| R5F2LA64ADFA | 16 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064GA-A | |
| R5F2LA66ADFP | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064KB-A | |
| R5F2LA66ADFA | 32 Kbytes | 1 Kbyte × 2 | 2 Kbytes | PLQP0064GA-A | |
| R5F2LA67ADFP | 48 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064KB-A | |
| R5F2LA67ADFA | 48 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064GA-A | |
| R5F2LA68ADFP | 64 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064KB-A | |
| R5F2LA68ADFA | 64 Kbytes | 1 Kbyte × 2 | 3.5 Kbytes | PLQP0064GA-A | |
| R5F2LA6AADFP | 96 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064KB-A | |
| R5F2LA6AADFA | 96 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064GA-A | |
| R5F2LA6CADFP | 128 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064KB-A | |
| R5F2LA6CADFA | 128 Kbytes | 2 Kbytes × 2 | 5.5 Kbytes | PLQP0064GA-A | |

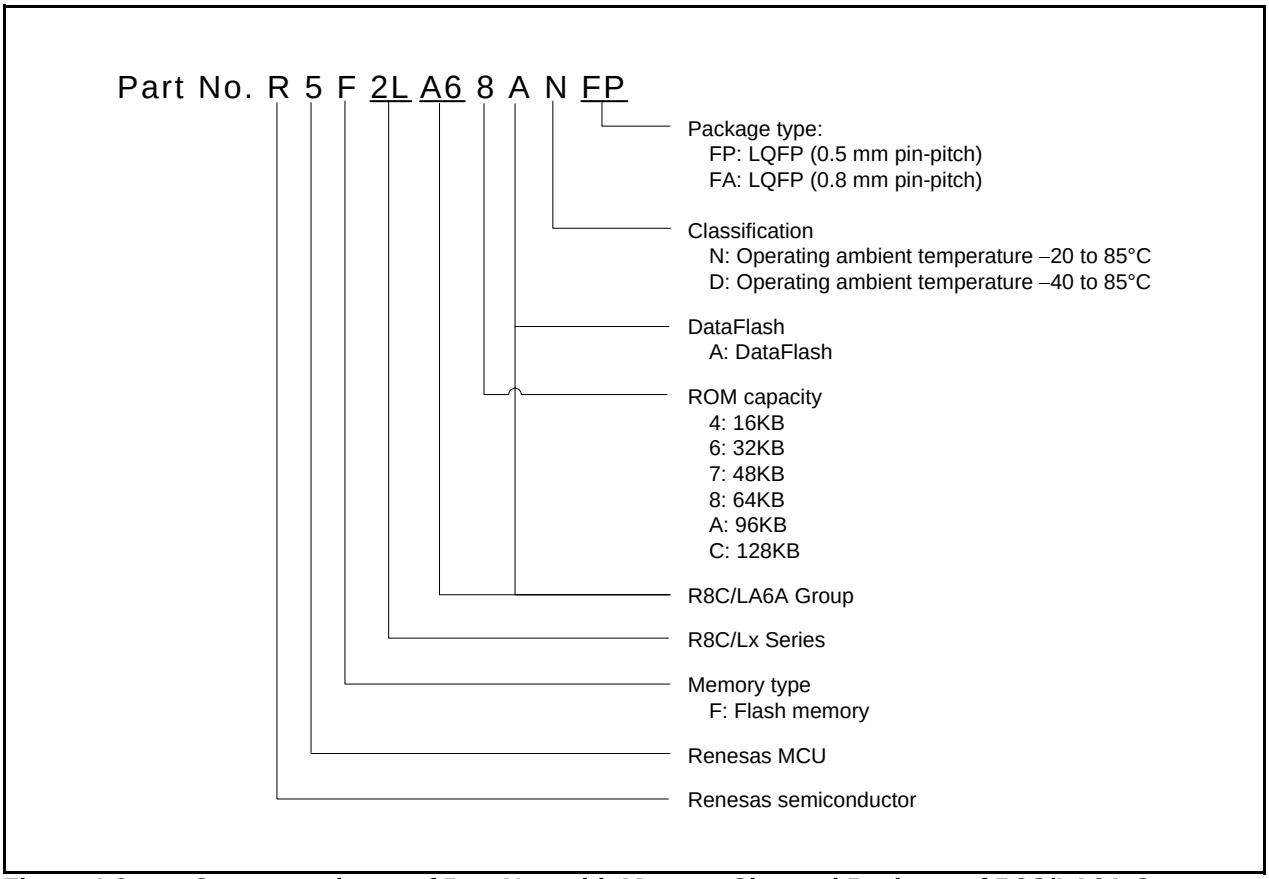
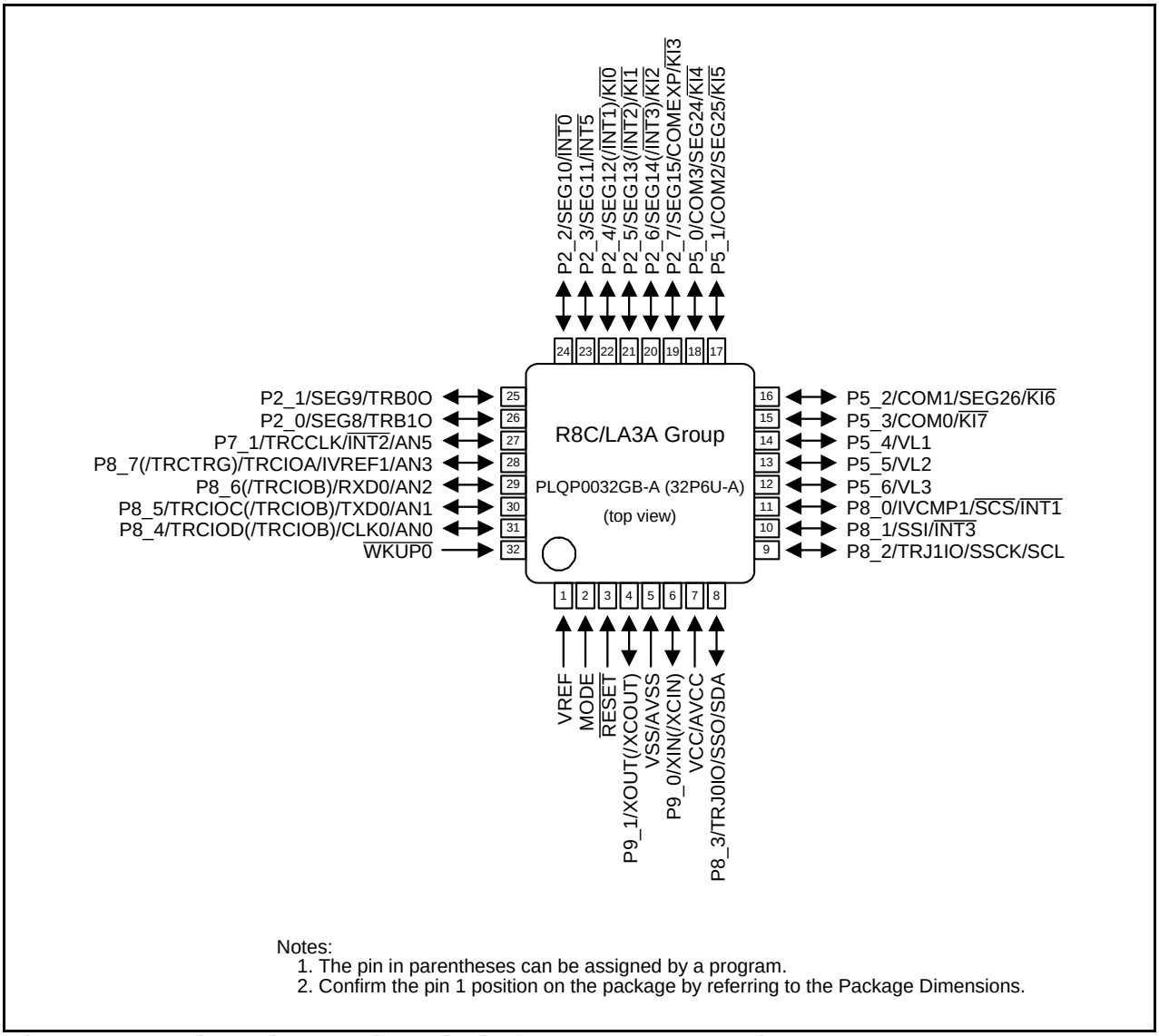



**Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group**

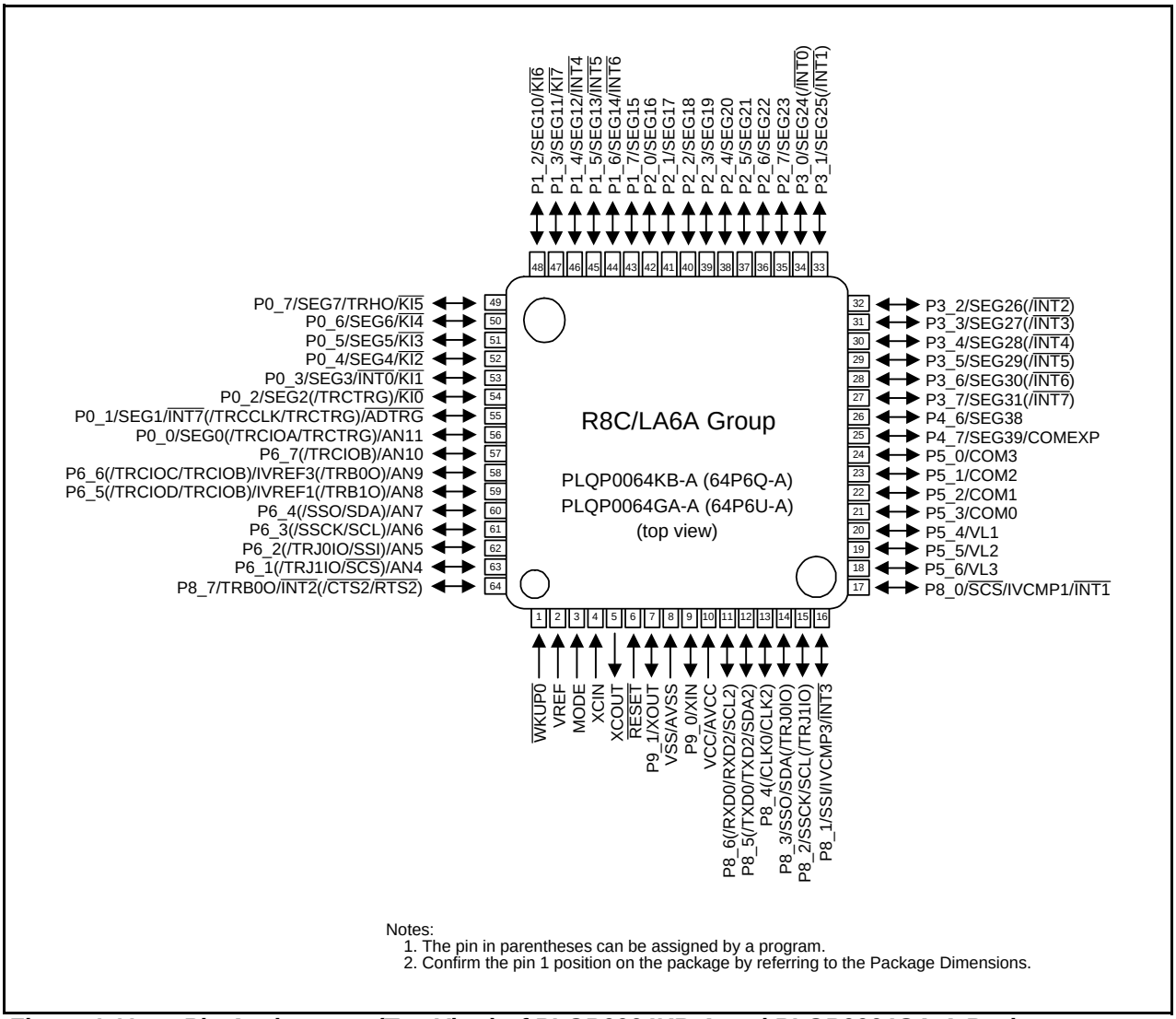
## 1.4 Pin Assignments

Figures 1.9 to 1.12 show pin assignments (top view). Tables 1.13 to 1.17 list the pin name information by pin number.




Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

**Figure 1.9 Pin Assignment (Top View) of PLQP0032GB-A Package**




Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

**Figure 1.11 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages**

**Table 1.15 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(1)**

| Pin Number | | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| LA8A | LA6A | | | Interrupt | Timer | Serial Interface | SSU | I²C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 1 | | | P7_1 | | TRJ1O | (TXD2/SDA2/RXD2/SCL2) | | | | |
| 2 | | $\overline{\text{WKUP1}}$ | P7_0 | | TRJ2O | (CLK2) | | | | |
| 3 | 64 | | P8_7 | $\overline{\text{INT2}}$ | TRB0O | ($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$) | | | | |
| 4 | 1 | $\overline{\text{WKUP0}}$ | | | | | | | | |
| 5 | 2 | VREF | | | | | | | | |
| 6 | 3 | MODE | | | | | | | | |
| 7 | 4 | XCIN | | | | | | | | |
| 8 | 5 | XCOUT | | | | | | | | |
| 9 | 6 | $\overline{\text{RESET}}$ | | | | | | | | |
| 10 | 7 | XOUT | P9_1 | | | | | | | |
| 11 | 8 | VSS/ AVSS | | | | | | | | |
| 12 | 9 | XIN | P9_0 | | | | | | | |
| 13 | 10 | VCC/ AVCC | | | | | | | | |
| 14 | 11 | | P8_6 | | | (RXD0/RXD2/SCL2) | | | | |
| 15 | 12 | | P8_5 | | | (TXD0/TXD2/SDA2) | | | | |
| 16 | 13 | | P8_4 | | | (CLK0/CLK2) | | | | |
| 17 | 14 | | P8_3 | | (TRJ0IO) | | SSO | SDA | | |
| 18 | 15 | | P8_2 | | (TRJ1IO) | | SSCK | SCL | | |
| 19 | 16 | | P8_1 | $\overline{\text{INT3}}$ | | | SSI | | IVCMP3 | |
| 20 | 17 | | P8_0 | $\overline{\text{INT1}}$ | | | $\overline{\text{SCS}}$ | | IVCMP1 | |
| 21 | 18 | | P5_6 | | | | | | | VL3 |
| 22 | 19 | | P5_5 | | | | | | | VL2 |
| 23 | 20 | | P5_4 | | | | | | | VL1 |
| 24 | 21 | | P5_3 | | | | | | | COM0 |
| 25 | 22 | | P5_2 | | | | | | | COM1 |
| 26 | 23 | | P5_1 | | | | | | | COM2 |
| 27 | 24 | | P5_0 | | | | | | | COM3 |
| 28 | 25 | | P4_7 | | | | | | | SEG39/ COMEXP |
| 29 | 26 | | P4_6 | | | | | | | SEG38 |
| 30 | | | P4_5 | | | | | | | SEG37 |

Note:
1. The pin in parentheses can be assigned by a program.

**Table 1.19 Pin Functions for R8C/LA5A Group (2)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| $I^2C$ bus | SCL | I/O | Clock I/O pin. |
| | SDA | I/O | Data I/O pin. |
| SSU | SSI | I/O | Data I/O pin. |
| | $\overline{SCS}$ | I/O | Chip-select signal I/O pin. |
| | SSCK | I/O | Clock I/O pin. |
| | SSO | I/O | Data I/O pin. |
| Reference voltage input | VREF | I | Reference voltage input pin for the A/D converter. |
| A/D converter | AN0 to AN6 | I | A/D converter analog input pins. |
| | $\overline{ADTRG}$ | I | AD external trigger input pin. |
| Comparator B | IVCMP1, IVCMP3 | I | Comparator B analog voltage input pins. |
| | IVREF1, IVREF3 | I | Comparator B reference voltage input pins. |
| I/O ports | P0_0 to P0_7,<br>P2_0 to P2_7,<br>P3_0 to P3_7,<br>P5_0 to P5_6,<br>P7_0 to P7_2,<br>P8_0 to P8_7,<br>P9_0, P9_1 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>Port P8 can be used as LED drive ports. |
| Segment output | SEG0 to SEG26 | O | LCD segment output pins. |
| Common output | COM0 to COM3,<br>COMEXP | O | LCD common output pins. |
| LCD power supply | VL1 | I | Apply the following voltage: 1 V ≤ VL1 ≤ VCC and VL1 ≤ VL2. |
| | VL2 | I | Apply the following voltage: VL2 ≤ 5.5 V and VL1 ≤ VL2 ≤ VL3. |
| | VL3 | I | Apply the following voltage: VL3 ≤ 5.5 V and VL2 ≤ VL3. |

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.20 Pin Functions for R8C/LA8A Group (1)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | — | Apply 1.8 V to 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | — | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Driving this pin low resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| Power-off 0 mode exit input | $\overline{\text{WKUP0}}$ | I | This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode. |
| | $\overline{\text{WKUP1}}$ | I | This pin is provided for input to exit the mode used in power-off 0 mode. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling. |
| XIN clock output | XOUT | O | |
| XCIN clock input | XCIN | I | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open. |
| XCIN clock output | XCOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ | I | $\overline{\text{INT}}$ interrupt input pins. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$ | I | Key input interrupt input pins. |
| Timer RB | TRB0O, TRB1O | O | Timer RB output pins. |
| Timer RC | TRCCLK | I | External clock input pin. |
| | TRCTRG | I | External trigger input pin. |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O pins. |
| Timer RH | TRHO | O | Timer RH output pin. |
| Timer RJ | TRJ0IO, TRJ1IO, TRJ2IO | I/O | Timer RJ I/O pins. |
| | TRJ0IO, TRJ1IO, TRJ2IO | O | Timer RJ output pins. |
| Serial interface | CLK0, CLK2 | I/O | Transfer clock I/O pin. |
| | RXD0, RXD2 | I | Serial data input pin. |
| | TXD0, TXD2 | O | Serial data output pin. |
| | $\overline{\text{CTS2}}$ | I | Transmission control input pin. |
| | $\overline{\text{RTS2}}$ | O | Reception control output pin. |
| | SCL2 | I/O | $I^2C$ mode clock I/O pin. |
| | SDA2 | I/O | $I^2C$ mode data I/O pin. |

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.21 Pin Functions for R8C/LA8A Group (2)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| $I^2C$ bus | SCL | I/O | Clock I/O pin. |
| | SDA | I/O | Data I/O pin. |
| SSU | SSI | I/O | Data I/O pin. |
| | $\overline{SCS}$ | I/O | Chip-select signal I/O pin. |
| | SSCK | I/O | Clock I/O pin. |
| | SSO | I/O | Data I/O pin. |
| Reference voltage input | VREF | I | Reference voltage input pin for the A/D converter. |
| A/D converter | AN0 to AN11 | I | A/D converter analog input pins. |
| | $\overline{ADTRG}$ | I | AD external trigger input pin. |
| Comparator B | IVCMP1, IVCMP3 | I | Comparator B analog voltage input pins. |
| | IVREF1, IVREF3 | I | Comparator B reference voltage input pins. |
| I/O ports | P0_0 to P0_7,<br>P1_0 to P1_7,<br>P2_0 to P2_7,<br>P3_0 to P3_7,<br>P4_0 to P4_7,<br>P5_0 to P5_6,<br>P6_0 to P6_7<br>P7_0 to P7_6,<br>P8_0 to P8_7,<br>P9_0, P9_1 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>Ports P7_0, P7_1 and P8 can be used as LED drive ports. |
| Segment output | SEG0 to SEG39 | O | LCD segment output pins. |
| Common output | COM0 to COM3, COMEXP | O | LCD common output pins. |
| LCD power supply | VL1 | I | Apply the following voltage: 1 V ≤ VL1 ≤ VCC and VL1 ≤ VL2. |
| | VL2 | I | Apply the following voltage: VL2 ≤ 5.5 V and VL1 ≤ VL2 ≤ VL3. |
| | VL3 | I | Apply the following voltage: VL3 ≤ 5.5 V and VL2 ≤ VL3. |

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

**Table 4.13 SFR Information for R8C/LA8A Group (4) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 00C0h | A/D Register 0 | AD0 | XXh |
| 00C1h | | | 000000XXb |
| 00C2h | A/D Register 1 | AD1 | XXh |
| 00C3h | | | 000000XXb |
| 00C4h | A/D Register 2 | AD2 | XXh |
| 00C5h | | | 000000XXb |
| 00C6h | A/D Register 3 | AD3 | XXh |
| 00C7h | | | 000000XXb |
| 00C8h | A/D Register 4 | AD4 | XXh |
| 00C9h | | | 000000XXb |
| 00CAh | A/D Register 5 | AD5 | XXh |
| 00CBh | | | 000000XXb |
| 00CCh | A/D Register 6 | AD6 | XXh |
| 00CDh | | | 000000XXb |
| 00CEh | A/D Register 7 | AD7 | XXh |
| 00CFh | | | 000000XXb |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Mode Register | ADMOD | 00h |
| 00D5h | A/D Input Select Register | ADINSEL | 11000000b |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | A/D Control Register 2 | ADCON2 | 00h |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | Port P5 Register | P5 | XXh |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | Port P7 Register | P7 | XXh |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | Port P7 Direction Register | PD7 | 00h |
| 00F0h | Port P8 Register | P8 | XXh |
| 00F1h | Port P9 Register | P9 | XXh |
| 00F2h | Port P8 Direction Register | PD8 | 00h |
| 00F3h | Port P9 Direction Register | PD9 | 00h |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | | | |
| 00FDh | | | |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

# 5. Electrical Characteristics

## 5.1 Electrical Characteristics (R8C/LA3A Group and R8C/LA5A Group)

### 5.1.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | | Condition | Rated Value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | –0.3 to 6.5 | V |
| $V_I$ | Input voltage | XIN | XIN-XOUT oscillation on (oscillation buffer ON) (1) | –0.3 to 1.9 | V |
| | | XIN | XIN-XOUT oscillation on (oscillation buffer OFF) (1) | –0.3 to $V_{CC}$ + 0.3 | V |
| | | P5_4/VL1 | | –0.3 to VL2 (2) | V |
| | | P5_5/VL2 | | VL1 to VL3 | V |
| | | P5_6/VL3 | | VL2 to 6.5 | V |
| | | Other pins | | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | XOUT | XIN-XOUT oscillation on (oscillation buffer ON) (1) | –0.3 to 1.9 | V |
| | | XOUT | XIN-XOUT oscillation on (oscillation buffer OFF) (1) | –0.3 to $V_{CC}$ + 0.3 | V |
| | | COM0 to COM3 | | –0.3 to VL3 | V |
| | | SEG0 to SEG26 | | –0.3 to VL3 | V |
| | | Other pins | | –0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | | –40 °C ≤ $T_{opr}$ ≤ 85 °C | 500 | mW |
| $T_{opr}$ | Operating ambient temperature | | | –20 to 85 (N version)/ –40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | | –65 to 150 | °C |

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

**Table 5.7 Flash Memory (Program ROM) Characteristics**
**($V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = 0 to 60 °C, unless otherwise specified.)**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance (1) | | 10,000 (2) | – | – | times |
| – | Byte program time | | – | 80 | – | µs |
| – | Block erase time | | – | 0.12 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 0.25 + CPU clock × 3 cycles | ms |
| – | Time from suspend until erase restart | | – | – | 30 + CPU clock × 1 cycle | µs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly terminated until reading is enabled | | – | – | 30 + CPU clock × 1 cycle | µs |
| – | Program, erase voltage | | 1.8 | – | 5.5 | V |
| – | Read voltage | | 1.8 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time (6) | Ambient temperature = 85 °C | 10 | – | – | year |

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.8 Flash Memory (Data flash Block A and Block B) Characteristics ($V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance (1) | | 10,000 (2) | – | – | times |
| – | Byte program time (program/erase endurance ≤ 10,000 times) | | – | 150 | – | µs |
| – | Block erase time (program/erase endurance ≤ 10,000 times) | | – | 0.05 | 1 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 0.25 + CPU clock × 3 cycles | ms |
| – | Time from suspend until erase restart | | – | – | 30 + CPU clock × 1 cycle | µs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly terminated until reading is enabled | | – | – | 30 + CPU clock × 1 cycle | µs |
| – | Program, erase voltage | | 1.8 | – | 5.5 | V |
| – | Read voltage | | 1.8 | – | 5.5 | V |
| – | Program, erase temperature | | −20 (6) | – | 85 | °C |
| – | Data hold time (7) | Ambient temperature = 85 °C | 10 | – | – | year |

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. −40 °C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

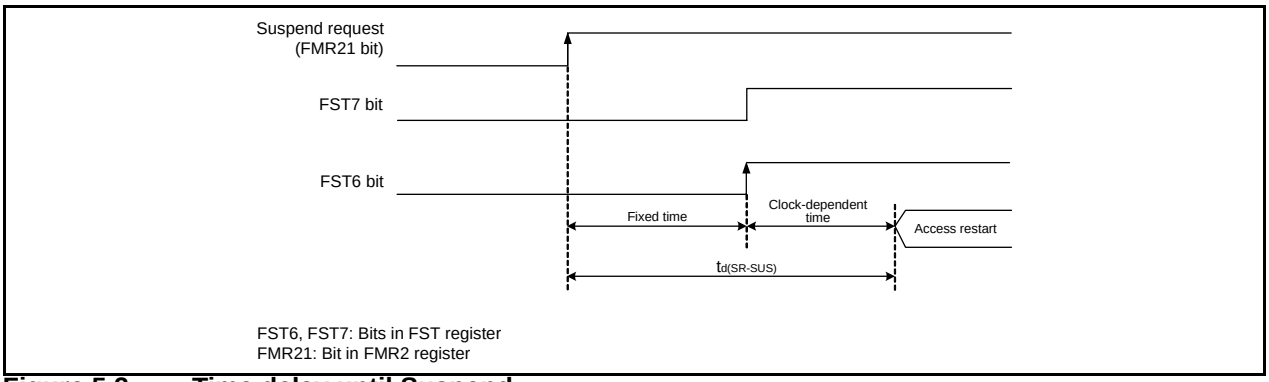



**Figure 5.2 Time delay until Suspend**

**Table 5.11 Voltage Detection 2 Circuit Characteristics**
**($V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

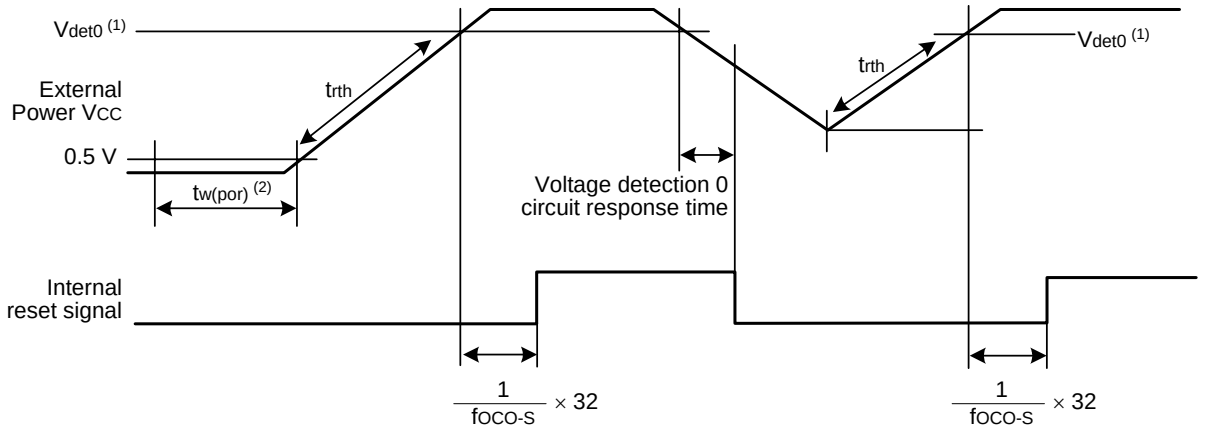
| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level Vdet2_0 (1) | At the falling of $V_{CC}$ | | 3.70 | 4.0 | 4.30 | V |
| – | Hysteresis width at the rising of Vcc in voltage detection 2 circuit | | | – | 0.10 | – | V |
| – | Voltage detection 2 circuit response time (2) | In operation | At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V | – | 20 | 150 | µs |
| | | In stop mode | At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V | – | 200 | 500 | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | | – | 1.7 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (3) | | | – | – | 100 | µs |

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.12 Power-on Reset Circuit Characteristics (1)**
**($T_{opr}$ = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{rth}$ | External power $V_{CC}$ rise gradient | | 0 | – | 50000 | mV/ms |

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.




Notes:
1. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** in the User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power $V_{CC}$ must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

**Figure 5.3 Power-on Reset Circuit Characteristics**

**Table 5.22 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]**
**(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | | Port P8 (1) | $I_{OH}$ = –2 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Other pins | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | | Port P8 (1) | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Other pins | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, $\overline{ADTRG}$, RXD0, CLK0, SSI, SCL, SDA, SSO | | | 0.05 | 0.4 | – | V |
| | | $\overline{RESET}$, $\overline{WKUP0}$ | | | 0.1 | 0.8 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 1.8 V, $V_{CC}$ = 1.8 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 1.8 V | | – | – | –4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 1.8 V | | 85 | 220 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 2.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 14 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.42 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | High-speed on-chip oscillator frequency after reset | VCC = 1.8 V to 5.5 V<br>– 20°C ≤ Topr ≤ 85°C | 19.2 | 20 | 20.8 | MHz |
| | | VCC = 1.8 V to 5.5 V<br>– 40°C ≤ Topr ≤ 85°C | 19.0 | 20 | 21.0 | MHz |
| | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1) | VCC = 1.8 V to 5.5 V<br>– 20°C ≤ Topr ≤ 85°C | 17.694 | 18.432 | 19.169 | MHz |
| | | VCC = 1.8 V to 5.5 V<br>– 40°C ≤ Topr ≤ 85°C | 17.510 | 18.432 | 19.353 | MHz |
| – | Oscillation stability time | | – | 5 | 30 | µs |
| – | Self power consumption at oscillation | VCC = 5.0 V, Topr = 25°C | – | 530 | – | µA |

Note:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 60 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | – | 35 | µs |
| – | Self power consumption at oscillation | VCC = 5.0 V, Topr = 25°C | – | 2 | – | µA |
| fOCO-WDT | Low-speed on-chip oscillator frequency for the watchdog timer | | 60 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | – | 35 | µs |
| – | Self power consumption at oscillation | VCC = 5.0 V, Topr = 25°C | – | 2 | – | µA |

**Table 5.44 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| td(P-R) | Time for internal power supply stabilization during power-on (1) | | – | – | 2000 | µs |

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

**Table 5.48 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]**
**(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | | | | | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Oscillation Circuit | | On-Chip Oscillator | | CPU Clock | Low-Power-Consumption Setting | Other | Min. | Typ. (3) | Max. | |
| | | | XIN (2) | XCIN | High-Speed | Low-Speed | | | | | | | |
| Icc | Power supply current (1) | High-speed clock mode | 20 MHz | Off | Off | 125 kHz | No division | – | | – | 4.7 | 10 | mA |
| | | | 16 MHz | Off | Off | 125 kHz | No division | – | | – | 3.9 | 8 | mA |
| | | | 10 MHz | Off | Off | 125 kHz | No division | – | | – | 2.3 | – | mA |
| | | | 20 MHz | Off | Off | Off | No division | FMR27 = 1<br>MSTCR0 = BEh<br>MSTCR1 = 3Fh | Flash memory off<br>Program operation on RAM<br>Module standby setting enabled | – | 3.1 | – | mA |
| | | | 20 MHz | Off | Off | 125 kHz | Divide-by-8 | – | | – | 1.8 | – | mA |
| | | | 16 MHz | Off | Off | 125 kHz | Divide-by-8 | – | | – | 1.5 | – | mA |
| | | | 10 MHz | Off | Off | 125 kHz | Divide-by-8 | – | | – | 1.0 | – | mA |
| | | High-speed on-chip oscillator mode | Off | Off | 20 MHz | 125 kHz | No division | – | | – | 5.0 | 11 | mA |
| | | | Off | Off | 20 MHz | 125 kHz | Divide-by-8 | – | | – | 2.1 | – | mA |
| | | | Off | Off | 4 MHz | 125 kHz | Divide-by-16 | MSTCR0 = BEh<br>MSTCR1 = 3Fh | | – | 0.9 | – | mA |
| | | Low-speed on-chip oscillator mode | Off | Off | Off | 125 kHz | No division | FMR27 = 1<br>VCA20 = 0 | | – | 110 | 320 | µA |
| | | | Off | Off | Off | 125 kHz | Divide-by-8 | FMR27 = 1<br>VCA20 = 0 | | – | 63 | 220 | µA |
| | | Low-speed clock mode | Off | 32 kHz | Off | Off | No division | FMR27 = 1<br>VCA20 = 0 | | – | 60 | 220 | µA |
| | | | Off | 32 kHz | Off | Off | No division | FMSTP = 1<br>VCA20 = 0 | Flash memory off<br>Program operation on RAM | – | 46 | – | µA |
| | | Wait mode | Off | Off | Off | 125 kHz | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1 | While a WAIT instruction is executed<br>Peripheral clock operation | – | 9.0 | 50 | µA |
| | | | Off | Off | Off | 125 kHz | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off | – | 2.8 | 33 | µA |
| | | | Off | 32 kHz | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode<br>LCD drive control circuit (4)<br>When external division resistors are used | – | 4.6 | – | µA |
| | | | Off | 32 kHz | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | – | 2.4 | – | µA |
| | | Stop mode | Off | Off | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 25°C<br>Peripheral clock off | – | 0.5 | 2.2 | µA |
| | | | Off | Off | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 85°C<br>Peripheral clock off | – | 1.2 | – | µA |
| | | Power-off mode | Off | Off | Off | Off | – | – | Power-off 0<br>Topr = 25°C | – | 0.01 | 0.1 | µA |
| | | | Off | Off | Off | Off | – | – | Power-off 0<br>Topr = 85°C | – | 0.03 | – | µA |
| | | | Off | 32 kHz | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>Topr = 25°C | – | 1.8 | 6.4 | µA |
| | | | Off | 32 kHz | Off | Off | – | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>Topr = 85°C | – | 2.7 | – | µA |

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

**Table 5.49 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]**
**(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | | Port P7_0, P7_1, P8 (1) | $I_{OH}$ = –5 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Other pins | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | | Port P7_0, P7_1, P8 (1) | $I_{OL}$ = 5 mA | – | – | 0.5 | V |
| | | | Other pins | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO | | | 0.05 | 0.4 | – | V |
| | | $\overline{RESET}$, $\overline{WKUP0}$ | | | 0.1 | 0.8 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 3 V, $V_{CC}$ = 3 V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 3 V | | – | – | –5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 3 V | | 25 | 80 | 140 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 2.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 14 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.51 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]**
**(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | | Port P7_0, P7_1, P8 (1) | $I_{OH}$ = –2 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Other pins | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | | Port P7_0, P7_1, P8 (1) | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Other pins | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO | | | 0.05 | 0.4 | – | V |
| | | $\overline{RESET}$, $\overline{WKUP0}$ | | | 0.1 | 0.8 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 1.8 V, $V_{CC}$ = 1.8 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 1.8 V | | – | – | –4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 1.8 V | | 85 | 220 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 2.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 14 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.