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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	56
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la66anfp-30

Email: info@E-XFL.COM

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#### 1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information. The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group	
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins	
	High current drive ports	8 pins	8 pins	8 pins	10 pins	
Interrupts	INT interrupt pins	5 pins	6 pins	8 pins	8 pins	
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin	
	Timer RJ1 output pin	None	None	None	1 pin	
	Timer RJ2 I/O pin	None	None	None	1 pin	
	Timer RJ2 output pin	None	None	None	1 pin	
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin	
Serial interface	UART2	None	None	1 pin	1 pin	
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins	
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins	
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins	
	Reference input voltage	1 pin	2 pins	2 pins	2 pins	
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin	
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin	
Packages	·	32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP	

#### Table 1.1 Differences between Groups

Note:

1. I/O ports are shared with I/O functions, such as interrupts or timers.

Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.



### 1.1.3 Specifications

Tables 1.6 to 1.8 list the specifications.

Table 1.6	Specifications	(1)
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Item	Function		Specification
CPU			R8C CPU core
CPU	Central processing unit		
			Number of fundamental instructions: 89
			Minimum instruction execution time:
			50 ns (f(XIN) = 20 MHz, VCC = $2.7 \text{ V to } 5.5 \text{ V}$ )
			125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V)
			• Multiplier: 16 bits $\times$ 16 bits $\rightarrow$ 32 bits
			• Multiply-accumulate instruction: 16 bits $\times$ 16 bits + 32 bits $\rightarrow$ 32 bits
			Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM		Refer to Tables 1.9 to 1.12 Product Lists.
	Data flash		
Power	Voltage detection	on circuit	Power-on reset
Supply			<ul> <li>Voltage detection 3 (detection level of voltage detection 0 and</li> </ul>
Voltage			voltage detection 1 selectable)
Detection			
I/O Ports	Programmable	R8C/LA3A Group	CMOS I/O ports: 26, selectable pull-up resistor <sup>(1)</sup>
	I/O ports		High current drive ports: 8
		R8C/LA5A Group	
		•	• High current drive ports: 8
		R8C/LA6A Group	
		1100/2/10/101000	High current drive ports: 8
		R8C/LA8A Group	
		ROC/LAOA Gloup	
			High current drive ports: 10
Clock	Clock generation	on circuits	4 circuits: XIN clock oscillation circuit
			XCIN clock oscillation circuit (32 kHz)
			High-speed on-chip oscillator (with frequency adjustment function)
			Low-speed on-chip oscillator
			Oscillation stop detection:
			XIN clock oscillation stop detection function
			Frequency divider circuit:
			Division ratio selectable from 1, 2, 4, 8, and 16
			<ul> <li>Low-power-consumption modes:</li> </ul>
			Standard operating mode (high-speed clock, low-speed clock, high-
			speed on-chip oscillator, low-speed on-chip oscillator), wait mode,
			stop mode, power-off mode
			Real-time clock (timer RH)
Interrupts		R8C/LA3A Group	Number of interrupt vectors: 69
			<ul> <li>External Interrupt: 13 (INT × 5, key input × 8)</li> </ul>
			Priority levels: 7 levels
		R8C/LA5A Group	Number of interrupt vectors: 69
			• External Interrupt: 14 (INT × 6, key input × 8)
			Priority levels: 7 levels
R8C/LA6A Group R8C/LA8A Group		R8C/LA6A Group	Number of interrupt vectors: 69
		R8C/LA8A Group	
	Roorenon Gloup		Priority levels: 7 levels
Watchdog	Timer	1	• 14 bits × 1 (with prescaler)
			Selectable reset start function
			Selectable low-speed on-chip oscillator for watchdog timer
			conclusion of speed of one oscillator for watchdog times

Note:

1. No pull-up resistor is provided in the pins P5\_4 to P5\_6.



1.	Overview

<b>D</b>	Internal RC	M Capacity	Internal RAM		
Part No.	Program ROM	• •	Capacity	Package Type	Remarks
R5F2LA64ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	N Version
R5F2LA64ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	-
R5F2LA66ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	-
R5F2LA66ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AANFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AANFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA6CANFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6CANFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA64ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	D Version
R5F2LA64ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AADFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AADFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	1
R5F2LA6CADFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	1
R5F2LA6CADFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	1

#### Table 1.11 Product List for R8C/LA6A Group

#### Current of Oct 2011

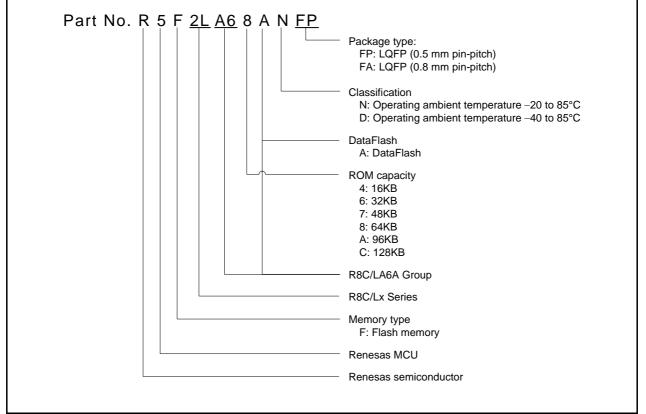


Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group

#### 1.4 Pin Assignments

Figures 1.9 to 1.12 show pin assignments (top view). Tables 1.13 to 1.17 list the pin name information by pin number.

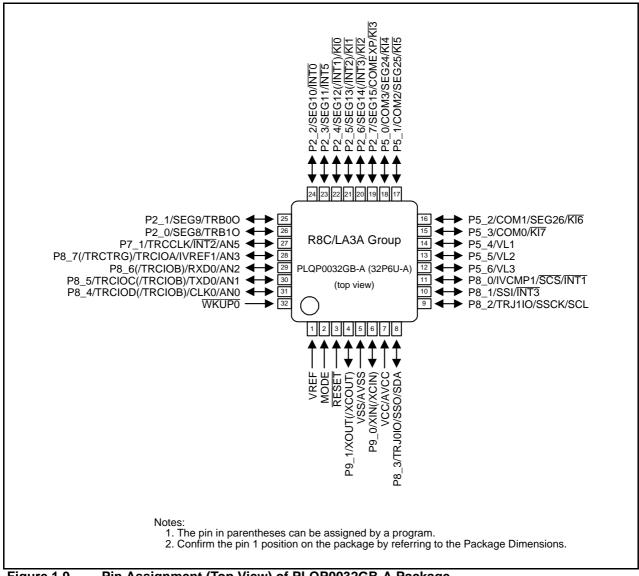


Figure 1.9 Pin Assignment (Top View) of PLQP0032GB-A Package



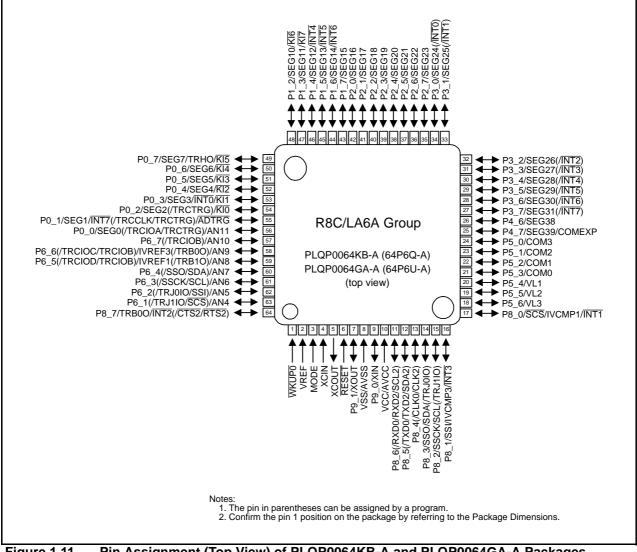


Figure 1.11 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages



Pin N	umber			I/O Pin Functions for Peripheral Modules						
LA8A	LA6A	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	I <sup>2</sup> C bus	A/D Converter, Comparator B	LCD drive Control Circuit
1			P7_1		TRJ10	(TXD2/SDA2/RXD2/ SCL2)				
2		WKUP1	P7_0		TRJ2O	(CLK2)				
3	64		P8_7	INT2	TRB0O	(CTS2/RTS2)				
4	1	WKUP0								
5	2	VREF								
6	3	MODE								
7	4	XCIN								
8	5	XCOUT								
9	6	RESET								
10	7	XOUT	P9_1							
11	8	VSS/ AVSS								
12	9	XIN	P9_0							
13	10	VCC/ AVCC								
14	11		P8_6			(RXD0/RXD2/SCL2)				
15	12		P8_5			(TXD0/TXD2/SDA2)				
16	13		P8_4			(CLK0/CLK2)				
17	14		P8_3		(TRJ0IO)		SSO	SDA		
18	15		P8_2		(TRJ1IO)		SSCK	SCL		
19	16		P8_1	INT3			SSI		IVCMP3	
20	17		P8_0	INT1			SCS		IVCMP1	
21	18		P5_6							VL3
22	19		P5_5							VL2
23	20		P5_4							VL1
24	21		P5_3							COM0
25	22		P5_2							COM1
26	23		P5_1							COM2
27	24		P5_0							COM3
28	25		P4_7							SEG39/ COMEXP
29	26		P4_6							SEG38
30			P4_5							SEG37

Table 1.15	Pin Name Information by Pin Number	(R8C/LA6A Group, R8C/LA8A Group)(1)
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Note:

1. The pin in parentheses can be assigned by a program.



Item	Pin Name	I/O Type	Description
I <sup>2</sup> C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
SSU	SSI	I/O	Data I/O pin.
	SCS	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN0 to AN6	I	A/D converter analog input pins.
	ADTRG	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O ports	P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_6, P7_0 to P7_2, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Port P8 can be used as LED drive ports.
Segment output	SEG0 to SEG26	0	LCD segment output pins.
Common output	COM0 to COM3, COMEXP	0	LCD common output pins.
LCD power supply	VL1	I	Apply the following voltage: $1 \text{ V} \leq \text{VL1} \leq \text{VCC}$ and $\text{VL1} \leq \text{VL2}$ .
	VL2	I	Apply the following voltage: VL2 $\leq$ 5.5 V and VL1 $\leq$ VL2 $\leq$ VL3.
	VL3	I	Apply the following voltage: VL3 $\leq$ 5.5 V and VL2 $\leq$ VL3.

Table 1.19	Pin Functions for R8C/LA5A Group (2)
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I: Input O: Output I/O: Input and output Note:

1. Contact the oscillator manufacturer for oscillation characteristics.



Item	Pin Name	I/О Туре	Description	
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.	
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.	
Reset input	RESET	I	Driving this pin low resets the MCU.	
MODE	MODE	I	Connect this pin to VCC via a resistor.	
Power-off 0 mode exit input	WKUP0	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.	
	WKUP1	I	This pin is provided for input to exit the mode used in power-off 0 mode.	
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins	
XIN clock output	clock output XOUT O XIN a pin ar used,		XIN and XOUT. <sup>(1)</sup> To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. <sup>(1)</sup>	
XCIN clock output	XCOUT	0	To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.	
INT interrupt input	INT0 to INT7	I	INT interrupt input pins.	
Key input interrupt	KI0 to KI7	I	Key input interrupt input pins.	
Timer RB	TRB0O, TRB1O	0	Timer RB output pins.	
Timer RC	TRCCLK	I	External clock input pin.	
	TRCTRG	I	External trigger input pin.	
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.	
Timer RH	TRHO	0	Timer RH output pin.	
Timer RJ	TRJ0IO, TRJ1IO, TRJ2IO	I/O	Timer RJ I/O pins.	
	TRJ0IO, TRJ1IO, TRJ2IO	0	Timer RJ output pins.	
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pin.	
	RXD0, RXD2	I	Serial data input pin.	
	TXD0, TXD2	0	Serial data output pin.	
	CTS2	Ι	Transmission control input pin.	
	RTS2	0	Reception control output pin.	
	SCL2	I/O	I <sup>2</sup> C mode clock I/O pin.	
	SDA2	I/O	I <sup>2</sup> C mode data I/O pin.	

Table 1.20	Pin Functions for R8C/LA8A Group (1)
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I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.



Item	Pin Name	I/O Type	Description
I <sup>2</sup> C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
SSU	SSI	I/O	Data I/O pin.
	SCS	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN0 to AN11	I	A/D converter analog input pins.
	ADTRG	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_6, P6_0 to P6_7 P7_0 to P7_6, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P7_0, P7_1 and P8 can be used as LED drive ports.
Segment output	SEG0 to SEG39	0	LCD segment output pins.
Common output	COM0 to COM3, COMEXP	0	LCD common output pins.
LCD power supply	VL1	I	Apply the following voltage: 1 V $\leq$ VL1 $\leq$ VCC and VL1 $\leq$ VL2.
	VL2	I	Apply the following voltage: VL2 $\leq$ 5.5 V and VL1 $\leq$ VL2 $\leq$ VL3.
	VL3	I	Apply the following voltage: VL3 $\leq$ 5.5 V and VL2 $\leq$ VL3.

Table 1.21	Pin Functions for R8C/LA8A Group (2)
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I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.



#### 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

#### 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

#### 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

#### 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

#### 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

#### 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

#### 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

#### 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

#### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

#### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

#### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

#### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

#### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



00000         ADP         Number of the second secon	Address	Register	Symbol	After Reset
00Ch         MCA         ADI         000000Xb           00CA         AD Register 1         ADI         00000Xb           00CA         AD Register 2         AD2         00000Xb           00CB         AD Register 3         AD3         00000Xb           00CB         AD Register 4         AD3         00000Xb           00CB         AD Register 5         AD4         000000Xb           00CB         AD Register 5         AD5         XXh           00CCh         AD Register 7         AD5         XXh           00CCh         AD Register 7         AD7         XXh           00CCh         AD Register 7         AD7         XXh           00CCh         AD Register 7         AD7         XXh           00Ch         AD Register 7         AD7         XXh           00Ch         AD Register 7         AD7         XXh           00Ch         AD Register 1         AD7				
000C3h         AD R Register 1         AD 1         XXh           000C3h         AD Register 2         AD 2         XXh           000C3h         AD Register 3         AD 3         XXh           000C3h         AD Register 3         AD 3         XXh           000000XXb         000000XXb         000000XXb         000000XXb           000C8h         AD Register 4         AD 4         XXh           000C8h         AD Register 5         AD 5         XXh           000C8h         AD Register 5         AD 5         XXh           000000XXb         000000XXb         000000XXb         000000XXb           00C7h         AD Register 7         AD 7         XXh           000000Xb         000000Xb         000000Xb         000000Xb           0007h         AD Register 7         AD 7         XXh           0007h         AD Socier Register         AD NOD         000h           0007h         AD Control Register 1         ADNOD         00h           0007h         AD Control Register 1         ADCON         00h           0007h         AD Control Register 1         ADCON         00h           0007h         AD Control Register 2         ADCON         00h			ADU	
00C3h         AD Pagister 2         000000000000000000000000000000000000		A/D Pagistar 1	AD1	
00C4h         AD         RXh         D00000XXb           00C6h         AD         Register 2         AD3         XXh           00C6h         AD         Register 3         AD3         XXh           00C6h         AD         Register 4         AD4         XXh           00C6h         AD         Register 5         AD5         XXh           00C6A         AD         Register 5         AD6         XXh           00C6Ch         AD         Register 7         AD7         XXh           00C6Ch         AD         Register 7         AD7         XXh           00C6Ch         AD         Register 7         AD7         XNh           00C7h         AD         Control Register 7         AD7         XNh           00C7h         AD         Control Reg			ADT	
00C5HAD Register 3AD3 002000Xb00C5HAD Register 4AD4 00000Xb00C5HAD Register 4AD4 00000Xb00C5HAD Register 5AD5 00000Xb00C6HAD Register 6AD6 00000Xb00C6HAD Register 7AD7 00000Xb00C6HAD Register 7AD7 00000Xb00C7HAD Register 7AD7 00000Xb00C6HAD Register 7AD7 00000Xb00C7HAD Register 7AD7 00000Xb00C7HAD Register 7AD7 00000Xb00D4HAD Register 7AD7 00000Xb00D4HAD Input Select RegisterADINSEL00D4HAD Control Register 1ADCON100D4HAD Control Register 1ADCON100D4HAD Control Register 1ADCON100D4HAD Control Register 1ADCON200D4HAD Control Register 1ADCON200D5HAD Control Register 2ADCON200D6HAD Control Register 2ADCON200D7HAD Control Register 2ADCON200D7HAD Control Register 2ADC00D7HAD Control Register 2ADC00D7HPOT PD Register 2ADA00D7HPOT PD Register 3PO100D7HPOT PD Register 4PO100D7HPOT PD Registe		A/D Devictor 0	4.52	
000Cbh         AD Register 3         AD3         XXh           000Cbh         AD Register 4         AD4         XXh           000Cbh         AD Register 5         AD5         XXh           000Cbh         AD Register 5         AD5         XXh           000Cbh         AD Register 6         AD6         XXh           000Cbh         AD Register 7         AD7         XXh           000Cbh         AD Register 7         00000XXb         00000XXb           000Dh         -         -         -           000Dh         -         -         -           000Dh         -         -         -           000Dh         AD Control Register 0         ADCON0         00h           00DDh         AD Control Register 1         ADCON1         00h           00DDh         AD Control Register 2         ADCON2         00h           00DDh         AD Control Register 2         ADCON2         00h           00DDh <td< td=""><td></td><td>A/D Register 2</td><td>AD2</td><td></td></td<>		A/D Register 2	AD2	
00CPh         AD Register 4         AD A         XNh           00CSh         A/D Register 5         AD S         XNh           00CSh         A/D Register 5         AD S         XNh           00CCh         A/D Register 6         AD S         XNh           00CCh         A/D Register 7         AD Xh         XNh           00CCh         A/D Register 7         XNh         XNh           00CDh         AD Register 7         XNh         XNh           00DDh         P         P         XNh           00DDh         P         P         P           00DDh         P         P         P           00DDh         P         P         P           00DDh         P         P         P           00DDh         AD Mode Register         ADMOD         Onh           00DDh         AD Control Register 1         ADCONI         Onh           00DDh         AD Control Register 1         ADCONI         Onh           00DDh         AD Control Register 2         ADCONI         Onh           00DDh         AD Control Register 2         ADCONI         Onh           00DDh         AD Control Register         PO         XNh <td></td> <td></td> <td></td> <td></td>				
00C6h         ADA         XAh         000000000000000000000000000000000000		A/D Register 3	AD3	
0000h         000000000000000000000000000000000000				
00CAh         ADF Register 5         ADF         XAh           00CCh         ADP Register 6         000000XXb         000000XXb           00CCh         ADP Register 6         0000000Xxb           00CCh         ADP Register 7         ADP           00CCh         ADP Register 7         000000000000000000000000000000000000		A/D Register 4	AD4	XXh
00000h         000000000000000000000000000000000000				
00CCh         A/D Register 6         AD6         XXh           00CDn         AD7         XXh         00000XXb           00CDn         AD7         XXh         00000XXb           00Dn         AD7         XXh         00000XXb           00Dn         AD7         XXh         00000XXb           00Dn         AD         AD7         XXh           00Dn         AD         AD8         AD8           00Dn         AD         AD8         AD8000         AD8           00Dn         AD Input Select Register         AD100000         AD6         AD8           00Dn         AD7 Control Register 1         AD6CON1         OD1         AD7           00Dn         AD7 Control Register 1         AD7         AD7         AD7           00Dn         AD7         AD7         AD7         AD7         AD7		A/D Register 5	AD5	XXh
00CDN         AD7         XXh           00CEN         AD7         XXh           00CEN         AD7         XXh           00D0h         Image: Constraint of the second s				
OCCEN         AD7         XXh           000CPh         000000Xb           00D1h         000000Xb           00D2h         000000Xb           00D2h         000000Xb           00D3h         000000Xb           00D3h         000000Xb           00D3h         AD Mode Register           00D3h         AD Control Register           00D5h         AD Control Register 0           00D5h         AD Control Register 1           00D5h         AD Control Register 2           00D5h         AD Control Register 3           00D5h         Port PO Register           00D5h         Port PD Register           00D5h         Port PD Register           00D5h         Port PD Register           00D5h         Port PD Register           00D5h		A/D Register 6	AD6	XXh
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0000h	00CEh	A/D Register 7	AD7	XXh
0001h	00CFh			000000XXb
00D2h         methods         methods           00D3h         AD Input Select Register         ADINSEL         11000000b           00D5h         AD Input Select Register         ADINSEL         11000000b           00D5h         AD Control Register 1         ADCON0         Ooh           00D5h         AD Control Register 1         ADCON1         Ooh           00D3h         AD Control Register 1         ADCON1         Ooh           00D3h         AD Control Register 1         ADCON2         Ooh           00D3h         AD Control Register 2         ADCON2         Ooh           00D5h         AD Fort PO Register         P1         XXh           00E5h         Port P3 Register         P2         Xh           00E5h         Port P3 Register         P3	00D0h			
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0006h         ADC Control Register 0         ADC ON         00h           0007h         ADC Control Register 1         ADC ON         00h           0005h				
00D7h         A/D Control Register 1         ADC ON1         00h           00D8h         -				
0008h				
0009h			ADCONT	
00DAh				
000Bh         Image: second secon				
00DCh         ADC Ontrol Register 2         ADC ON2         00h           00DEh         ADCON2         00h            00DFh         Port P0 Register         P0         XXh           00E0h         Port P1 Register         P1         XXh           00E2h         Port P0 Direction Register         P1         XXh           00E3h         Port P1 Direction Register         PD1         00h           00E4h         Port P2 Register         P2         XXh           00E5h         Port P2 Register         P2         00h           00E3h         Port P2 Register         P2         00h           00E5h         Port P3 Register         PD2         00h           00E6h         Port P3 Direction Register         PD2         00h           00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P5         XXh           00E6h         Port P5 Register         P5         00h           00E6h         Port P6 Register         PD5         00h           00E6h         Port P6 Register         P06         0Xh           00E6h         Port P6 Register         P06         0Xh				
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00F4h				
00F5h             00F6h             00F7h             00F8h             00F9h             00F8h             00F9h             00F9h             00F8h             00F8h             00FBh             00FBh             00FCh             00FEh		Port P9 Direction Register	PD9	00h
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00F7h            00F8h            00F9h            00F9h            00FAh            00FBh            00FBh            00FCh            00FDh            00FEh	00F6h			
00F8h	00F7h			
00F9h				
00FAh				
00FBh				
00FCh 00FDh 00FEh				
00FDh 00FEh 00FEh				
00FEh				
X: Undefined				

 Table 4.13
 SFR Information for R8C/LA8A Group (4) <sup>(1)</sup>

X: Unde Note:

1. Blank spaces are reserved. No access is allowed.



### 5. Electrical Characteristics

### 5.1 Electrical Characteristics (R8C/LA3A Group and R8C/LA5A Group)

#### 5.1.1 Absolute Maximum Ratings

#### Table 5.1 Absolute Maximum Ratings

Symbol		Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage			-0.3 to 6.5	V
VI	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>	-0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup>	-0.3 to Vcc + 0.3	V
		P5_4/VL1		-0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		-0.3 to Vcc + 0.3	V
Vo	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>	-0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup>	-0.3 to Vcc + 0.3	V
		COM0 to COM3		-0.3 to VL3	V
		SEG0 to SEG26		-0.3 to VL3	V
		Other pins		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	on	$-40 \ ^{\circ}C \le T_{opr} \le 85 \ ^{\circ}C$	500	mW
Topr	Operating ambi	ent temperature		-20 to 85 (N version)/ -40 to 85 (D version)	°C
Tstg	Storage temper	ature		-65 to 150	°C

Notes:

1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.

2. The VL1 voltage should be VCC or below.



Symbol	Parameter	Conditions		Sta	ndard	1.1
			Min.	Тур.	Max.	Unit
-	Program/erase endurance (1)		10,000 (2)	-	-	times
_	Byte program time		-	80	-	μS
-	Block erase time		-	0.12	-	S
td(SR-SUS)	Time delay from suspend request until suspend		-	_	0.25 + CPU clock × 3 cycles	ms
-	Time from suspend until erase restart		-	-	30 + CPU clock × 1 cycle	μS
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30 + CPU clock × 1 cycle	μS
-	Program, erase voltage		1.8	-	5.5	V
-	Read voltage		1.8	-	5.5	V
-	Program, erase temperature		0	-	60	°C
_	Data hold time <sup>(6)</sup>	Ambient temperature = 85 °C	10	-	-	year

# Table 5.7Flash Memory (Program ROM) Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = 0 to 60 °C, unless otherwise specified.)

Notes:

1. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

- 3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

6. The data hold time includes time that the power supply is off or the clock is not supplied.



# Table 5.8Flash Memory (Data flash Block A and Block B) Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless<br/>otherwise specified.)

Symbol	Parameter	Conditiono		Linit		
Symbol	Parameter	Conditions	Min.	Min. Typ. Max.		Unit
-	Program/erase endurance (1)		10,000 (2)	-	-	time s
-	Byte program time (program/erase endurance ≤ 10,000 times)		-	150	-	μS
-	Block erase time (program/erase endurance ≤ 10,000 times)		-	0.05	1	S
td(SR-SUS)	Time delay from suspend request until suspend		-	-	0.25 + CPU clock × 3 cycles	ms
-	Time from suspend until erase restart		-	-	30 + CPU clock × 1 cycle	μS
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30 + CPU clock × 1 cycle	μS
-	Program, erase voltage		1.8	-	5.5	V
-	Read voltage		1.8	-	5.5	V
-	Program, erase temperature		-20 (6)	-	85	°C
-	Data hold time <sup>(7)</sup>	Ambient temperature = 85 °C	10	-	_	year

Notes:

1. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

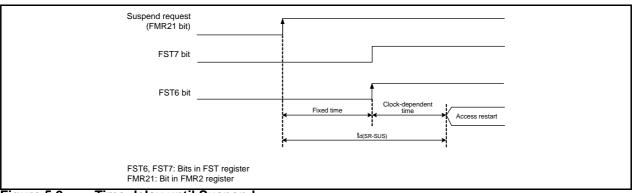
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

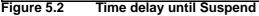
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

6. -40 °C for D version.

7. The data hold time includes time that the power supply is off or the clock is not supplied.







# Table 5.11Voltage Detection 2 Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless<br/>otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
Symbol	Falameter		Condition	Min.	Тур.	Max.	Unit
Vdet2	Voltage detection level Vdet2_0 <sup>(1)</sup>	At the falling c	of Vcc	3.70	4.0	4.30	V
-	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			-	0.10	-	V
-	Voltage detection 2 circuit response time <sup>(2)</sup>	In operation	At the falling of Vcc from $5 \text{ V to } (\text{Vdet2}_0 - 0.1) \text{ V}$	-	20	150	μs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 - 0.1) V	-	200	500	μs
-	Voltage detection circuit self power consumption	VCA27 = 1, V	cc = 5.0 V	-	1.7	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>			Ι	-	100	μS

Notes:

1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.

2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.

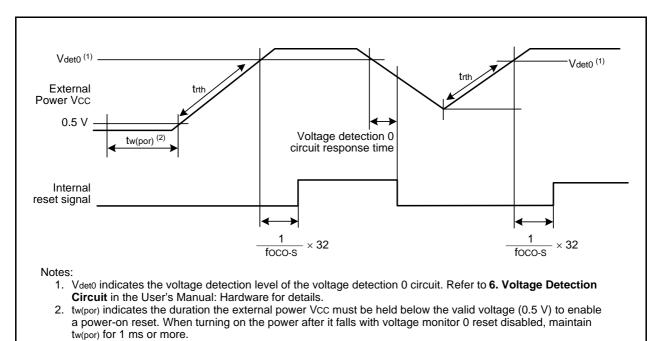
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

# Table 5.12Power-on Reset Circuit Characteristics (1)<br/>(Topr = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Unit		
	Faidinetei	Condition	Min.	Тур.	Max.	Offic
trth	External power Vcc rise gradient		0	-	50000	mV/ms

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



#### Figure 5.3 Power-on Reset Circuit Characteristics



## Table 5.22DC Characteristics (5) [1.8 V $\leq$ Vcc < 2.7 V]<br/>(Topr = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Sumbol	Dere	matar	Condition		Sta	andard		Unit
Symbol	Para	meter	Condition		Min.	Тур.	Max.	•••••
Vон	Output "H" voltage		Port P8 <sup>(1)</sup>	Iон = -2 mA	Vcc - 0.5	-	Vcc	V
			Other pins	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		Port P8 <sup>(1)</sup>	IoL = 2 mA	-	-	0.5	V
			Other pins	lo∟ = 1 mA	-	-	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2,           INT3, INT5, INT7,           KI0, KI1, KI2, KI3,           KI4, KI5, KI6, KI7,           TRCIOA, TRCIOB,           TRCIOC, TRCIOD,           TRJ0IO, TRJ1IO,           TRCTRG, TRCCLK,           ADTRG,           RXD0, CLK0, SSI,           SCL, SDA, SSO           RESET, WKUP0			0.05	0.4	_	V
Ін	Input "H" current	,	VI = 1.8 V, Vcc = 1.8 V		-	-	4.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 1.8 V		-	-	-4.0	μΑ
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 1.8 V		85	220	500	kΩ
RfXIN	Feedback resistance	XIN			-	2.0	-	MΩ
RfXCIN	Feedback resistance	XCIN			-	14	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	-	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.



# Table 5.42High-speed On-Chip Oscillator Circuit Characteristics<br/>(Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless<br/>otherwise specified.)

Symbol	Parameter	Condition		Unit		
Symbol	Falameter	Condition	Min.	Тур.	Max.	Unit
-	High-speed on-chip oscillator frequency after reset	$\label{eq:Vcc} \begin{array}{l} Vcc = 1.8 \ V \ to \ 5.5 \ V \\ - \ 20^{\circ}C \leq T_{opr} \leq 85^{\circ}C \end{array}$	19.2	20	20.8	MHz
		$\label{eq:VC} \begin{array}{l} Vcc = 1.8 \; V \; \text{to} \; 5.5 \; V \\ - \; 40^\circ C \leq Topr \leq 85^\circ C \end{array}$	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into	Vcc = 1.8 V to 5.5 V - 20°C ≤ Topr ≤ 85°C	17.694	18.432	19.169	MHz
	the FRA1 register and the FRA5 register correction value into the FRA3 register <sup>(1)</sup>	$\label{eq:VC} \begin{array}{l} \mbox{Vcc} = 1.8 \mbox{ V to } 5.5 \mbox{ V} \\ \mbox{-} 40^{\circ}\mbox{C} \leq \mbox{Topr} \leq 85^{\circ}\mbox{C} \end{array}$	17.510	18.432	19.353	MHz
-	Oscillation stability time		-	5	30	μS
-	Self power consumption at oscillation	$VCC = 5.0 V$ , $Topr = 25^{\circ}C$	-	530	-	μΑ

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

#### Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics

## (Vcc = 1.8 to 5.5 V and Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Unit		
Symbol	Falanielei	Condition	Min.	Тур.	Max.	Unit
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
-	Oscillation stability time		-	-	35	μS
-	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	2	-	μΑ
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
-	Oscillation stability time		-	-	35	μS
-	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	2	-	μΑ

### Table 5.44 Power Supply Circuit Characteristics

#### (Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	:	Standard	4	Unit
Symbol	Falanielei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on <sup>(1)</sup>		-	-	2000	μS
	power-on (1)					

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.



				. ,		•			•			,	
							Condition			S	tanda	rd	
Symbol	Parameter		Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power- Consumption	Other			Max	Uni
			XIN (2)	XCIN	High- Speed	Low- Speed		Setting	0.1101		(3)		
CC	Power	High-	20 MHz	Off	Off	125 kHz	No division	-		-	4.7	10	m/
	supply current <sup>(1)</sup>	speed clock	16 MHz	Off	Off	125 kHz	No division	-		-	3.9	8	m/
	ourront	mode	10 MHz	Off	Off	125 kHz	No division	-		-	2.3	-	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	-	3.1	-	m/
			20 MHz	Off	Off	125 kHz	Divide-by-8	-		-	1.8	-	m/
			16 MHz	Off	Off	125 kHz	Divide-by-8	-		-	1.5	-	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	-		-	1.0	I	m/
		High-	Off	Off	20 MHz	125 kHz	No division	-		-	5.0	11	m/
		speed	Off	Off	20 MHz	125 kHz	Divide-by-8	-		-	2.1	I	m/
		on-chip oscillator mode	Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		-	0.9	-	m/
		Low- speed	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		-	110	320	μA
		on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		-	63	220	μA
		Low- speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		-	60	220	μΑ
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	-	46	-	μΑ
		Wait mode	Off	Off	Off	125 kHz	-	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	-	9.0	50	μΑ
			Off	Off	Off	125 kHz	-	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		2.8	33	μΑ
			Off	32 kHz	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT LCD drive instruction is executed circuit <sup>(4)</sup> Peripheral When clock off external Timer RH division operation in real-time used clock mode	-	4.6	-	μΑ
			Off	32 kHz	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real- time clock mode	-	2.4	1	μA
		Stop mode	Off	Off	Off	Off	_	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	-	0.5	2.2	μA
			Off	Off	Off	Off	-	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	-	1.2	-	μA
		Power- off mode		Off	Off	Off	-	-	Power-off 0 Topr = 25°C	-	0.01	0.1	μA
			Off	Off	Off	Off	-	-	Power-off 0 Topr = 85°C	-	0.03	-	μA
			Off	32 kHz	Off	Off	-	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	-	1.8	6.4	μA
			Off	32 kHz	Off	Off	-	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	-	2.7	I	μA

#### **Table 5.48** DC Characteristics (2) [4.0 V $\leq$ Vcc $\leq$ 5.5 V] (Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Notes:

1. 2. 3. 4.

Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss. XIN is set to square wave input. Vcc = 5.0 V VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.49	DC Characteristics (3) [2.7 V $\leq$ Vcc $<$ 4.0 V]
	(Topr = $-20$ to 85°C (N version)/ $-40$ to 85°C (D version), unless otherwise specified.)

Symbol	Doro	meter	Condition	St	Unit			
Symbol	Fdia	meter	Condition	Min.	Тур.	Max.	Unit	
Vон	Output "H" voltage		Port P7_0, P7_1, P8 (1)	Iон = -5 mA	Vcc - 0.5	-	Vcc	V
			Other pins	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		Port P7_0, P7_1, P8 (1)	IOL = 5 mA	-	-	0.5	V
			Other pins	IoL = 1 mA	-	-	0.5	V
VT+-VT-	Hysteresis	INT0,         INT1,         INT2,           INT3,         INT4,         INT5,           INT6,         INT7,         INT6,           INT0,         INT6,         INT7,           TRCIOA, TRCIOB,         TRCIOC, TRCIOD,           TRJ2IO, TRJ1IO,         TRJ2IO, TRCTRG,           TRCCLK, ADTRG,         INT6,           RXD0, RXD2, CLK0,         CLK2, SSI, SCL,           SDA, SSO         SO			0.05	0.4	_	V
		RESET, WKUP0			0.1	0.8	-	V
Ін	Input "H" current		VI = 3 V, Vcc = 3 V		-	_	5.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 3 V		-	_	-5.0	μA
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 3 V		25	80	140	kΩ
RfXIN	Feedback resistance	XIN			-	2.0	-	MΩ
RfxCIN	Feedback resistance	XCIN			-	14	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	-	V

Note:

This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.



## Table 5.51DC Characteristics (5) [1.8 V $\leq$ Vcc < 2.7 V]<br/>(Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Doro	meter	Condition		Sta	Unit		
Symbol	Fala	meter	Condition	Min.	Тур.	Max.	Unit	
Vон	Output "H" voltage		Port P7_0, P7_1, P8 (1)	lон = −2 mA	Vcc - 0.5	-	Vcc	V
			Other pins	Iон = -1 mA	Vcc - 0.5	_	Vcc	V
Vol	Output "L" voltage		Port P7_0, P7_1, P8 (1)	IOL = 2 mA	-	-	0.5	V
			Other pins	lo∟ = 1 mA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT2,           INT3, INT4, INT5,           INT6, INT7,           KI0, KI1, KI2, KI3,           KI4, KI5, KI6, KI7,           TRCIOA, TRCIOB,           TRCIOC, TRCIOD,           TRJOIO, TRJIIO,           TRJOIO, TRJIIO,           TRCLK, ADTRG,           RXD0, RXD2, CLK0,           CLK2, SSI, SCL,           SDA, SSO			0.05	0.4	-	V
		RESET, WKUP0			0.1	0.8	-	
Iн	Input "H" current		VI = 1.8 V, Vcc = 1.8 V		-	-	4.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 1.8 V		-	-	-4.0	μA
Rpullup	Pull-up resistance	1	VI = 0 V, Vcc = 1.8 V		85	220	500	kΩ
RfXIN	Feedback resistance	XIN			-	2.0	-	MΩ
Rfxcin	Feedback resistance	XCIN			-	14	_	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	-	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

