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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	56
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la67anfp-30

Table 1.8 Specifications (3)

Item	Function	Specification
LCD Drive Control Circuit	R8C/LA3A Group	Common output: Max. 4 pins Segment output: Max. 11 pins
	R8C/LA5A Group	Common output: Max. 4 pins Segment output: Max. 27 pins
	R8C/LA6A Group	Common output: Max. 4 pins Segment output: Max. 32 pins
	R8C/LA8A Group	Common output: Max. 4 pins Segment output: Max. 40 pins
Flash Memory		• Programming and erasure voltage: VCC = 1.8 V to 5.5 V (data flash VCC = 1.8 V to 5.5 V) • Programming and erasure endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ROM code protect, ID code check • On-chip debug function • On-board flash rewrite function
Operating Frequency/ Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 8 MHz (VCC = 1.8 V to 5.5 V)
Current Consumption		Typ. 4.7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 2.3 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 1.7 μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 0.5 μ A (VCC = 3.0 V, stop mode) Typ. 1.3 μ A (VCC = 3.0 V, power-off 2 mode, timer RH enabled) Typ. 0.01 μ A (VCC = 3.0 V, power-off 0 mode, timer RH disabled)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾

Note:

1. Specify the D version if D version functions are to be used.

Table 1.10 Product List for R8C/LA5A Group**Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA52ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	N Version
R5F2LA54ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA56ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA58ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0052JA-A	
R5F2LA52ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	D Version
R5F2LA54ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA56ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA58ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0052JA-A	

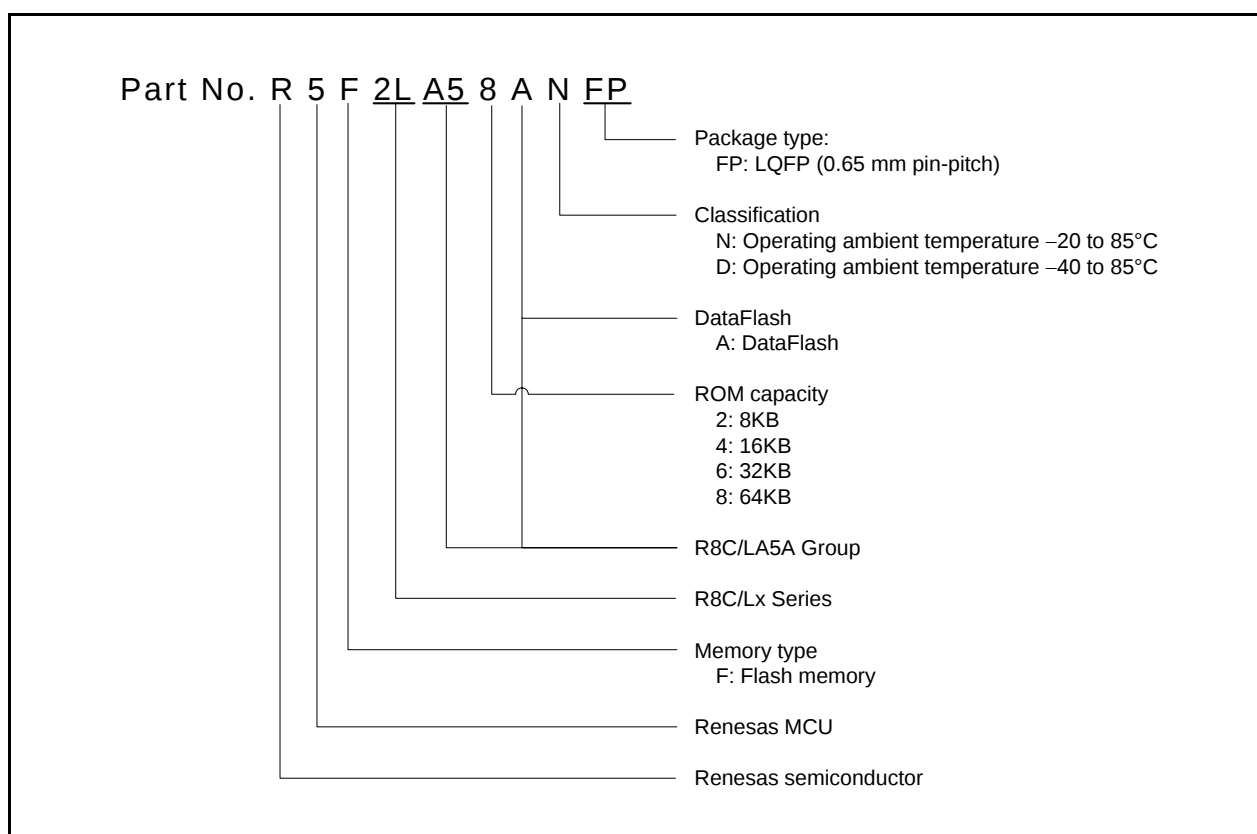
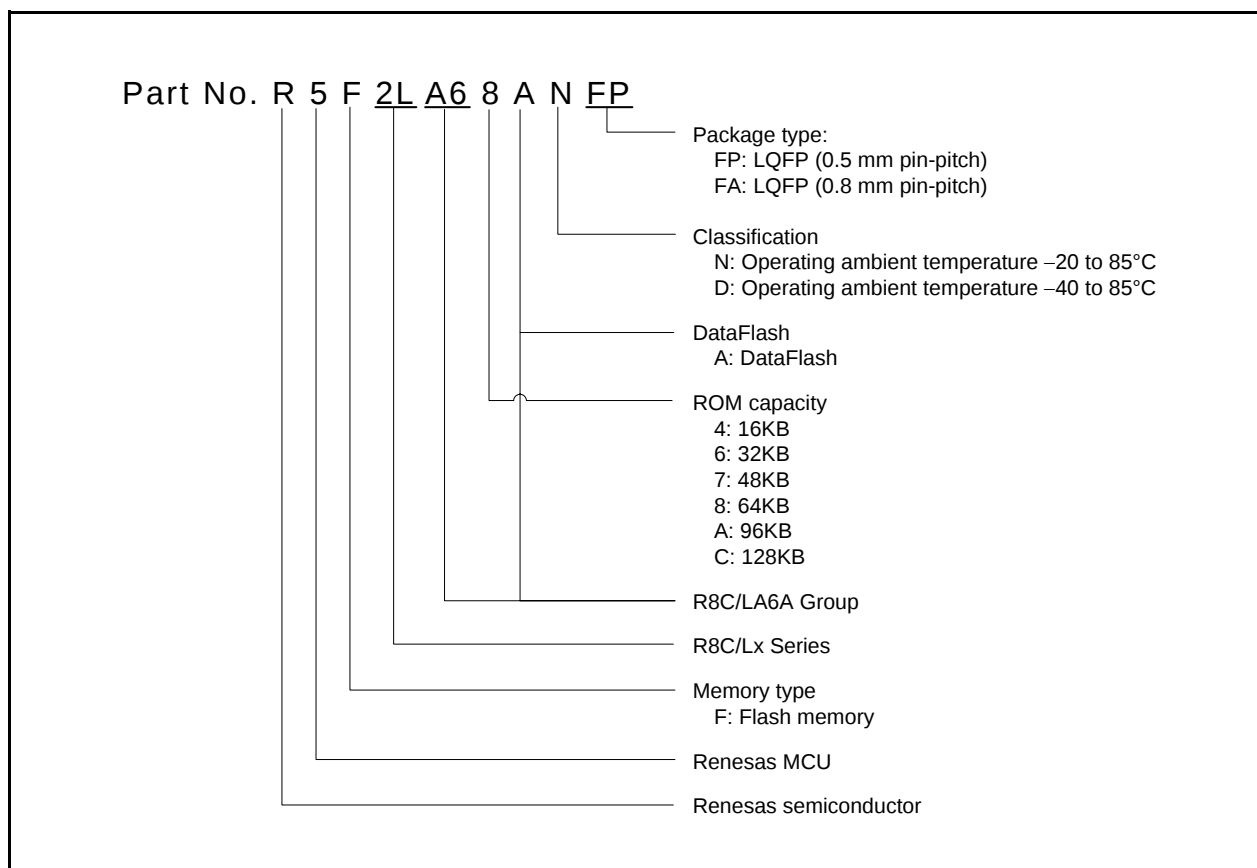
**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/LA5A Group**

Table 1.11 Product List for R8C/LA6A Group**Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA64ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	N Version
R5F2LA64ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AANFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AANFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA6CANFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6CANFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA64ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	D Version
R5F2LA64ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AADFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AADFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA6CADFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6CADFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	

**Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group**

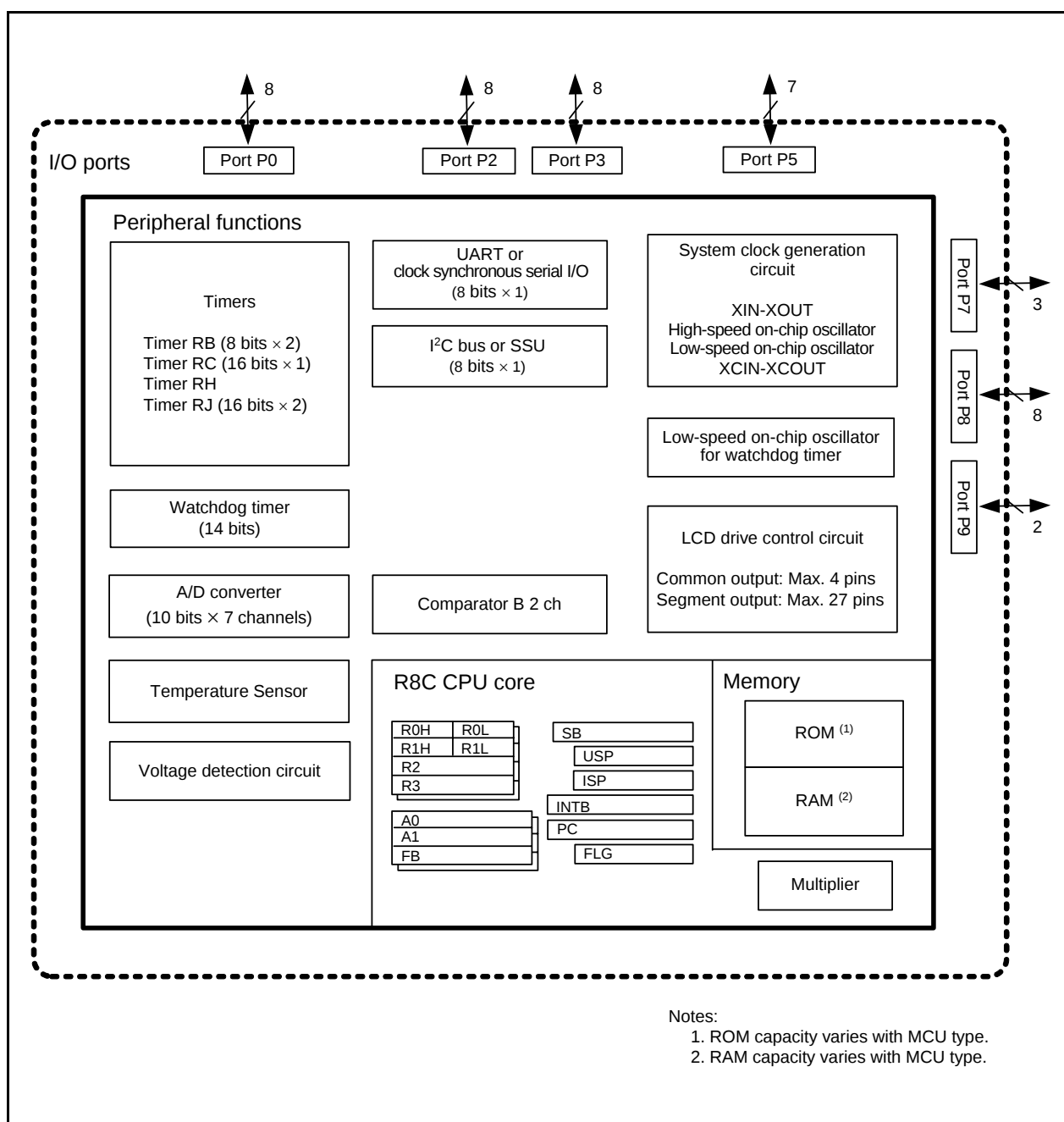


Figure 1.6 Block Diagram of R8C/LA5A Group

1.5 Pin Functions

Tables 1.18 and 1.19 list Pin Functions for R8C/LA5A Group, and Tables 1.20 and 1.21 list Pin Functions for R8C/LA8A Group.

Table 1.18 Pin Functions for R8C/LA5A Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	WKUP0	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$, $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RB	TRB0O, TRB1O	O	Timer RB output pins.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RH	TRHO	O	Timer RH output pin.
Timer RJ	TRJ0IO, TRJ1IO	I/O	Timer RJ I/O pins.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 4.4 SFR Information for R8C/LA5A Group (4) ⁽¹⁾

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh	A/D Control Register 2	ADCON2	00h
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h			
00E2h	Port P0 Direction Register	PD0	00h
00E3h			
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h			
00E9h	Port P5 Register	P5	XXh
00EAh			
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh	Port P7 Register	P7	XXh
00EEh			
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information for R8C/LA8A Group (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.18 SFR Information for R8C/LA8A Group (9) ⁽¹⁾

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
:			
2FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 5.5 Gain Amplifier Characteristics
(V_{SS} = 0 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V _{GAIN}	Gain amplifier operating range		0.4	—	AV _{CC} – 1.0	V
φ _{AD}	A/D conversion clock		1	—	5	MHz

Table 5.6 Comparator B Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{ref}	IVREF1, IVREF3 input reference voltage		0	—	V _{CC} – 1.4	V
V _I	IVCMP1, IVCMP3 input voltage		–0.3	—	V _{CC} + 0.3	V
—	Offset		—	5	100	mV
t _d	Comparator output delay time ⁽¹⁾	V _I = V _{ref} ± 100 mV	—	—	1	μs
I _{CMP}	Comparator operating current	V _{CC} = 5.0 V	—	12	—	μA

Note:

1. When the digital filter is disabled.

Table 5.9 Voltage Detection 0 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	50	500	μs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	100	500	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (2)			—	—	100	μs

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽¹⁾	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽¹⁾	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽¹⁾	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽¹⁾	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽¹⁾	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽¹⁾	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽¹⁾	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽¹⁾	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽¹⁾	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽¹⁾	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽¹⁾	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽¹⁾	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽¹⁾	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽¹⁾	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽¹⁾	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽¹⁾	At the falling of Vcc		4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		—	0.07	—	V
		Vdet1_6 to Vdet1_F selected		—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽²⁾	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	μs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	250	500	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾			—	—	100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.21 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]**(Topr = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

Symbol	Parameter		Condition							Standard			Unit	
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)		Max .
			XIN (2)	XCIN	High-Speed	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	4.7	10	mA
			10 MHz	Off	Off	125 kHz	No division	—			—	2.3	6	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled		—	2.9	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.8	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.0	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	2.1	—	mA
			Off	Off	10 MHz	125 kHz	No division	—			—	2.9	—	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.5	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh			—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0			—	106	300	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	54	200	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	54	200	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	36	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	2.5	31	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	3.1	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode		—	1.7	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM10 = 1	Topr = 25 °C Peripheral clock off		—	0.5	2.2	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off		—	1.2	—	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1			—	—	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25 °C		—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85 °C		—	0.02	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C		—	1.3	4.5	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C		—	2.2	—	μA

Notes:

1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.22 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage		Port P8 (1)	IOH = -2 mA	VCC - 0.5	—	VCC	V
			Other pins	IOH = -1 mA	VCC - 0.5	—	VCC	V
VOL	Output "L" voltage		Port P8 (1)	IOL = 2 mA	—	—	0.5	V
			Other pins	IOL = 1 mA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	—	V
		RESET, WKUP0			0.1	0.8	—	V
I _{IH}	Input "H" current		VI = 1.8 V, VCC = 1.8 V		—	—	4.0	μA
I _{IL}	Input "L" current		VI = 0 V, VCC = 1.8 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		VI = 0 V, VCC = 1.8 V		85	220	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	2.0	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

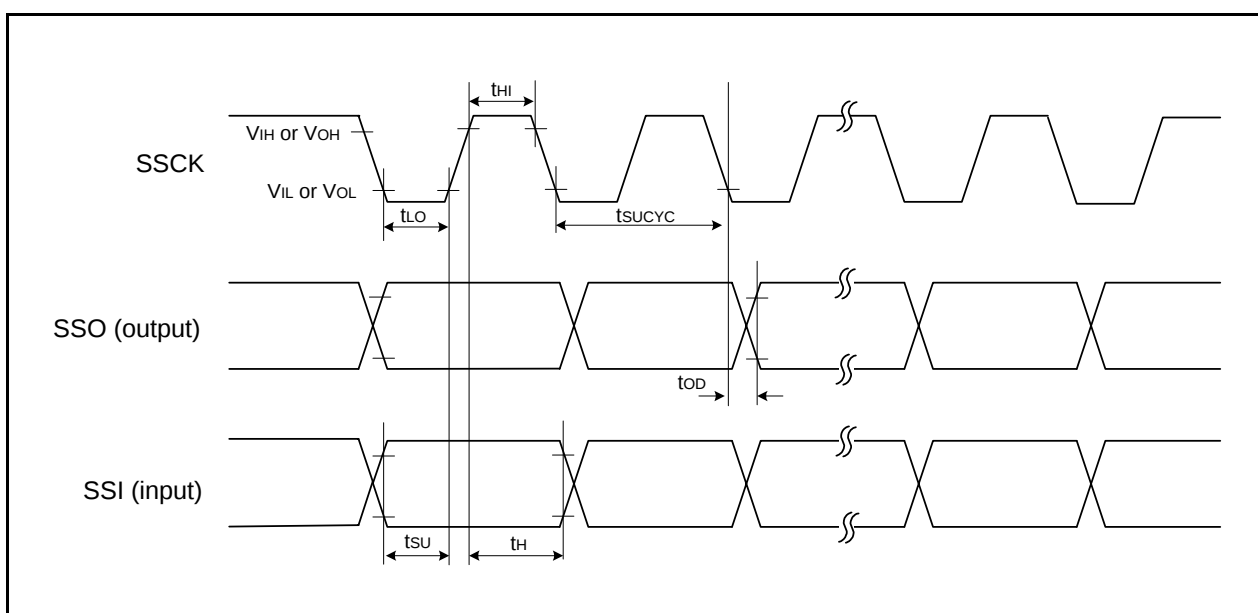


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

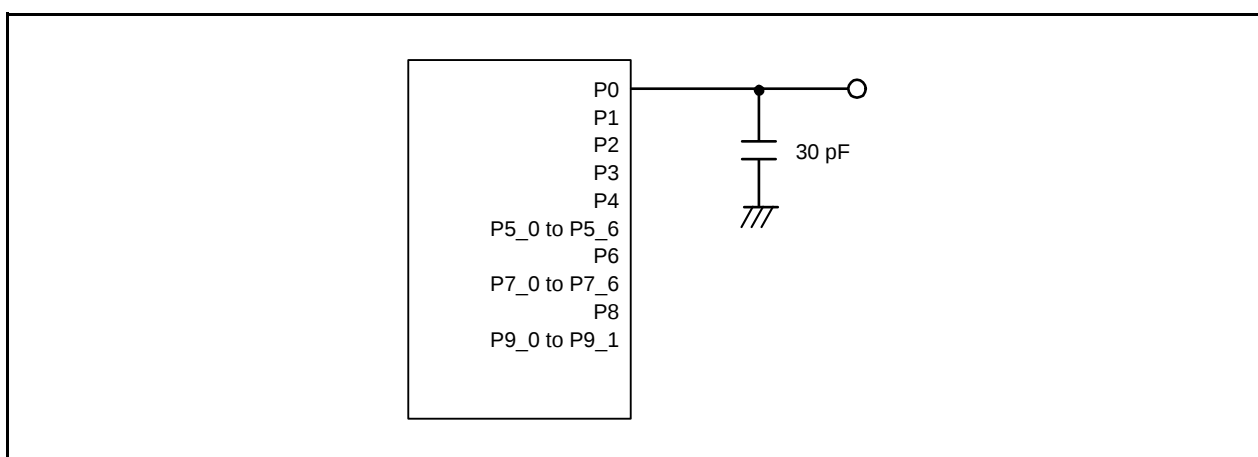


Figure 5.12 Ports P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, and P9_0 to P9_1 Timing Measurement Circuit

Table 5.52 DC Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	—			—	2.1	—	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.9	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.1	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh			—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0			—	106	300	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	54	200	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	54	200	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	36	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	2.5	31	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	2.4	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode		—	1.7	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	0.5	2.2	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	1.2	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25°C		—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85°C		—	0.02	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C		—	1.2	4	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C		—	2	—	μA

Notes:

1. $V_{CC} = 1.8\text{ V to }2.7\text{ V}$, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. $V_{CC} = 2.2\text{ V}$
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

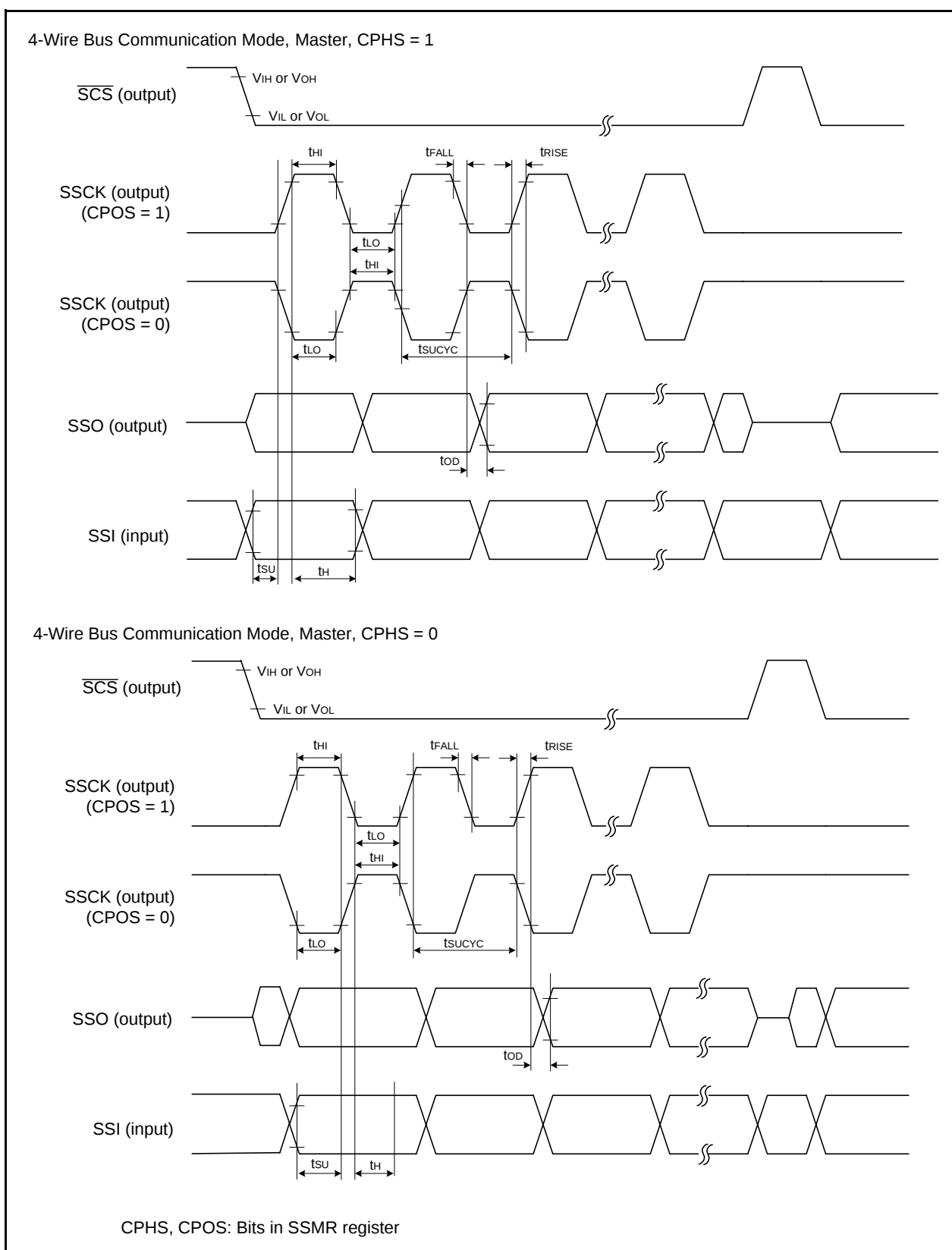


Figure 5.15 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

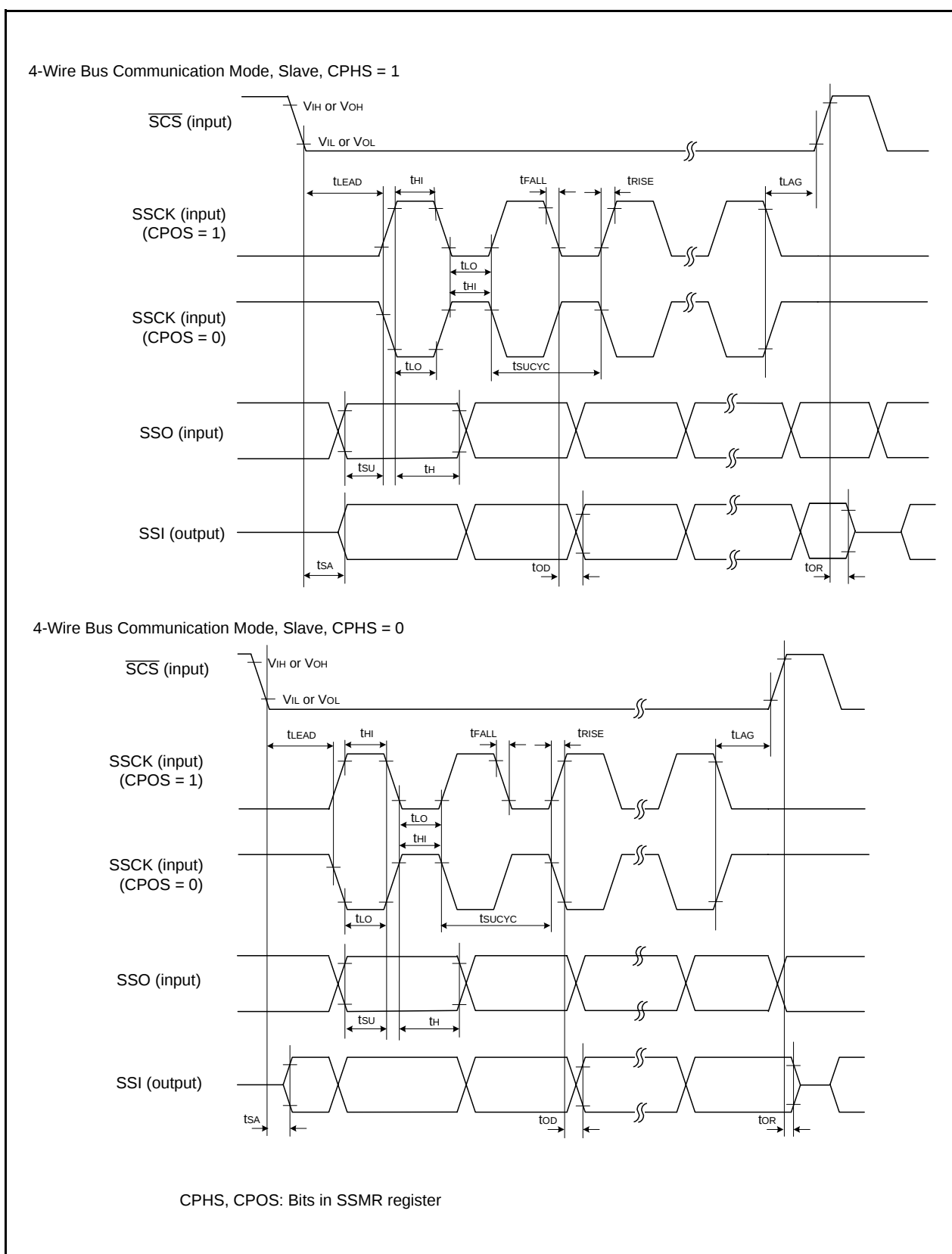


Figure 5.16 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

