Renesas Electronics America Inc - R5F2LA68ANFA#U0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la68anfa-u0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.
Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins
	High current drive ports	8 pins	8 pins	8 pins	10 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	6 pins	8 pins	8 pins
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin
	Timer RJ1 output pin	None	None	None	1 pin
	Timer RJ2 I/O pin	None	None	None	1 pin
	Timer RJ2 output pin	None	None	None	1 pin
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin
Serial interface	UART2	None	None	1 pin	1 pin
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins
	Reference input voltage	1 pin	2 pins	2 pins	2 pins
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin
Packages		32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

Table 1.2 Programmable I/O Ports Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Programmable I/O Port	R8C/LA3A Group Total: 26 I/O pins								R8C/LA5A Group Total: 44 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	✓	—	—	—	—	—	—	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:
1. The symbol "✓" indicates a programmable I/O port.
2. The symbol "—" indicates the settings should be made as follows:
   - Set 0 to the corresponding bits in the PDi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.
   - Set 0 to the corresponding bits in the Pi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.

Table 1.3 Programmable I/O Ports Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:
1. The symbol "✓" indicates a programmable I/O port.
2. The symbol "—" indicates the settings should be made as follows:
   - Set 0 to the corresponding bits in the PDi (i = 1, 4 to 7, 9) register. When read, the content is 0.
   - Set 0 to the corresponding bits in the Pi (i = 1, 4 to 7, 9) register. When read, the content is 0.
   - Set 0 to the corresponding bits in the P7DRR register. When read, the content is 0.

Table 1.4 LCD Display Function Pins Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Shared I/O Port	R8C/LA3A Group Common output: Max. 4 Segment output: Max. 11								R8C/LA5A Group Common output: Max. 4 Segment output: Max. 27							
P0	—	—	—	—	—	—	—	—	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P2	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P3	—	—	—	—	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24

Notes:
1. The symbol "—" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0, LSE2, and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

Table 1.5 LCD Display Function Pins Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3

Notes:
1. The symbol "—" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE1, LSE4 and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.9 Product List for R8C/LA3A Group **Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA32ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	N Version
R5F2LA34ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	
R5F2LA32ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	D Version
R5F2LA34ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	

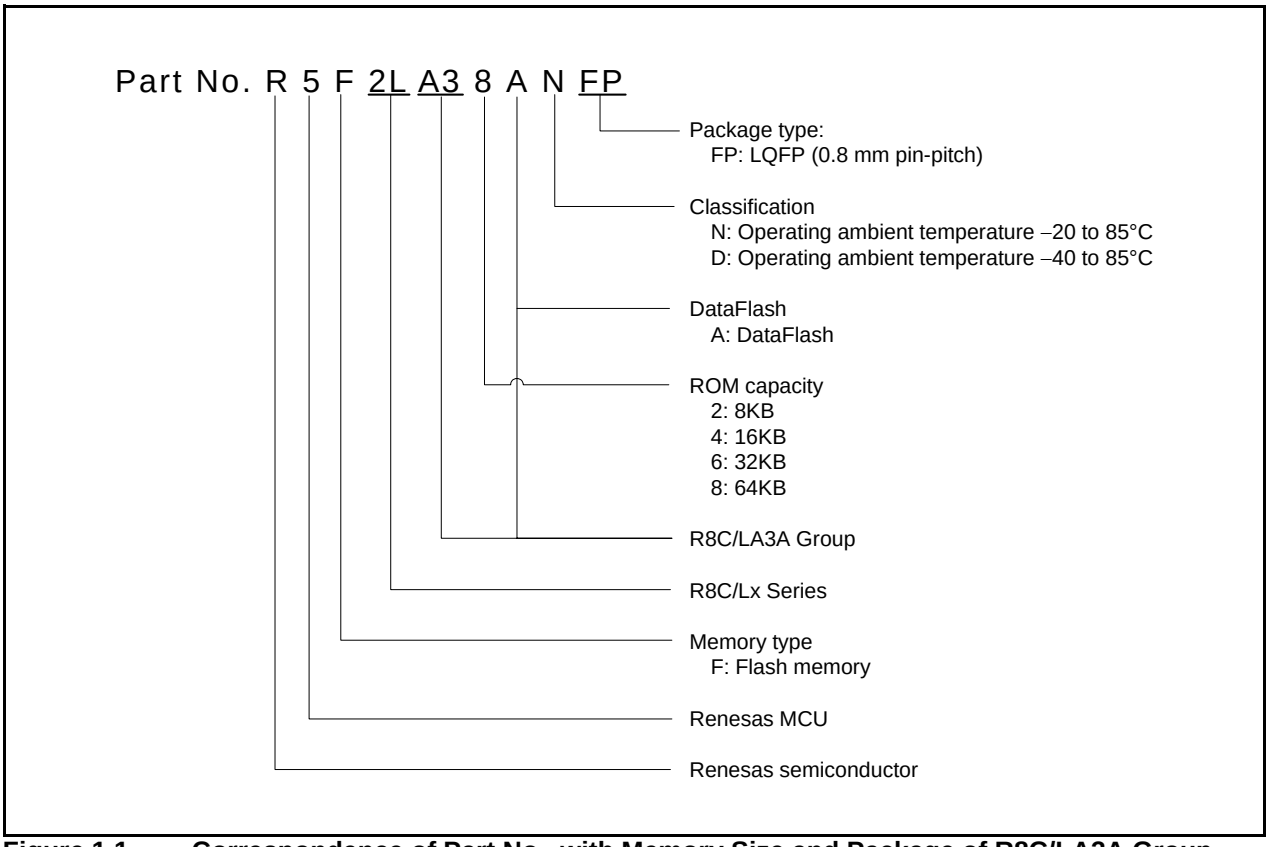


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/LA3A Group. Figure 1.6 shows a Block Diagram of R8C/LA5A Group. Figure 1.7 shows a Block Diagram of R8C/LA6A Group. Figure 1.8 shows a Block Diagram of R8C/LA8A Group.

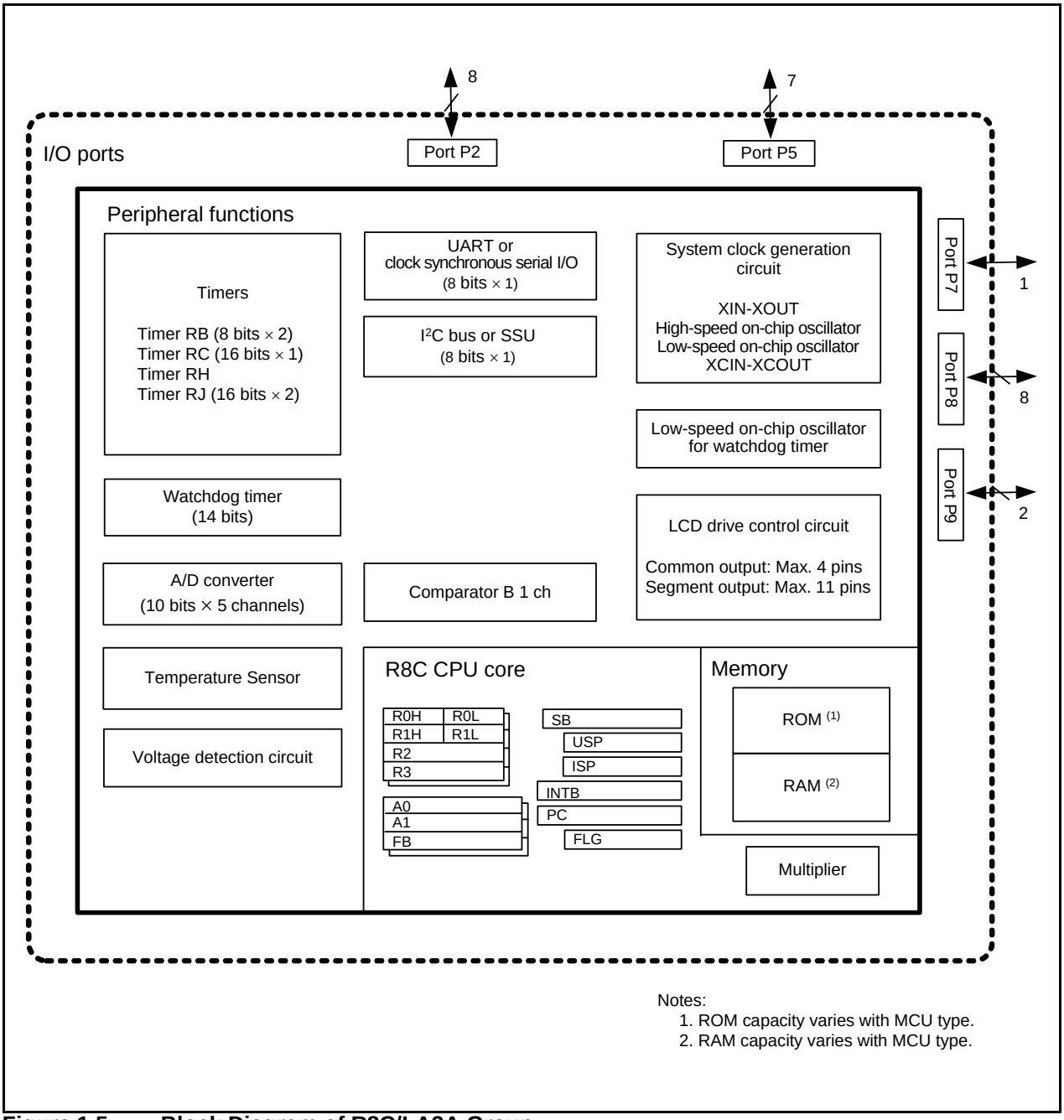


Figure 1.5 Block Diagram of R8C/LA3A Group

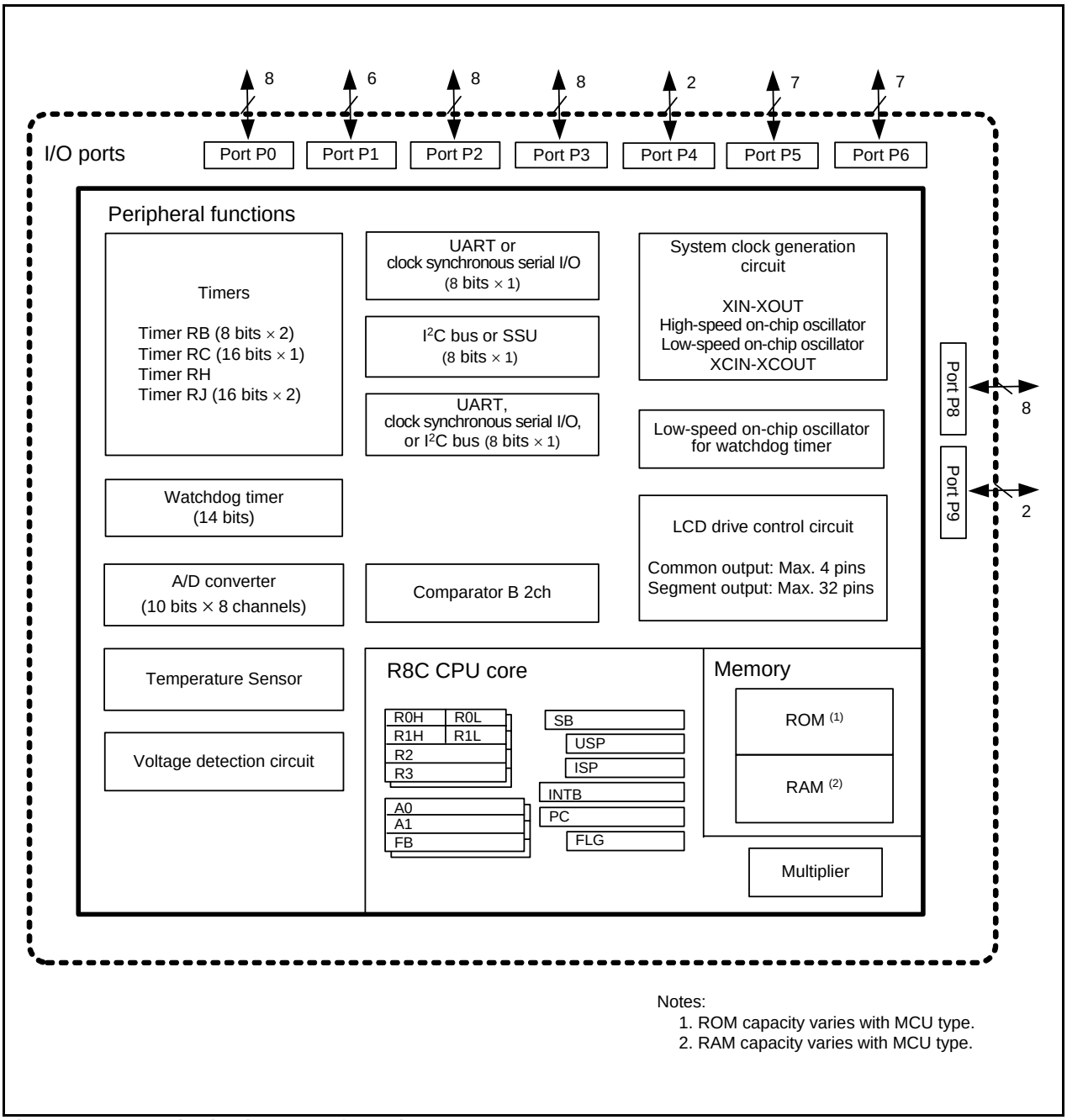
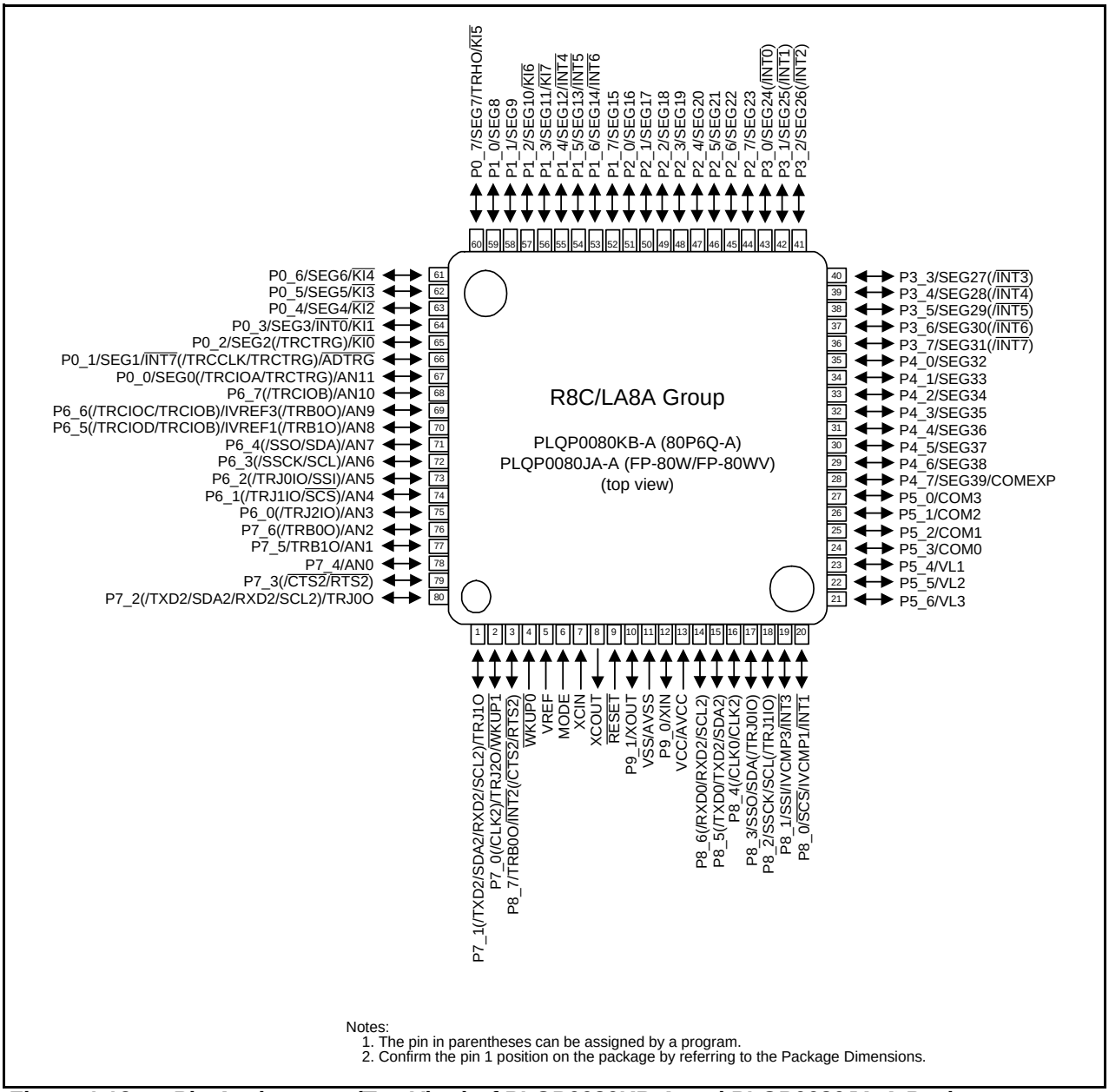


Figure 1.7 Block Diagram of R8C/LA6A Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.12 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

Table 1.19 Pin Functions for R8C/LA5A Group (2)

Item	Pin Name	I/O Type	Description
I^2C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{SCS}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN0 to AN6	I	A/D converter analog input pins.
	$\overline{ADTRG}$	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O ports	P0_0 to P0_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_6, P7_0 to P7_2, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Port P8 can be used as LED drive ports.
Segment output	SEG0 to SEG26	O	LCD segment output pins.
Common output	COM0 to COM3, COMEXP	O	LCD common output pins.
LCD power supply	VL1	I	Apply the following voltage: 1 V ≤ VL1 ≤ VCC and VL1 ≤ VL2.
	VL2	I	Apply the following voltage: VL2 ≤ 5.5 V and VL1 ≤ VL2 ≤ VL3.
	VL3	I	Apply the following voltage: VL3 ≤ 5.5 V and VL2 ≤ VL3.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.12 SFR Information for R8C/LA8A Group (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.14 SFR Information for R8C/LA8A Group (5) (1)

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h (2)
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h (2)
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h (2)
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h (2)
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b (2)
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b (2)
0116h	Timer RH Year Data Register	TRHYR	XXh 00h (2)
0117h	Timer RH Control Register	TRHCR	XXX00X0Xb 000XX1X0b (2)
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb (2)
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h (2)
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b (2)
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h (2)
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h (2)
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h (2)
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h (2)
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b (2)
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. This is the reset value after reset by RTCRST bit in TRHCR register.

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
(Vcc/AVcc = Vref = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	8	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	ms
tSAMP	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
IVref	Vref current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
Vref	Reference voltage				1.8	–	AVcc	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:
1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VTMP	Temperature sensor output voltage	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	550	600	650	mV
–	Temperature coefficient	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	–	–2.1	–	mV/°C
–	Start-up time	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	–	200	µs
ITMP	Operating current	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	100	–	µA

Table 5.7 Flash Memory (Program ROM) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time		–	0.12	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.9 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	50	500	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	100	500	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc		4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		–	0.07	–	V
		Vdet1_6 to Vdet1_F selected		–	0.10	–	V
–	Voltage detection 1 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	250	500	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

5.2.1 Absolute Maximum Ratings

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

Table 5.48 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

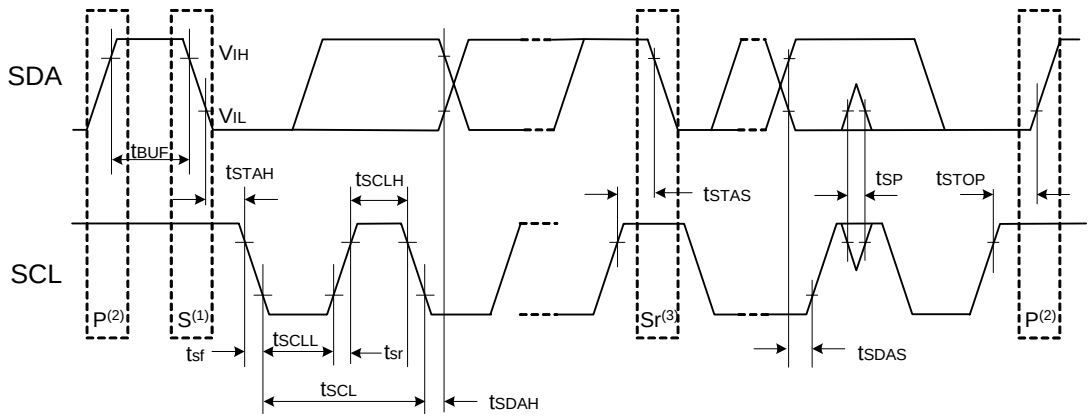
Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	63	220	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	60	220	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	46	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	4.6	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	2.4	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.03	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.8	6.4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.7	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.54 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	–	–	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	–	–	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	–	–	ns
tsf	SCL, SDA input fall time		–	–	300	ns
tSP	SCL, SDA input spike pulse rejection time		–	–	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	–	–	ns
tSTAH	Start condition input hold time		3tCYC (1)	–	–	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	–	–	ns
tSTOP	Stop condition input setup time		3tCYC (1)	–	–	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	–	–	ns
tSDAH	Data input hold time		10	–	–	ns

Note:
1. 1tCYC = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.18 I/O Timing of I²C bus Interface

Table 5.57 Timing Requirements of Serial Interface
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	300	–	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	150	–	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	150	–	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	–	80	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	0	–	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	70	–	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	90	–	90	–	ns

i = 0, 2

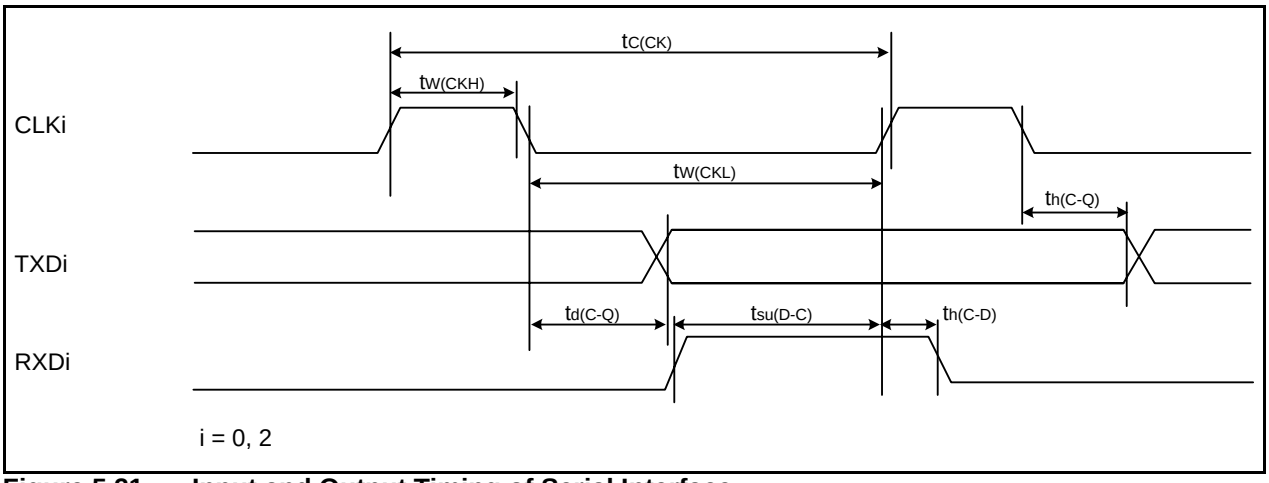


Figure 5.21 Input and Output Timing of Serial Interface

Table 5.58 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 7) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	380 (1)	–	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	380 (2)	–	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

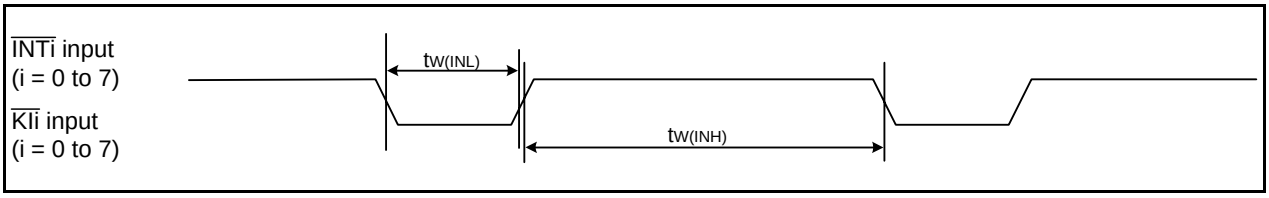


Figure 5.22 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$

REVISION HISTORY	R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan 18, 2010	—	First Edition issued
0.02	Jul 16, 2010	2	Table 1.1 revised
		3	Table 1.2 revised
		4	Tables 1.4 and 1.5 revised
		5	Table 1.6 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		8	Table 1.9 and Figure 1.1 revised
		9	Table 1.10 and Figure 1.2 revised
		10	Table 1.11 and Figure 1.3 revised
		11	Table 1.12 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		16	Figure 1.9 revised
		17	Figure 1.10 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		21	Figure 1.12 revised
		25	Table 1.18 revised
		26	Table 1.19 revised
		30	Figure 3.1 revised
		31	Table 4.1, Note 3 revised
		35	Table 4.5 revised
		41 to 44	Package Dimensions revised
1.00	Dec 21, 2010	All	“Preliminary” and “Under development” deleted
		2	Table 1.1 revised
		3	Tables 1.2 and 1.3 Note 2 revised
		4	Tables 1.4 and 1.5 Note 1 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		10	Table 1.11 and Figure 1.3 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		15	Figure 1.8 revised
		16	Figure 1.9 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		22	Table 1.15 revised
		23	Table 1.16 revised
		24	Table 1.17 revised
		25, 26	Tables 1.18 and 1.19 Pin Functions for R8C/LA5A Group added

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